Sensors and Materials, Vol. 26, No. 6 (2014) 393–402
MYU Tokyo

S & M 1007

Sapphire Substrate Processing for High-Performance GaN-Based Light-Emitting Diodes –Micropatterning of Sapphire Substrates and Its Effect on Light Enhancement in GaN-Based Light-Emitting Diodes–

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(Received December 2, 2013; accepted March 5, 2014)

Key words: light-emitting diodes (LEDs), patterned sapphire substrate (PSS), wet etching, GaN, internal quantum efficiency, light extraction efficiency

We investigated the pattern size control mechanism of patterned sapphire substrates (PSSs) fabricated by wet etching and evaluated the effect of the pattern size of the PSSs on the efficiency of light-emitting diodes (LEDs). It was found that the pattern height, top diameter, and bottom diameter can be controlled by the etching time and diameter of the etching mask. The angle of side surfaces of patterns showed a constant value, which corresponds to the $\{10\bar{1}2\}$ plane of sapphire crystals, when changing the etching time and diameter of the etching mask. On the basis of the pattern size control mechanism that we have established, PSSs with different diameters were successfully fabricated and the efficiency of the LEDs on the PSSs was evaluated. As a result, the light output of the LEDs on a PSS with the largest pattern diameter in this study was 1.2 times higher than that on planar sapphire. In addition, it was shown that the light intensity of the LEDs proportionally increases with increasing pattern diameter of the PSS, suggesting that the area of the side surface for patterns could affect the increase in the light intensity of the LEDs.

1. Introduction

GaN-based light-emitting diodes (LEDs) have attracted much attention as a key technology for energy-saving devices.[1] The main applications of GaN-based LEDs are backlight of liquid crystal display (LCD), general lighting, automobile headlights, and

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so on. There is no doubt on the larger potential of GaN-based LED devices, since low energy consumption can be achieved by replacing conventional light sources with GaN-based LED devices. However, the current performance of GaN-based LEDs has not yet reached perfection in comparison with theoretical expectations.[2–4]

There are mainly two reasons for the insufficient performance of GaN-based LEDs: high dislocation densities in the LED films and low light extraction efficiency. The large mismatch in both the lattice constant and thermal expansion coefficient between GaN and sapphire, which is commonly used as a substrate for GaN epitaxial growth, is the main cause of the former problem.[5] For the latter one, a narrow escape cone of light, which is around 24.7°, has been pointed out, as there is a large gap in refractive index between GaN and air.[6] Namely, the current issues are summarized as low internal quantum efficiency (IQE) and low light extraction efficiency (LEE).

The patterned sapphire substrate (PSS) is becoming a common substrate as compared with planar sapphire substrates, since the use of the PSS is one of the key techniques to improve IQE and LEE at the same time.[7,8] It has bumps with a diameter, a pitch, and a height of a few microns on the entire surface of the sapphire substrate. As the growth of GaN films starts on the planar surface between bumps, and then the grown films coalesce over bumps by epitaxial lateral overgrowth (ELOG), threading dislocation densities (TDDs) are reduced by bending and mutual annihilation of dislocations, which contribute to the IQE improvement. In addition, the PSS has a strong effect on LEE improvement, since the patterned surface enhances the light reflections as compared with the planar surface. This increases the probability of light entering into the narrow escape cone, resulting in an increment in the amount in extracted light from LEDs.

In the PSS fabrication, conventional photolithography and dry etching are used for the mass production of PSSs.[9] On the other hand, a wet-etched PSS, which is fabricated by conventional photolithography and wet etching, has recently attracted much attention, as it leads to a lower fabrication cost than a dry-etched PSS. Since GaN-based LEDs with a lower fabrication cost and a higher light intensity have been required in the LED market,[10] the development of the wet-etched PSS is considerably important for meeting market requirements. However, there are still a few reports dealing with the wet-etched PSS and its effect on LED performance, although there are many research studies on the dry-etched PSS.[11,12] In particular, the number of reports on the pattern size control and its effect on the light efficiency of the LEDs is limited in the wet-etched PSS, although the effect of pattern size on the light output of the LEDs has been reported in the dry-etched PSS.[13–16]

In this work, we investigate the pattern size control mechanism of the wet-etched PSS and evaluate the effect of pattern size on the efficiency of GaN-based LEDs. We demonstrate that pattern height, top diameter, and bottom diameter can be controlled by etching conditions, particularly, the etching time and diameter of the etching mask. Patterns with a flat top surface and threefold symmetric side surfaces are obtained under these etching conditions. The angle of side surfaces of patterns shows a constant value, which corresponds to the $\{10\bar{1}2\}$ plane of sapphire crystals, when changing the etching conditions. On the basis of the established control mechanism for the pattern size of the wet-etched PSS, PSSs with different diameters and GaN-based LEDs on the

PSSs are successfully fabricated. It is demonstrated that the light intensity of the LEDs proportionally increases with increasing pattern diameter, which suggests that the area of the side surfaces of patterns could affect the increase in the light intensity of the LEDs.

2. Experimental Procedure

Figure 1 shows a fabrication process for the wet-etched PSS in this study. Sapphire substrates of 2 inch diameter with the (0001) plane of sapphire crystals were used for PSS fabrication. SiO_2 films of 0.1 μm thickness were deposited onto the substrates by plasma-enhanced chemical vapor deposition (PECVD). Subsequently, triangular arrays of 6 μm pitch and different diameters were defined by photolithography. The triangular arrays were aligned along the $\langle 10\bar{1}2 \rangle$ direction of sapphire crystals. A HF solution was used for SiO_2 etching with a patterned photoresist as a SiO_2 etching mask. After the removal of the patterned photoresist, SiO_2 patterns for the sapphire etching mask were obtained. 500 ml of 3:1 mixture solution of H_2SO_4 and H_3PO_4 at the temperature of 573 K was used for sapphire etching. Etching times of 1, 5, 10, and 15 min were applied. After sapphire etching, the SiO_2 mask was removed using the HF solution. The obtained sapphire pattern shape was measured by atomic force microscopy (AFM). To evaluate the effect of pattern size on the light output of the LEDs, GaN-based LEDs were grown on PSSs with different diameters by metal organic chemical vapor deposition (MOCVD).

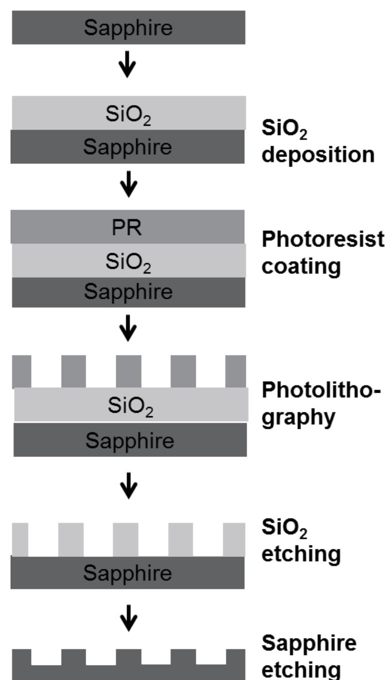

Fig. 1. Process flow for PSS fabrication by wet etching.

3. Results and Discussion

Figures 2(a) and 2(b) show the AFM image and schematic of a typical sapphire pattern shape for the wet-etched PSS, respectively. Bumps with a flat top surface and threefold symmetric side surfaces were obtained by anisotropic etching. The side surfaces emerged vertical to the $\langle 10\bar{1}0 \rangle$ direction of sapphire crystals, indicating that a side surface corresponds to the $\{10\bar{1}k\}$ plane. As described in Fig. 2(b), the pattern height, pattern top diameter, pattern bottom diameter, pattern pitch, slope angle across the side surface, and slope angle across the edge line were defined as H, $D1$, $D2$, P, $\theta 1$, and $\theta 2$, respectively.

To investigate the pattern size control mechanism for the wet-etched PSS, the relationship among H, $D1$, $D2$, SiO_2 diameter (Ds), and etching time (T) is discussed. Figure 3 shows a plot of H as a function of T. It was shown that H proportionally increases with increasing T. The slope in this plot corresponds to the etching rate of the (0001) plane of sapphire crystals, which is about 0.1 μm/min. This etching rate is in good agreement with that reported in another paper.[11] Figure 4 shows plots of $D1$ as a function of T for different Ds values. We found that $D1$ is affected not by T but by Ds. $D1$ was almost the same as Ds. Figure 5 shows plots of $D2$ as a function of T

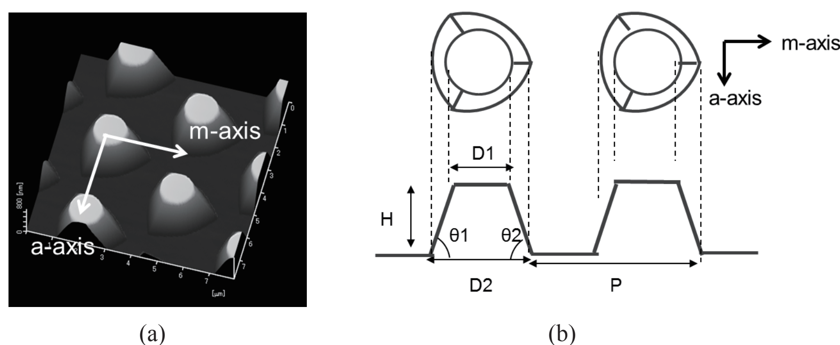

Fig. 2. (a) AFM image and (b) schematic drawing of a typical sapphire pattern shape fabricated by wet etching.

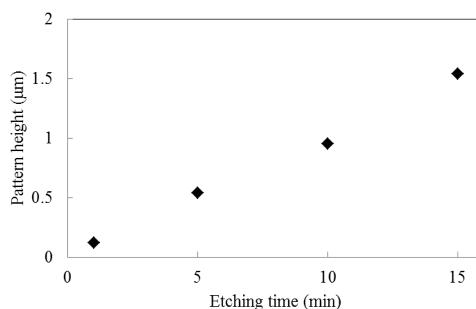

Fig. 3. Plot of pattern height as a function of etching time.

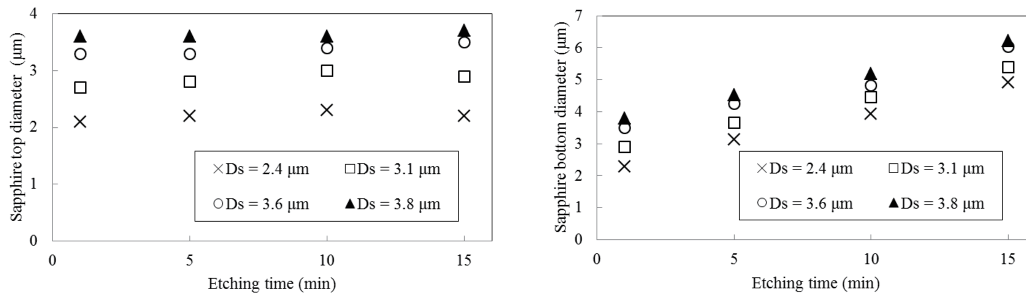

Fig. 4 (left). Plots of sapphire pattern top diameter as a function of etching time for different SiO_2 mask diameters.
Fig. 5 (right). Plots of sapphire pattern bottom diameter as a function of etching time for different SiO_2 mask diameters.

for different *Ds* values. It was found that *D*2 proportionally increases with increasing *T*. In addition, we confirmed that *D*2 can also be controlled by *Ds*. On the basis of the relationship between pattern size and etching conditions, the pattern height and pattern top diameter can be controlled by etching time and the SiO_2 diameter, respectively. Moreover, the pattern bottom diameter can be controlled by both the etching time and the SiO_2 diameter.

Considering the relationship among pattern size, etching conditions, and angles of side surfaces, we estimate the angles of the side surfaces from the geometry of the sapphire pattern shape and the obtained pattern sizes, as it is well known that the angles of the side surfaces for patterns always show the same value under some etching conditions for the wet etching of Si crystals.[17] For example, in the case of wet etching of Si substrates with (100) planes using KOH solutions, (111) planes always emerged as the side surfaces of patterns owing to the lower etching rate for the (111) plane than for other planes. If the angle of the side surfaces for sapphire patterns is controlled by the etching rate of crystal planes, it should correlate with the etching conditions. Figure 6 shows a schematic of the pattern shape geometry, which is considered in the calculation of the side surface angle. As shown in the schematic, when *H*, *D*1, and *D*2 are fixed, the angles of the side surface ($\theta 1$) and edge line ($\theta 2$) can be described as

$$\theta 1 = \tan^{-1}\left[\frac{H}{(\frac{1}{3}D2 - \frac{1}{3}D1)}\right], \tag{1}$$

$$\theta 2 = \tan^{-1}\left[\frac{H}{(\frac{2}{3}D2 - \frac{2}{3}D1)}\right]. \tag{2}$$

In the schematic, the top diameter is approximated by considering a triangular shape. By assigning the pattern size obtained experimentally to these equations, $\theta 1$ and $\theta 2$ can be calculated. Figures 7(a) and 7(b) show plots of the calculated $\theta 1$ and $\theta 2$ as a function of

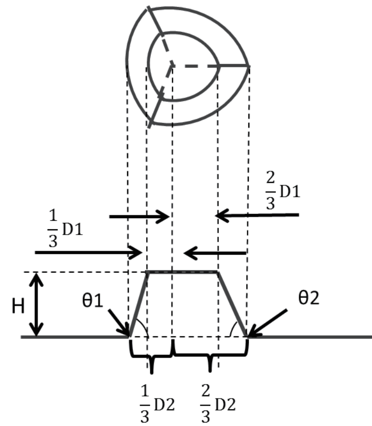

Fig. 6. Schematic drawing of pattern shape for wet-etched PSS used for calculation of side surface angle.

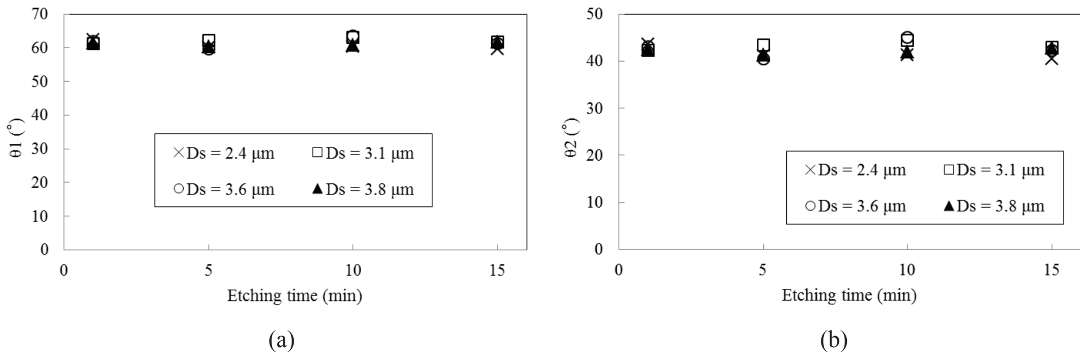

Fig. 7. Plots of calculated (a) $\theta 1$ and (b) $\theta 2$ as a function of etching time for different SiO_2 diameters.

T for different *Ds* values. There is no dependence of both $\theta 1$ and $\theta 2$ on *T* and *Ds*. The angles $\theta 1$ and $\theta 2$ are about 60 and 40°, respectively. The side surface with $\theta 1$ is not a flat plane but a curved plane as shown in Fig. 2, indicating that it is not an exact crystal plane. However, the angle $\theta 1$ remains the same under any etching conditions. Therefore, this result indicates that the low etching rate and stability of the $\{10\bar{1}2\}$ plane of sapphire crystals, which is crystallographically defined from the angle of the side surface with $\theta 1$.

To confirm the stability of the $\{10\bar{1}2\}$ plane, the sapphire substrate with a $(10\bar{1}2)$ plane was also etched. The stripe mask fabricated along $\langle 11\bar{2}0 \rangle$ on the sapphire substrate was etched using the same mixture solution and temperature described in the experimental procedure. If the $\{10\bar{1}2\}$ plane is more stable than other planes, a stripe pattern emerges first and then disappears. Figures 8(a)–8(c) show a schematic of the stripe mask on the sapphire substrate and AFM images of the obtained stripe pattern

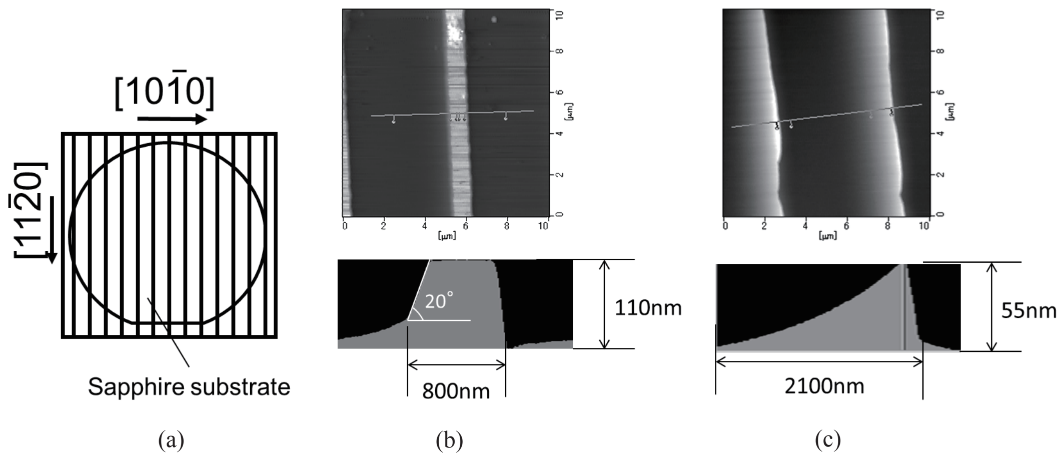

Fig. 8. (a) Schematic of stripe mask direction on sapphire substrate, (b) AFM images of stripe pattern for (10$\bar{1}$2) sapphire substrate after 10 min etching, and (c) after 20 min etching.

for the sapphire substrate with the (10$\bar{1}$2) plane after wet etching for 10 and 20 min, respectively. As shown in Fig. 8(b), the side surface with an angle of about 20° against the (10$\bar{1}$2) plane was obtained. This plane is crystallographically defined as the {10$\bar{1}$4} plane of sapphire crystals. When the etching time was extended, as shown in Fig. 8(c), the {10$\bar{1}$4} plane almost disappeared and the height of the stripe pattern decreased. Finally, when the etching time of 30 min was applied, the stripe pattern disappeared. From these results, the {10$\bar{1}$2} plane is considered more stable than the other planes, such as the {10$\bar{1}$4} plane. This stability could be explained by the atomic density of crystal planes. For Si crystals, the stability of crystal planes is discussed by considering their atomic density.[17] The lower etching rate and stability of (111) for Si crystals are explained by the higher atomic density of the (111) plane. In the case of sapphire crystals, as the {10$\bar{1}$2} plane emerged after the wet etching, it is expected that the {10$\bar{1}$2} plane will have a higher atomic density than the other planes. Thus, we confirmed the stability of the {10$\bar{1}$2} plane; however, to discuss the stability of the {10$\bar{1}$2} plane in detail, further investigations, such as a simulation of the atomic density of the crystal planes, will be necessary.

On the basis of the above discussion, we summarize the size control mechanism of the wet-etched PSS. The relationship among pattern height (H), pattern top diameter ($D1$), pattern bottom diameter ($D2$), etching time (T), and SiO_2 diameter (Ds) can be described as

$$H = 0.1 \times T, \tag{3}$$

$$D1 = Ds, \tag{4}$$

$$D2 = \left(\frac{0.1}{\tan 60°} + \frac{0.1}{\tan 40°}\right) \times T + Ds. \quad (5)$$

As these equations are based on the experimental results obtained under the etching conditions considered, the etching rate, undercut, and side surface angle are expected to change under other etching conditions. However, we found that pattern size can be designed using these equations under the etching conditions considered. Figure 9 shows a schematic model of pattern size control for the wet-etched PSS. With increasing etching time, the pattern height proportionally increases, which depends on the etching rate of the (0001) plane. With increasing SiO_2 diameter, the pattern top diameter proportionally increases, as it is almost the same as the SiO_2 diameter. With increasing either etching time or SiO_2 diameter, pattern bottom diameter proportionally increases, since the angle of the side surface showed a constant value for all the etching conditions, which corresponds to the $\{10\bar{1}2\}$ plane.

As discussed above, we established the size control mechanism for the wet-etched PSS. Here, the actual effects of pattern size on the LED performance should be worth discussing. In this study, we focus on the effect of pattern diameter on the light output of GaN-based LEDs. We fabricate five types of wet-etched PSS with different diameters, the same pattern height, and the same pattern pitch, which are denoted as Samples A, B, C, D, and E. Their pattern sizes are listed in Table 1. Figure 10 shows a plot of the light output of the LEDs on the PSS as a function of pattern diameter. The LEDs fabricated on Sample A, which has the largest diameter in this study, showed the highest light intensity, and their light output was 1.2 times higher than that of the LEDs on planar sapphire. It was also observed that the light output of the LEDs proportionally increases with increasing pattern diameter. Considering the cause of the dependence of pattern diameter on the light output of the LEDs, it seems that the area of the side surface for patterns would

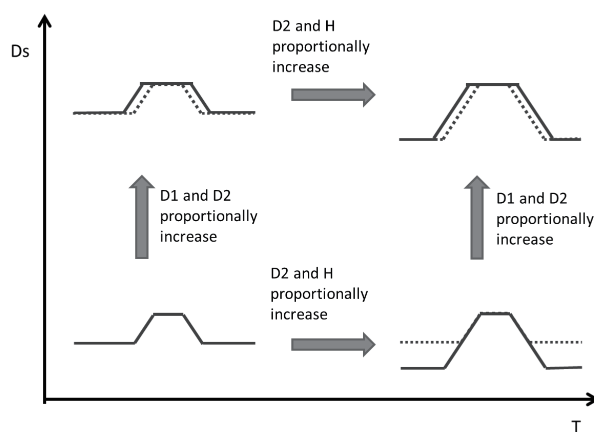

Fig. 9. Schematic model of pattern size control for wet-etched PSS.

Table 1
Pattern size of wet-etched PSS used for LED fabrication.

Sample	Size (μm)			
	*D*1	*D*2	*H*	*P*
A	2.2	4.9	1.4	6.0
B	2.0	4.5	1.4	6.0
C	1.4	3.7	1.4	6.0
D	0.8	3.0	1.4	6.0
E	0.6	2.7	1.4	6.0

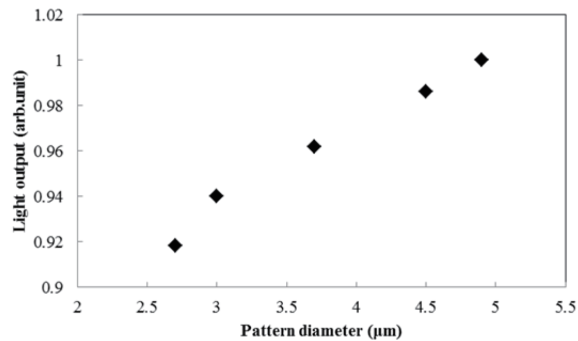

Fig. 10. Plot of light output of the LEDs on PSS as a function of pattern diameter.

affect the light intensity of the LEDs. With increasing pattern diameter, the surface area for patterns also increases. The increment in surface area for patterns causes an increase in the possibility of light reflection on patterns, resulting in the improvement of the light extraction of the LEDs. Flat-top areas of patterns are not markedly effective for the improvement of light extraction, since light reflection on a flat area cannot change the propagation angle of the emitted light. Thus, it was implied that the increase in light output with increasing pattern diameter is caused by the increase in side surface area. Although further comprehensive investigations, such as that focusing on the dependence of pattern height on the light intensity of the LEDs on the PSS, are necessary to confirm the effect of side surfaces on the light output of the LEDs, it was experimentally verified that the increase in light output with increasing pattern diameter is caused by the increase in side surface area.

4. Conclusions

We investigated the pattern size control mechanism of PSSs fabricated by wet etching and evaluated the effect of pattern size on the efficiency of GaN-based LEDs. It was found that the pattern height, top diameter, and bottom diameter can be controlled by the etching time and diameter of the etching mask. The angle of side surfaces for patterns

showed a constant value, which corresponds to the $\{10\bar{1}2\}$ plane of sapphire crystals, when changing the etching time and diameter of the etching mask. On the basis of the pattern size control mechanism that we have established, PSSs with different diameters and GaN-based LEDs on the PSSs were successfully fabricated. As a result, we observed that the light output of the LEDs on the PSS with the largest pattern diameter in this study is 1.2 times higher than that on planar sapphire. In addition, it was revealed that the light output of the LEDs proportionally increases with increasing pattern diameter, suggesting that the area of the side surface for patterns could affect the increase in the light intensity of the LEDs.

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