Sensors and Materials, Vol. 27, No. 1 (2015) 97–105
MYU Tokyo

S & M 1050

Linear-Logarithmic Wide-Dynamic-Range Active Pixel Sensor with Negative Feedback Structure Using Gate/Body-Tied Photodetector with an Overlapping Control Gate

Sung-Hyun Jo, Myunghan Bae, Byoung-Soo Choi, Sang-Ho Seo[1], Pyung Choi and Jang-Kyoo Shin*

School of Electronics Engineering, Kyungpook National University,
80 Daehak-ro, Buk-gu, Daegu 702-701, Korea
[1]Samsung Display, #465, Beonyeong-ro, Seobuk-gu, Cheonan,
Chungcheongnam-Do 331-710, Korea

(Received July 18, 2014; accepted December 8, 2014)

Key words: wide dynamic range, high-sensitivity, photodetector, control gate, active pixel sensor

In this paper, we present a linear-logarithmic wide-dynamic-range complementary metal oxide semiconductor (CMOS) active pixel sensor (APS) that uses a gate/body-tied (GBT) photodetector (PD) with an overlapping control gate. The amplifying photocurrent of the PD is 100-fold larger than that of a conventional n+/p-sub PD. Although the GBT PD with an overlapping control gate has high sensitivity, it is difficult to apply this PD to the structure of an APS owing to its very narrow dynamic range. Therefore, we proposed a novel APS using an output voltage feedback structure that makes it possible to extend the dynamic range to 101 dB while maintaining high sensitivity under low illumination (below 20 lx). The proposed APS was fabricated using a 0.35-μm, 2-poly 4-metal standard CMOS process, and its characteristics were evaluated.

1. Introduction

Complementary metal oxide semiconductor (CMOS) image sensors (CISs) are increasingly being developed as wide-dynamic-range detection systems for applications such as fluorescence imaging and biomedical and chemical experiments.[1–3] Many photodetector (PD) elements are available in a CMOS, including n+/p-well, p+/n-well, and n-well/p-sub junctions, which are used for imaging applications.[1,4] These

*Corresponding author: e-mail: jkshin@ee.knu.ac.kr

PDs cannot be applied to low-light-level detection imaging systems because of their reduced photodetection area and decreased supply voltage.[5] The avalanche photodiode (APD) is an alternative device that can simultaneously achieve high responsivity and high speed by operating APDs as single-photon counters.[6–8] However, the avalanche charge multiplication requires higher operational voltages. The higher bias voltages of APDs are not compatible with the peripheral circuits in standard CMOS technology. To improve the responsivity of PDs, phototransistors from a standard CMOS process have been applied to PDs and active pixel sensors (APSs). In contrast to APDs, the phototransistors can operate at low supply voltages, thereby offering a higher gain in photocurrent. The general phototransistor is a hybrid device composed of a metal-oxide-semiconductor field-effect transistor (MOSFET), a lateral bipolar junction transistor (BJT), and a vertical BJT. Some phototransistors achieve photocurrent gains of 7500 to 50000, but their responsivity drops when the photobiasing voltages are below 0.4 V.[9,10]

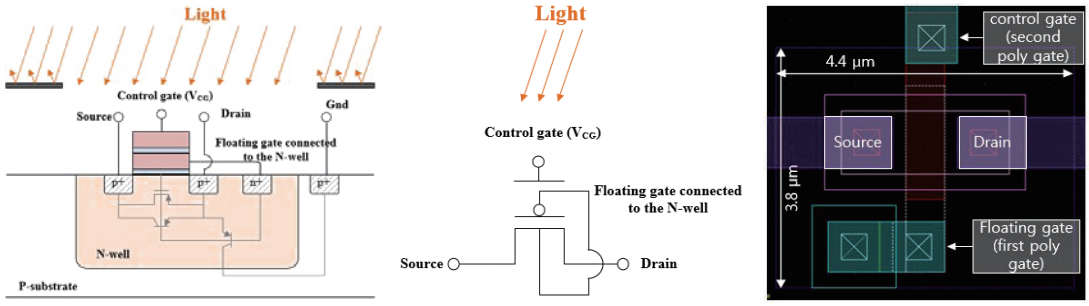
For an APS, sensitivity and dynamic range are trade-off factors. Various approaches have been proposed to attain high sensitivity and a wide dynamic range.[11–16] Multiple sampling techniques provide a wide dynamic range without requiring pixel modification.[17–20] However, a conventional multiple-sampling method requires additional frame memories and an image synthesis process. Logarithmic sensors may considerably widen the dynamic range of the APS in the high-illumination range by compressing the image signal. However, conventional logarithmic sensors operating in the subthreshold region suffer from low sensitivity at low light intensities. The quality of the resulting output image of the logarithmic sensor is degraded because of mismatches between the individual pixels in each sensor. A linear-logarithmic sensor is constructed in real time without the use of a frame memory. Although this sensor's dynamic range is in excess of 120 dB, the sensor addresses the problems of high pixel pattern noise (FPN) and slow response time in the logarithmic mode.[21]

In this work, we proposed a linear-logarithmic wide-dynamic-range APS using a gate/body-tied (GBT) PD with an overlapping control gate. Applying imaging applications to the previously developed GBT APS is difficult because of its very narrow dynamic range resulting from its high sensitivity.[22] Therefore, we proposed a novel APS using an output voltage feedback structure that makes it possible to extend the dynamic range significantly while maintaining high sensitivity under low illumination. The proposed APS was fabricated using a 2-poly 4-metal 0.35-μm standard CMOS process, and its optical responses were measured.

2. Operational Principle of the Proposed APS

2.1 *GBT PD with overlapping control gate*

Figure 1 shows the symbol, cross section, and layout of the GBT PD with an overlapping control gate. The idea of this device comes from the GBT silicon-on-insulator (SOI) n-channel MOSFET (NMOSFET) photosensor.[23,24] Figure 2 shows the light response characteristics of the GBT PD with an overlapping control gate. The GBT PD consists of a MOSFET and lateral and vertical BJTs. Unlike the p-channel MOSFET (PMOSFET)-type phototransistor, the n-well body is connected to a floating gate. When



(a) (b) (c)

Fig. 1. (Color online) High-sensitivity GBT PD with an overlapping control gate: (a) cross section, (b) symbol, and (c) layout.

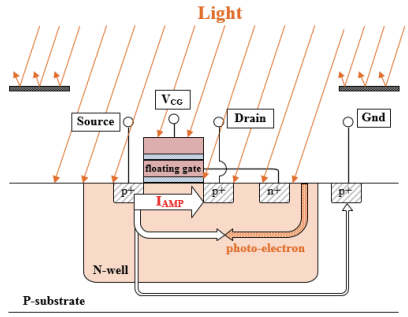


Fig. 2. (Color online) Light response characteristics of the GBT PD with an overlapping control gate.

the device is illuminated, the incident light generates electron–hole pairs (EHPs) in the p+/n-well and n-well/p-sub junctions. The holes move toward the minimum potential in the channel and ground, while electrons accumulate in the n-well region. Therefore, the threshold voltage of the phototransistor is reduced, and the photocurrent is amplified. The modulation of the threshold voltage of the GBT PMOSFET can be explained using the following expression:[25,26]

$$V_{TH} = V_{TH0} - \gamma \left(\sqrt{|-2\Phi_F|} - \sqrt{|-2\Phi_F + V_{BS}|} \right) \quad (1)$$

where V_{TH0} is the threshold voltage at zero body bias, γ is the body effect coefficient, $2\Phi_F$ is the surface potential at strong inversion, and V_{BS} is the body-source voltage. The body effect coefficient in eq. (1) has a minus sign because of the forward-biased body-source junction.[27] Figure 3 shows the energy band diagrams of the GBT PD with the overlapping control gate according to the V_{CG} bias. The control gate can vary the energy barrier for the holes by changing the electric field of V_{CG}. When the bias of V_{CG} is 0 V,

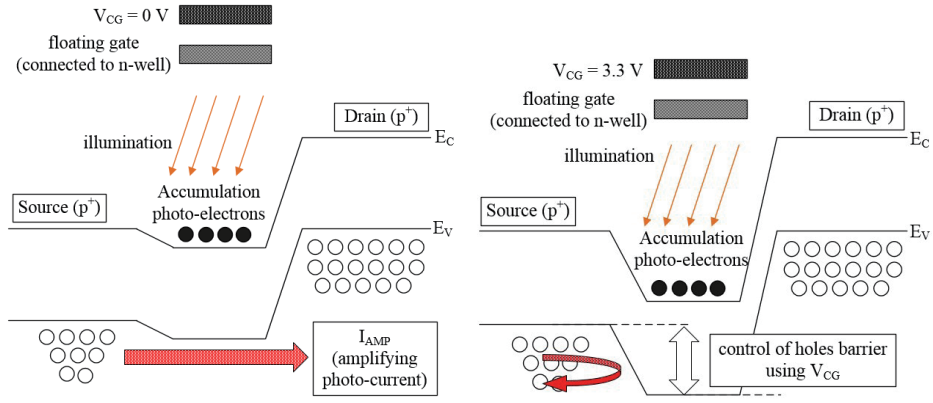


Fig. 3. (Color online) Energy band diagrams of the GBT PD with overlapping control gate according to the V_{CG} bias: (a) V_{CG} = 0 V and (b) V_{CG} = 3.3 V.

the energy barrier is lower under the floating gate, so that the amplifying photocurrent (I_{AMP}) flows from source to drain, as shown in Fig. 3(a). On the other hand, when the bias of V_{CG} is 3.3 V, the energy barrier is higher under the floating gate, and the holes cannot flow from source to drain, as shown in Fig. 3(b). Reference 22 provides more details of our experimental procedures.

2.2 *Output voltage feedback APS*

Figures 4(a) and 4(b) show the schematic of the proposed APS with output voltage feedback structure and its timing diagram, respectively. The proposed APS is similar to a conventional APS. The operation mode of the proposed APS is changed by varying the high-level voltage of the reset (V_{RST_HV}). Figure 5 shows the detailed operating principle of the proposed APS. Since the output node is connected to the gate of M1, the proposed APS requires a negative reset voltage (V_{RST} = −1.5 V) for its reset operation, as shown in Fig. 5(a). After the reset period, the high-level voltage of the reset (V_{RST}) is fixed from 0 to 0.6 V to extend the dynamic range. When a light beam is incident on the n-well region, EHPs are created and separated by the built-in potential of the channel. This is caused by the work function difference and the n-well/P-substrate junction diode. The holes are attracted to the channel and drift to the p+ drain. The electrons are accumulated in the n-well region, which decreases the potential of the floating gate because of the n-well/floating gate connection. Then, the amplifying photocurrent (I_{AMP}) of the GBT PD flows from V_{DD} to V_{FD}, and the output voltage of the proposed APS is increased, as shown in Fig. 5(b). At that time, the feedback transistor M1 is operated in the subthreshold region, and the output voltage of the proposed APS is increased linearly until $V_{OUT} - V_{RST\_HV*} = V_{threshold(M1)}$. After a certain charge accumulation period, M1 is gradually turned on because of the increased output voltage that is connected to the gate of M1 ($V_{OUT} - V_{RST\_HV} \geq V_{threshold(M1)}$). During that time, the amplifying photocurrent (I_{AMP}) of the GBT PD flows

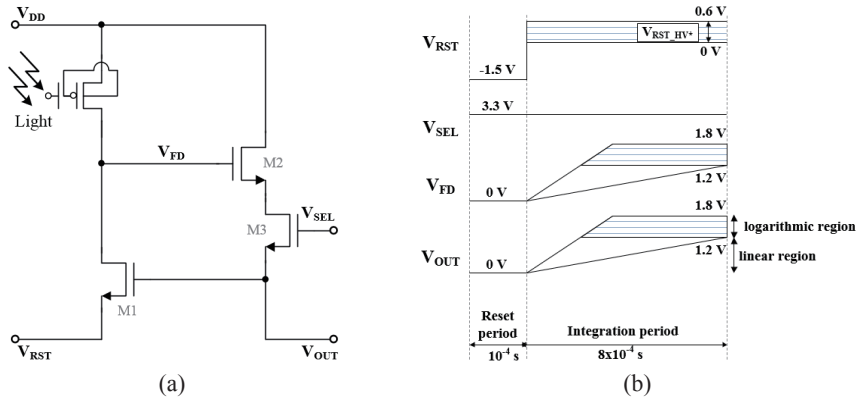


Fig. 4. (Color online) Proposed APS: (a) pixel schematic and (b) operational timing diagram.

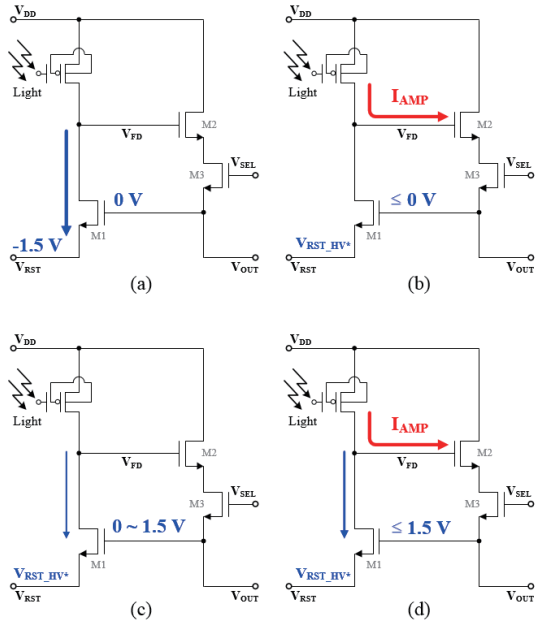


Fig. 5. (Color online) Operational sequence of the proposed APS: (a) reset state, (b) integration state, and (c) and (d) feedback state.

to the source of M1, as shown in Fig. 5(c). As the incident light intensity increases, the gate voltage of M1 that is connected to the output voltage is further increased. For this reason, the output voltage is not saturated because more electrons are induced in the channel and the drain current in M1 is increased, as shown in Fig. 5(d). This effect prevents the output voltage from saturating, and thus increases the dynamic range of the APS.

3. Results and Discussion

Figure 6 shows the variation in the drain current of the GBT PD with the overlapping control gate, according to the source-to-drain voltage (V_{SD}) as a function of control gate bias (V_{CG}). The light source was a He–Ne laser (wavelength: 632.8 nm) with 5 mW of optical power. The GBT PD with the overlapping control gate was fabricated by a 0.35-μm standard CMOS process. The control gate is capable of controlling the amount of photocurrent of the GBT PD, as shown in Fig. 6. The GBT PD with an overlapping control gate is similar to a field-aided lateral PNP phototransistor. Most lateral PNP phototransistors fabricated using a CMOS process use the poly-silicon gate to define the separation between the emitter and the collector, and to force the carriers to flow below the surface. In addition, the gate bias can control the surface inversion under the gate for the MOSFET function. This is called the field-aided lateral BJT. Unlike MOSFETs, PNP phototransistors do not have significant gate-to-body capacitance, and require a transient current to deposit a sufficient charge at the gate to create a conductive channel from drain to source. However, the parasitic vertical PNP substrate transistor is formed by a p+ emitter, nwell base, and p-type substrate. This vertical PNP transistor reduces the collector current efficiency by 30 to 40%.[28] However, this reduction is not an issue, because the collector is connected to the substrate in a common-collector configuration.

Figure 7 shows the variation in the output voltage of the proposed APS with light intensity as a function of V_{REF_HV} when the integration time is 0.8 ms: (a) semi-log graph and (b) log-log graph. The proposed APS has a gate-controlled resistor (M1) to extend the dynamic range of the proposed APS. If the gate voltage, which is connected to the output node, exceeds the threshold voltage of M1 in an n-channel device, the electrons are induced in the underlying gate of M1. Since this channel is connected to the integration node (V_{FD}) and reset voltage node (V_{RST}), the structure looks electrically

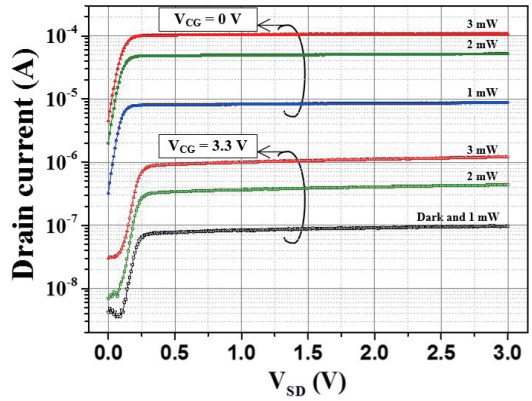
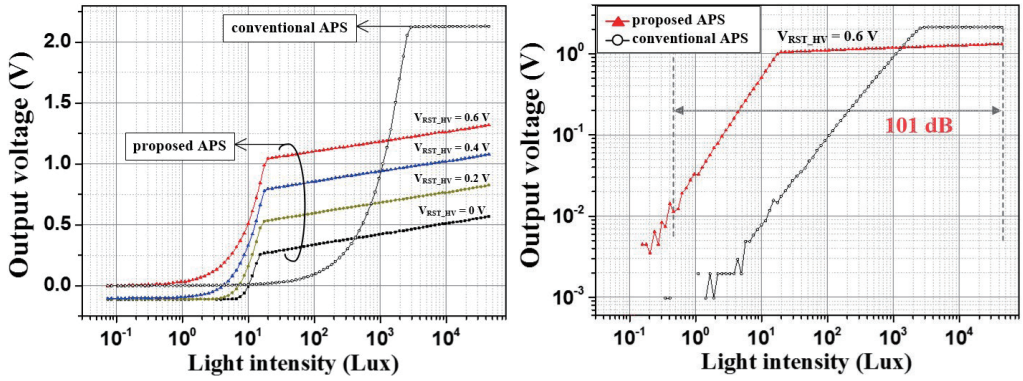


Fig. 6. (Color online) Variation in the drain current of the GBT PD with overlapping control gate according to source-to-drain voltage (V_{SD}) as a function of control gate bias (V_{CG}).



(a) (b)

Fig. 7. (Color online) Variation in the output voltage of the proposed APS with light intensity as a function of V_{REF_HV} when integration time is 0.8 ms: (a) semi-log graph and (b) log-log graph.

similar to an induced n-type resistor. As the gate voltage of M1, which is connected to the output node (V_{OUT}), increases when the light intensity is increased, more electrons are induced in the channel, and the channel's conductance increases. The feedback current of M1 is gradually increased as the illumination level is increased, as shown in Fig. 5(d). For this reason, the dynamic range of the proposed APS is significantly extended to 101 dB, as shown in Fig. 7(b). The proposed APS can improve its sensitivity under low illumination (below 20 lx), and also extend the dynamic range according to its feedback structure. Compared with previously reported wide-dynamic-range methods, the proposed method is simple and powerful. However, the feedback structure of the proposed APS is optimized for only one pixel. In order to apply an image sensor array, this reset gate connection is shifted to the source of M2. This modified structure is capable of applying an image sensor array.

4. Conclusions

In this paper, we have presented a linear-logarithmic 101-dB-dynamic-range CMOS APS using a GBT PD with an overlapping control gate and a feedback structure. The amplifying photocurrent of the GBT PD is 100-fold larger than that of a conventional N+/P-sub PD, and the feedback structure of the proposed APS has a gate-controlled resistor for enhancing the dynamic range. Therefore, the proposed APS has not only high sensitivity under low illumination (below 20 lx) owing to the GBT PD, but also has low sensitivity under high illumination owing to its feedback structure. Compared with previously reported wide-dynamic-range methods, the proposed method is simple and powerful. Therefore, the proposed APS is expected to be useful for wide-dynamic-range applications.

Acknowledgements

This work was supported by the Center for Integrated Smart Sensors, funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2011-0031868), the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIP) (No. 2012-0062617), the BK21 Plus project funded by the Ministry of Education, Korea (21A20131600011), and the Integrated Circuit Design Education Center (IDEC) in Korea.

References

1 J. Ota, T. Tokuda, K. Kagawa, M. Nunoshita and S. Shiosaka: IEEE Proc. of Symposium Circuit and Systems (IEEE, Kobe, 2005) 3487.
2 N. Nelson, D. Sander, M. Dandin, S. Prakash, A. Sarje and P. Abshire: IEEE Trans. Biomed. Circuits Syst. **3** (2009) 99.
3 Y.-W. Chang, Y.-T. Tai, Y.-T. Huang and Y.-S. Yang: IEEE Journal of Sensors **9** (2009) 673.
4 Y. Ardeshirpour, M. J. Deen and S. Shirani: Journal of Vacuum Science & Technology A **24** (2006) 860.
5 H.-S. Wong: IEEE Transactions on Electron Devices **43** (1996) 2131.
6 Y. Maruyama and E. Charbon: 16th International Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS) (IEEE, Beijing, 2011) pp. 1180–1183.
7 M. M. El-Desouki, M. J. Deen, Q. Y. Fang, L. W. C. Liu, F. Tse and D. Armstrong: J. Sens. **9** (2009) 430.
8 N. Faramarzpour, M. J. Deen, S. Shirani and Q. Fang: IEEE Transactions on Electron Devices **55** (2008) 760.
9 Y.-W. Chang and Y.-T. Huang: IEEE Photonics Technology Letters **21** (2009) 899.
10 Y.-J. Kook, J.-H. Cheon, J.-H. Lee and Y.-J. Park: IEEE Transactions on Electron Devices **50** (2003) 2189.
11 S.H. Seo, K. D. Kim, M. W. Seo, J. S. Kong, J. K. Shin and P. Choi: Sens. Mater. **19** (2007) 435.
12 J. H. Park, S. H. Seo, I. S. Wang, J. K. Shin and P. Choi: Sens. Mater. **15** (2003) 361.
13 H.Y. Hyun, J. S. Kong and J. K. Shin: Sens. Mater. **20** (2008) 381.
14 D. Park, Jehyuk Rhee and Youngjoong Joo: IEEE Electron Device Letters **28** (2007) 890.
15 Noriko Ide, Woonghee Lee, Nana Akahane and Shigetoshi Sugawa: IEEE Journal of Solid-State Circuits **43** (2008) 1577.
16 H. Kim, E. Chang, G. Hong, G. Han and J. Choi: Electronics Letters **47** (2011) 1277.
17 D. Park, J. Rhee and Y. Joo: IEEE Sensors Journal **7** (2007) 897.
18 Lisa G. McIlrath: IEEE Journal of Solid-State Circuits **35** (2001) 846.
19 W. Lee, N. Akahane, S. Adachi, K. Mizobuchi and S. Sugawa: IEEE Transactions on Electron Devices **56** (2009) 2436.
20 J. H. Park, S. Kawahito and Y. Wakamori: Institute of Electronics, Information and Communication Engineers (IEICE) Electronics Express **2** (2005) 482.
21 Spyros Kavadias, Bart Dierickx, Danny Scheffer, Andre Alaerts, Dirk Uwaerts and Jan Bogaerts: IEEE Journal of Solid-State Circuits **35** (2000) 1146.
22 Joontaek Jung, Sung-Hyun Jo, Sang-Ho Seo1, Myunghan Bae and Jang-Kyoo Shin: Jpn. J. Appl. Phys. **51** (2012) 02BG06.
23 Hideaki Yamamoto, Kenji Taniguchi and Chihiro Hamaguchi: Jpn. J. Appl. Phys. **35** (1996) 1382.

24 W. Zhang, M. Chan, S. Fung and Ping K. Ko: IEEE Electron Device Letters **19** (1998) 435.
25 F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko and C. Hu: IEEE Transactions on Electron Devices **44** (1997) 414.
26 J. Rabaey: Digital Integrated Circuits: A Design Perspective (Prentice Hall, Upper Saddle River, N. J, 1996).
27 Mohamed Elgebaly and Manoj Sachdev: Proc. of International Conference on Microelectronics (IEEE, 2001) pp. 75–78.
28 E. A. Vittoz: IEEE Journal of Solid-State Circuits **18** (1983) 273.