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A High-Resolution All-Digital Temperature Sensor with Process Variation Compensation

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In this paper, we propose a high-resolution all-digital complementary metal–oxide semiconductor (CMOS) temperature sensor with a ring oscillator for temperature sensing and power supply immunity, a time amplifier for process variation compensation, and serial digital output for low area consumption. Because of the linearity of its high output cycle–temperature, the sensor has excellent measurement accuracy; the architecture of the sensor effectively decreased power supply sensitivity, and the parallel-to-serial converter considerably reduced area consumption. In addition, the high resolution is determined by the time amplifier with external digital codes. The determination of resolution using the time amplifier and the process variation compensation were accomplished simultaneously. The temperature sensor was fabricated using 0.18-μm standard CMOS technology, and the core circuit occupies an area of 0.001 mm^2. The experimental results indicated that the energy per conversion rate was only 10 nJ at a supply voltage of 1.8 V; the conversion rate was 15–30 k samples/s, and the error in temperature sensing ranged from −1.58 to +1.6 °C with a resolution higher than 0.1 °C after one-point calibration in the −40 to +130 °C range. With these advantages, the temperature sensor is suitable for application in large integrated circuit (IC) systems and three-dimensional ICs.

1. Introduction

With technological advances, the number of circuits on a chip has increased. However, considerable heat is generated when more circuits function. Leaving this problem unsolved may cause many other problems that can affect the circuit. Moreover, the circuits may be destroyed, which is a major concern. Therefore, several major methods have been reported for implementing temperature sensors. The main design criteria include sensing range, resolution, sample rate, power supply sensitivity (PSS), area consumption, and process variation.

Temperature sensors are mainly implemented using two methods: analog[1] and digital.[2–9] Compared with analog sensors, digital sensors offer advantages of higher system integration and lower area consumption. However, process variation affects the measurement accuracy. Several methods have been proposed to overcome this problem.[3–6] One method calibrates the sensing elements directly, whereas another method changes the time domain to reduce the effect of process

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variation.[3,5,6] The second method is superior, because process variation compensation technology is integrated to the primary circuit and offers the advantages of low power and area consumption.

In this study, the proposed temperature sensor was based on a ring oscillator for low PSS; a time amplifier was used to achieve process variation compensation, and a parallel-to-serial converter was adopted to reduce the chip area. This paper is organized as follows. Section 2 describes the proposed temperature sensor, § 3 presents the experimental results, and § 4 contains the conclusions.

2. Proposed Temperature Sensor

2.1 Proposed architecture and operation principle

The architecture of the proposed temperature sensor is illustrated in Fig. 1. It consists of a temperature sensor, a control unit, a time-to-digital converter, a calibration unit, and a parallel-to-serial converter. The temperature sensor uses the ring oscillator structure for sensing temperature. The control unit consists of a variable time amplifier (VTA) for process variation compensation and a digital control circuit (DCC), which produces three control signals to control the register, counter, and parallel-to-serial converter. The time-to-digital converter generates a group of digital codes related to temperature. These codes are calibrated using a calibration unit to reduce the temperature measurement error. The parallel-to-serial converter not only changes the form of the digital output but also reduces the chip area. The timing diagram of the proposed temperature sensor is shown in Fig. 2. First, the ring oscillator provides the output cycle, which is linear with temperature. Next, the output cycle result is applied to the VTA in the control unit. The time amplifier generates a pulse width (T_A) with external 9-bit compensation digital codes. The pulse width T_A is converted to three types of control signals: S_{REG}, S_{RST}, and S_{PTS}. After this operation, the time-to-digital converter outputs digital codes, D_{TDC}, which are calibrated using external digital codes. Finally, the final digital codes, which are in a clock form, are exported using the parallel-to-serial converter.

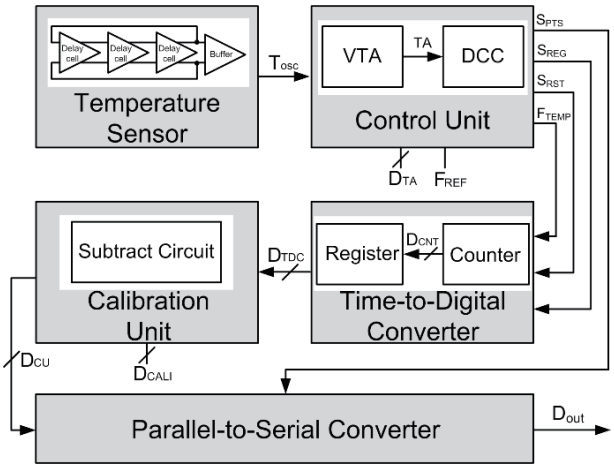

Fig. 1. Architecture of proposed temperature sensor.

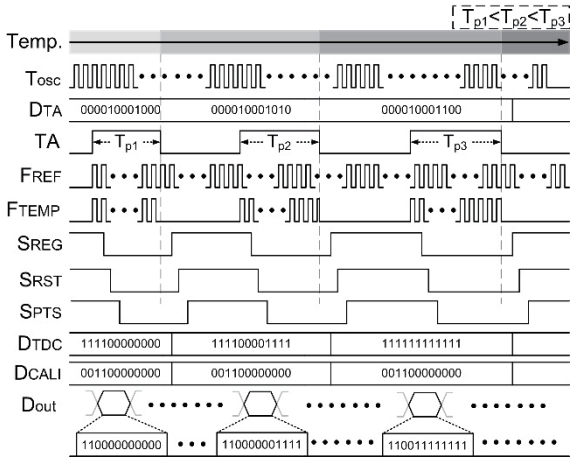

Fig. 2. Timing diagram of the proposed temperature sensor.

2.2 Temperature sensor

Figure 3 depicts the temperature-sensing element in the proposed temperature sensor, which is constructed using a three-stage differential ring oscillator. Its output cycle is linear with temperature and the operating principle is as follows.

When V_{in}^{+} is logic 1 and V_{in}^{-} is logic 0, the PMOS transistors M1 and M2 turn on and off, respectively. Similarly, when V_{out}^{+} is pulled up to logic 1 and V_{out}^{-} is pulled down to logic 0, the NMOS transistors M4 and M3 turn on and off, respectively. In this situation, the circuit is stable until the signals V_{in}^{+} and V_{in}^{-} are changed. In addition, the differential delay cell replaces the conventional single delay cell to reduce PSS. Moreover, the NMOS transistors M5 and M6 are used as resistors, which offer power supply immunity and compensation of temperature linearity.

2.3 Control unit

The control unit comprises VTA and DCC, as shown in Fig. 4. The temperature resolution is set using the VTA, and process variation compensation is conducted simultaneously. The output of the temperature sensor, T_{osc}, is enlarged using the VTA using 9-bit digital codes D_{TA}. The digital codes of the up-counter, D_{CNT}, and the compensation codes D_{TA} are then compared using the comparator, and the pulse width T_{COM} is generated. Subsequently, T_{COM} and a constant signal, START, which is always logic 1, are operated using the XOR logic gate. Finally, the pulse width T_A, which is greater than the signal T_{OSC}, is generated according to process variations and the resolution of the temperature.

The DCC in the control unit comprises several delay cells to generate three control signals, S_{REG}, S_{RST}, and S_{PTS}, which are based on the signal T_A, to control the counter and register of the time-to-digital converter and the parallel-to-serial converter individually. Moreover, the signal T_A and the reference F_{REF} are operated using an AND logic gate to generate the signal F_{TEMP} associated with temperature.

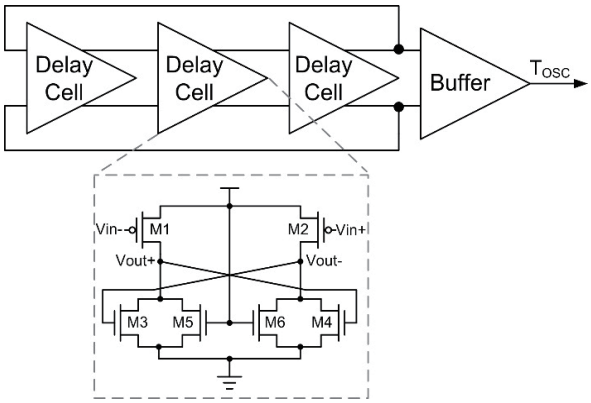

Fig. 3. Architecture of the temperature sensor.

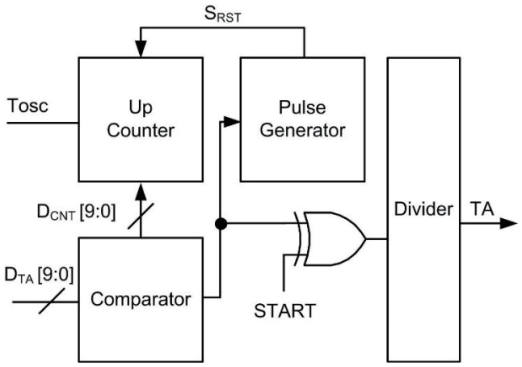

Fig. 4. Architecture of the VTA.

2.4 Time-to-digital converter

The proposed time-to-digital converter consists of a 12-bit counter and register, as shown in Fig. 1. The counter is triggered by F_{TEMP}, and the 12-bit digital codes, D_{CNT}, related to temperature are then produced. Next, the digital codes, D_{CNT}, are entered in the 12-bit register. In addition, S_{REG} and S_{RST} control the register and counter to ensure correct circuit operation. Eventually, the time-to-digital converter provided a group of digital codes, D_{TDC}, related to temperature.

2.5 Calibration unit

Figure 5 shows the architecture of the proposed calibration unit. It mainly comprises 12-stage subtract circuits. The digital codes D_{TDC} and external calibration codes D_{CALI} are operated in this circuit, and the output digital codes D_{CU} are obtained after calibration. The digital codes D_{CALI} are provided according to the optimal reference point for reducing the temperature error. For example, assume that −40 °C is the reference point and that the digital codes D_{TDC} are set to $(010100101111)_2$, represented as $(1327)_{10}$. Thus, the digital codes D_{CALI} are set to $(010100101111)_2$. Subsequently, the digital codes D_{TDC} and D_{CALI} are operated using a 12-bit full subtractor. Finally, the output digital codes D_{CU} are shifted to $(000000000000)_2$.

2.6 Parallel-to-serial converter

To reduce the chip area, a parallel-to-serial converter is designed in the proposed temperature sensor. Figure 6 shows the architecture of the parallel-to-serial converter, which primarily comprises 12-stage parallel-to-serial cells. A single stage of a parallel-to-serial cell comprises three NAND logic gates and one D flip-flop, which is controlled by two signals, namely, write and shift, which are obtained from the signal S_{PTS} of the control unit. When the parallel digital codes D_{CU} are supplied to the parallel-to-serial converter to shift bit by bit, a serial output signal D_{OUT} is generated.

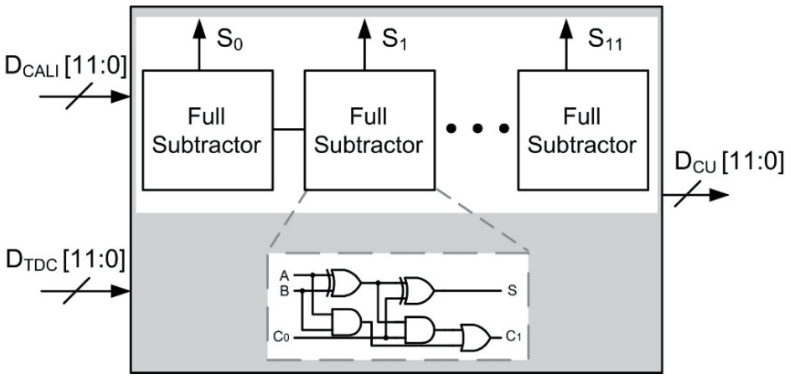

Fig. 5. Architecture of the calibration unit.

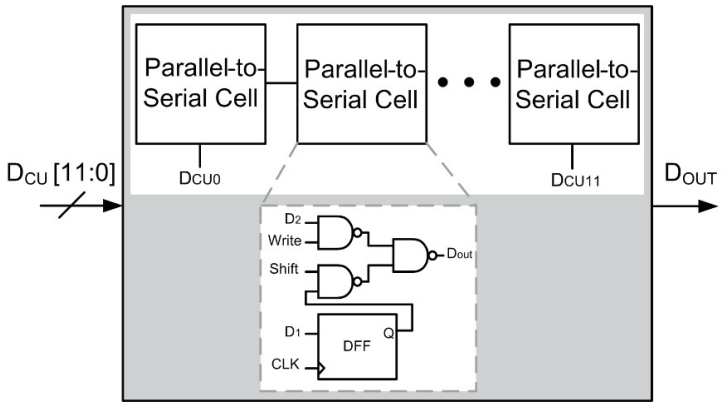

Fig. 6. Architecture of the parallel-to-serial converter.

3. Experimental Results

The proposed temperature sensor was fabricated using a 0.18-μm standard complementary metal–oxide semiconductor (CMOS) process, and the temperature-sensing element occupied an area of 0.001 mm^2. Figure 7 shows the die micrograph of the temperature sensor. Figure 8 shows the simulation results of the T_{OSC} signal vs the temperature, which ranged from −40 to 130 °C in 10 °C increments, and a ±10% power supply variation (1.62, 1.80, and 1.98 V) at the TT corner. In addition, the linearity of the output cycle offers a Pearson correlation coefficient of 0.9999, and the maximum PSS is only 5.16%, which can be expressed using the following equations

$$R^2 = \frac{\sum_i^n (x_i - \bar{x})(y_i - \bar{y})}{\sqrt{\left|[\sum_{i=1}^n (x_i - \bar{x})^2][\sum_{i=1}^n (y_i - \bar{y})^2]\right|}}, \quad (1)$$

where x is the temperature, $\bar{x}$ is the average of the temperature, y is the output cycle, and $\bar{y}$ is the average of the output cycle, and

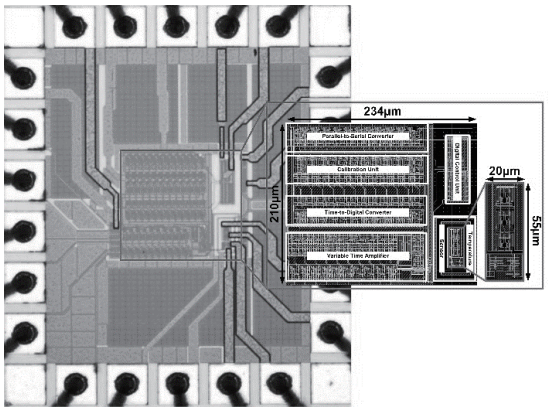

Fig. 7. Chip diagram of the proposed temperature sensor.

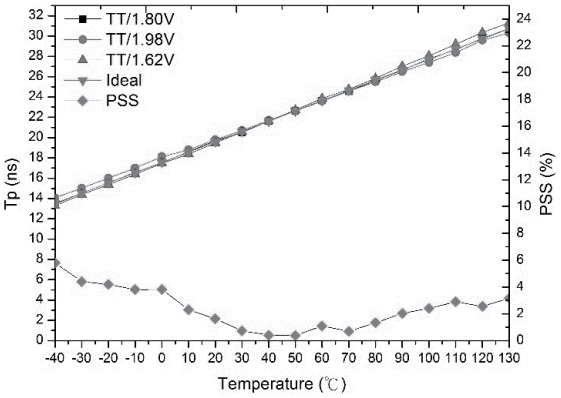

Fig. 8. Relationships at TT1.8, 1.98, and 1.62 V between the temperature and the output cycle of the oscillator.

$$PSS = \frac{Y_{\max} - Y_{\min}}{Y_{1.8V}} \times 100\%, \tag{2}$$

where Y_{max}, Y_{min}, and $Y_{1.8V}$ are the output cycles of +10%, −10%, and 1.8-V power supply, respectively.

The simulation of process variation compensation is as follows. The circuit was simulated under five process corner (TT, FF, SS, SF, and FS) variations at a power of 1.8 V. The output cycle of the ring oscillator was enlarged for process variation compensation by the VTA. In other words, in this method, the slope of the graph of the output cycle versus temperature is adjusted and is expressed using the following equation

$$T_A = (N + 1) \times T_{OSC} \times 2, \tag{3}$$

where T_A and T_{OSC} are the output cycles after and before enlargement, respectively, and N is the enlarged times.

Figures 9(a) and 9(b) show the circuits before and after process variation compensation. According to the simulation results of five process corner variations before compensation, the slopes of the output cycle versus temperature were 0.0914, 0.0908, 0.0914, 0.0882, and 0.0957 ns/°C. The slopes after compensation were adjusted to the same magnitude of 100 ns/°C by enlarging the output cycle. The compensation is carried out as follows. We assume that the magnitude of the temperature change is ΔX and that the corresponding magnitude of the output cycle change is ΔY. When ΔX is changed by a constant magnitude for five process corners, ΔY remains the same. Thus, process variation compensation was accomplished.

Figure 10 shows the simulation and measurement results of the output signals T_{OSC} and D_{OUT} at 25 °C. The simulation and measurement results of T_{OSC} and D_{OUT} were 18.8 ns and $(011111110101)_2$ and 18.78 ns and $(011111110001)_2$, as shown in Figs. 10(a) and 10(b), respectively. A comparison of the simulation and measurement results reveals that the digital codes are almost the same.

The new temperature sensor was compared with temperature sensors reported in several previous studies,[1–3,8] as shown in Table 1. The new temperature sensor provides high sensing range, high resolution, and low area consumption. Furthermore, the new sensor possesses excellent temperature measurement accuracy.

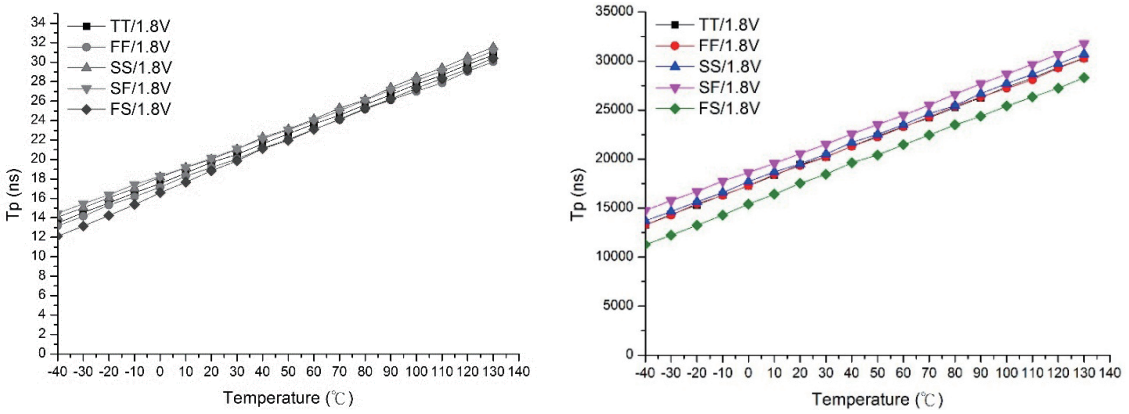

Fig. 9. (Color online) Output cycle of the oscillator (a) before and (b) after enlargement.

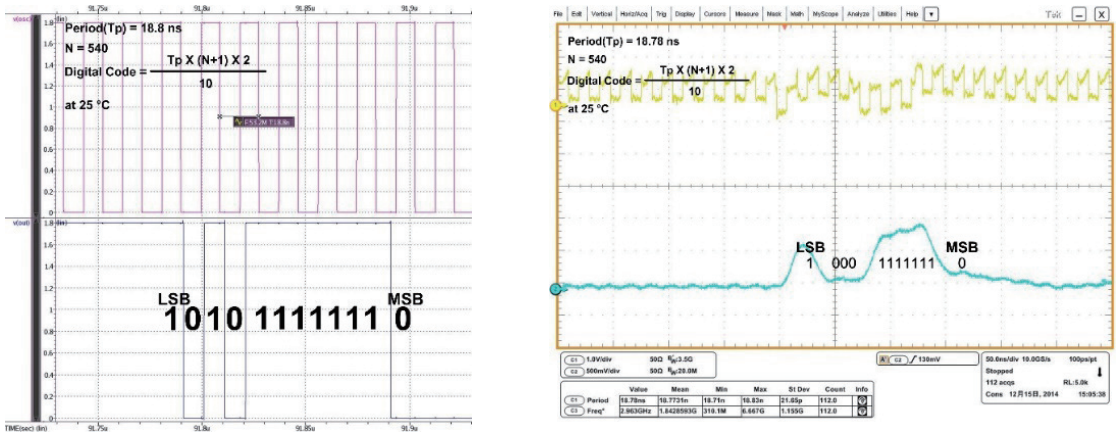

Fig. 10. (Color online) Output digital codes of (a) simulation and (b) measurement.

Table 1
Performance comparison.

Parameter	[1]	[2]	[3]	[8]	This work
Process (nm)	65	180	130	65	180
Range (°C)	0–120	0–100	20–120	−40–110	−40–130
Supply voltage (V)	1	0.5	1.2	1.2	1.8
Resolution (°C)	0.3	0.3	0.595	0.34	<0.1
Sample rate (k/s)	200	0.5	430	366	15–30
Accuracy (°C)	−3–3	−1.8–1.2	−0.63–1.04	−2.8–2.9	−1.58–1.6
Power (W)	39 μ	47 n	N/A	400 μ	150 μ
Energy/sample (nJ)	0.2	N/A	0.67	1.09	10
Area (mm^2)	0.01	N/A	0.031	0.0013	0.001* 0.049#

*for sensor only, #for system.

4. Conclusions

A ring oscillator was used as a temperature-sensing element, and the architecture of the proposed oscillator was provided with power supply immunity. Moreover, process variation compensation was implemented in the new temperature sensor with the VTA of the control unit. The temperature sensor was fabricated using standard 0.18-μm CMOS process, and the temperature-sensing element occupied an area of 0.001 mm^2. When the temperature ranged from −40–130 °C, the temperature sensor yielded a Pearson correlation coefficient of 0.998, a sample rate of 15–30 k, and a resolution exceeding 0.1 °C. High linearity, resolution, and accuracy and low area consumption were achieved with the new temperature sensor.

Acknowledgements

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References

1 N. Testi and Y. Xu: Proc. Int. Symp. Qual. Electron. Design (IEEE, Santa Clara, 2013) pp. 696–702.
2 S. Mohamad, F. Tang, A. Amira, A. Bermak, and M. Benammar: Proc. Asian Symp. Qual. Electron. Design (IEEE, Penang, 2013) pp. 50–54.
3 Y. J. An, K. Ryu, D. H. Jung, S. H. Woo, and S. O. Jung: Proc. Int. Conf. Consum. Electron. (IEEE, Las Vegas, 2013) pp. 572–573.
4 S. Hwang, J. Koo, K. Kim, H. Lee, and C. Kim: Trans. Circuits Syst. I **60** (2013) 2241.
5 P. Chen, S. C. Chen, Y. S. Shen, and Y. J. Peng: Trans. Circuits Syst. I **58** (2013) 913.
6 M. H. Chang, S. Y. Lin, P. C. Wu, O. Zakoretska, C. T. Chuang, K. N. Chen, C. C. Wang, K. H. Chen, C. T. Chiu, H. M. Tong, and W. Hwang: Proc. Int. Symp. Circuits Syst. (IEEE, Beijing, 2013) pp. 133–136.
7 S. X. and W. T. Ng: Proc. Int. Symp. Circuit Syst. (IEEE, Beijing, 2013) pp. 2617–2620.
8 K. Kim, H. Lee, and C. Kim: Trans. Very Large Scale Integration (VLSI) Syst. **21** (2012) 1950.
9 N. Jandhyala, L. He, and M. Jones: Proc. Int. Symp. Qual. Electron. Design (IEEE, San Jose, 2008) pp. 293–296.