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Design and Fabrication of Identification Inkjet Print Head Chip Fuse Sensors

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This paper describes the development of a thermal inkjet print head with an identification circuit. The identification circuit was designed using a fuse and other electronic components. The multifunctionality of the integrated circuit in a print head of the cartridge was used to satisfy user demands. The circuit was encoded to enable identification of general information regarding the ink cartridge, such as its model number, serial number, color settings (color or gray scale), and the best print quality. In addition, the current status of the cartridge, such as whether its life has elapsed, can be identified. The identification circuit was connected in series with the metal oxide semiconductor (MOS) drain fuse after the wafer factory burn break fuse. A V_{ID} of more than 3.6 V indicates a blown fuse. Therefore, the fuse-blow voltage was set to be 3.6 V. At a value of V_{GS} equal to 15.5 V, blown fuse parameter analysis was performed. Linear regression showed that the I_D current was 54.36 mA. X-ray diffraction patterns revealed that the X-rays penetrate the fuse circuit from the top. Therefore, the elemental composition of all layers, from the upper layer SiC/SiN to the Si substrate, was analyzed and determined to be Si, C, N, Ta, Al, P, and O, among others. Because most layers contain Si, the Si peak was the largest. The fuse profile was characterized using scanning electron microscopy. Fuse size and current density were also investigated.

1. Introduction

The use of computers for printing data has increased in recent years, and this has in turn increased the demand for inkjet printers. Print heads of inkjet printers are of two types: permanent and discardable. In permanent print heads, which use a piezoelectric architecture, only the cartridge (and not the entire unit) is replaced when the printer is out of ink. In these print heads, a voltage is applied across the piezoelectric material within the print head, resulting in deformation of the material (i.e., the piezoelectric material changes shape).[1–5] This deformation creates pressure within the cartridge, which causes ink to be extruded onto the paper. In discardable print heads, which are thermal bubble-type print heads, the entire unit is discarded when the cartridge is out of ink.[6–15] The principle used in these print heads is the same as that underlying the formation of water bubbles when water is boiled: during heating,[16–25] when nucleation occurs, a local ink bubble

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is formed and the ink is extruded directly onto the paper. These inkjet printers are less expensive than those with permanent print heads. Therefore, they have many advantages, and their market share exceeds 90%. Each ink cartridge has a unique chip number. This number is printed in the chip circuit, called the identification circuit.

The identification circuit is connected in series with the metal oxide semiconductor (MOS) drain fuse after the wafer factory burn break fuse line. The original ink wafer is not defined, which is advantageous. The wafer must go through the printer system to detect and transmit an identification signal to the ink brake wafer. This study configured the circuit and the defined properties of the materials in the inkjet system. A new circuit architecture was designed after the fuse burn break circuit. This design can be used to identify whether the ink brake system matches the printer's status in addition to detecting ink levels in the cartridge. This design necessitates a driver MOS device and special architecture for the material process fuse element. When the MOS fuse is blown (open circuit), the signal detected is "0"; otherwise, the printer detects and transmits the signal "1" to confirm that it is the same print head and to authenticate the inkjet printer system identification signal.

2. Design and Fabrication

Circuit identification is available for each print head, identifying the circuit design, and the presence of the complementary MOS micro-electromechanical system (CMOS-MEMS) chips can be confirmed. In this study, the identification circuit is in series with one end of the MOS drain fuse after the wafer factory burn break fuse line. When the MOS is blown (open circuit), the signal detected is "0"; otherwise, the printer sends the feedback signal "1" to confirm that it is the same print head. Figure 1 shows integrated fuse and CMOS logic large-scale integration (LSI).

To aid our discussion, we have divided the description of the ink jet print head identification circuit design into two sections: (1) the design of the fuse exterior, and (2) the design that drives the circuit.

Either tantalum aluminum (TaAl) filament or a tantalum aluminum nitride (TaAIN) filament can be used as the fuse element. The fuse heater chip can have a number of heater layers, depending on the application. The multiplexer memory array has a number of CMOS devices, such as diodes, pnp transistors, and npn transistors. The MOS devices are used to isolate each fuse so that the transistor can be used to program or read many different fuses based on the address sent from the printer. Specifically, the number of row programming transistors and the number of column

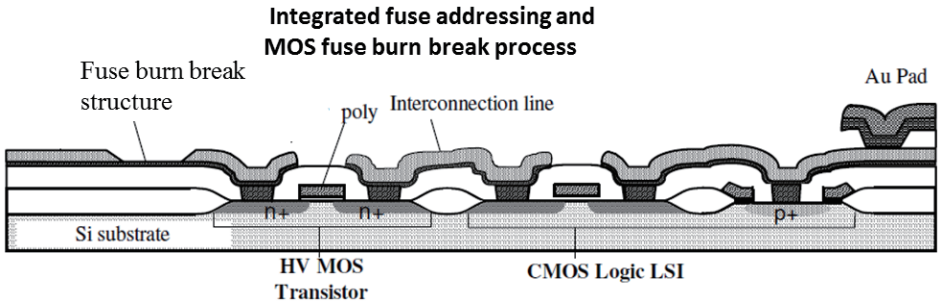

Fig. 1. Integrated fuse and CMOS logic LSI.

programming transistors form an array of memory elements. The multiplexer memory can be programmed by selecting the row power transistor and a corresponding column power transistor. The row and column transistors thus reduce the area covering the fuse and the MOS device. Consequently, either the overall area of the array can be greatly reduced or the number of memory elements can be increased in the same chip area.

3. Integrated Fuse Addressing and MOS Fuse Burn Break

In this section, we describe the driver circuit. The driver circuit identification uses MOS field-effect transistor (MOSFET); each of two polygate MOSs is connected in parallel to each other and shares a pairwise MOS source. They share a common design; the polygate is 3.85 μm wide, the source and drain widths are 6.98 μm, and the contact hole is 3.04 μm in diameter.

The latch data bits circuit system has a series-in/parallel-out architecture. The latch data bits circuit created "A" bits for addressing the jets group. A latch is a system of bistable multivibrators.

Figure 2 shows the serial input and parallel output shift register connections, which convert serial data input into a parallel output format. After several serial data communication requirements to complete the input, it can read out at each parallel data output simultaneously. In this arrangement, each flip-flop is edge-triggered. The first flip-flop works at a given clock frequency. The remaining pre-stage flip-flop has a binary frequency, and the duty cycle is changed twice. Therefore, it takes twice as long for the rising/falling edge to trigger each subsequent flip-flop. This shifts the serial input in the time domain, resulting in parallel output.

Figure 3 shows the shift register circuit system. We designed the new structure using displacement data: bit-by-bit data input. An identification code is required for comparison and authentication of the ink cartridge identity. Another data point that must be identified is the amount of ink used. These information codes are wisdom certification and record.

To prevent electromagnetic and capacitance interference with the fuse heater, we propose an interval N bit elements switch multiplexer circuit system print head, as shown in Fig. 3. Electrical noise in the fuse heater generates specious signals from the fuse heater. The encoding algorithm system belongs to the inkjet system authentication.

The identification integrated circuit of the multiplexer inkjet head is composed of a silicon chip. An nMOS is made from a silicon wafer. A wafer was introduced into the hot furnace tube to

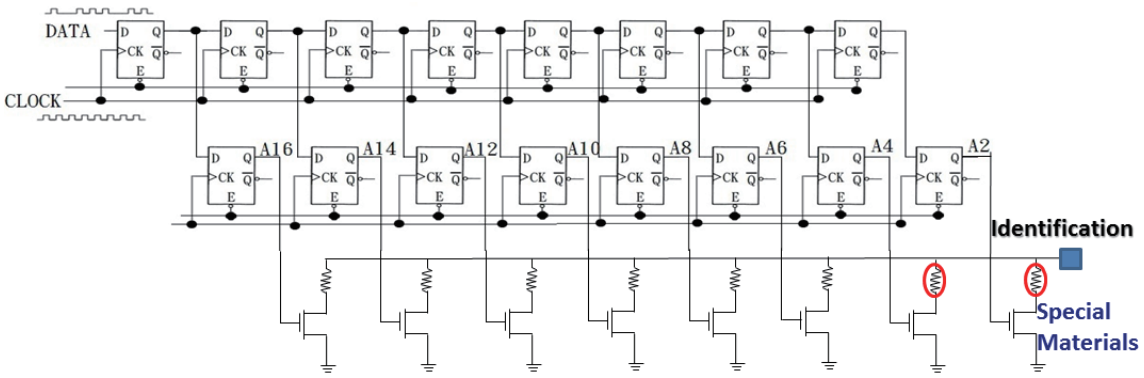

Fig. 2. (Color online) Serial input and parallel output shift register connections.

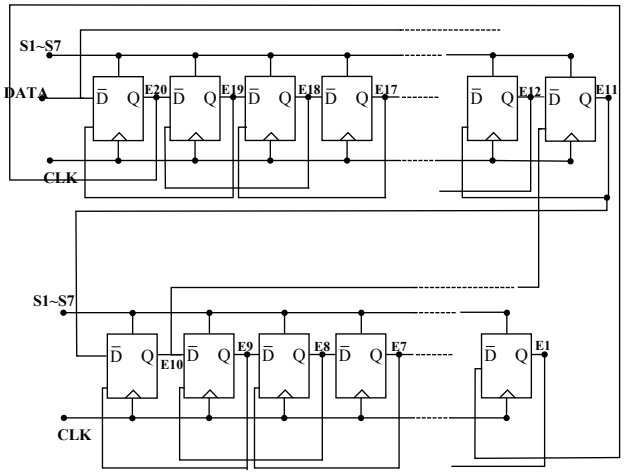

Fig. 3. Shift register circuit system.

form an SiO_2 layer 100 Å thick. The thickness of the Si_3N_4 layer was approximately 4000–5000 Å. A 100-Å SiO_2 layer was deposited by low-pressure chemical vapor deposition. First, the Si_3N_4/SiO_2 layer was defined through photolithography. Local oxidation of silicon (LOCOS) was mainly used as a mask. The mask defined the active area (active region), followed by a LOCOS isolation process. LOCOS is the traditional isolation technique. At first a very thin silicon oxide layer is grown on the wafer, the so-called pad oxide. Then a layer of silicon nitride is deposited which is used as an oxide barrier. The pattern transfer is performed by photolithography. After lithography the pattern is etched into the nitride. In the middle current ion implanter, the entire wafer was implanted with boron atoms (dosage = $10^{13}/cm^3$) from a boron ion source (ion source). After the resist was removed, it was fed into the wafer oxidation furnace tube, where the field oxide layer grew thicker. First, using implanted boron ions and then through high-temperature diffusion, there was a concentration gradient into the silicon substrate. Because one surface of the Si region was covered by Si_3N_4, water molecules and oxygen could not easily pass through; hence, SiO_2 was not formed because of the lack of oxidation. In contrast, the other surface of the Si region was not covered by Si_3N_4, and the consequent oxidation formed a field oxide layer composed of silica. Because of the presence of water molecules and oxygen on the Si_3N_4 region, horizontal diffusion was possible; hence, the layer had a beak-like appearance.

The identification circuit was designed primarily after the completion of all print head manufacturing processes, because the printer must confirm the inkjet chip certification. In this study, the identification circuit was in series with one end of the MOS drain fuse after the wafer factory burn break fuse line. This architecture could be defined by the blown fuse circuit and the detected signal "0". When the fuse was not blown, the printer sent the feedback signal "1" to confirm that it was the same print head. This identification circuit architecture may be used to detect the amount of ink as well as for inkjet chip-based authentication.

Through integrated fuse addressing and the MOS fuse burn break process, the input control circuit can be expanded to two groups, namely, shift registers and a latch system, such that the size of the detection signal is 8 bits. The inkjet chip can certify a total of 2^8 combinations of conditions.

In addition, the layout of the fuse circuit breaking architecture was designed. However, the

drawback of the design was that when the chip circuit detected signals from printer after the completion of fixed designed architecture. This situation only corresponds to a specific printer. The ink detecting circuit mask was designed to detect the amount of ink. It cannot quantify the ink level.

4. Experiments and Results

The MOSFET driver design architecture produced fuse burn break current. The identification circuit is designed with a fuse system and a number selected by a multiplexer. It is necessary that the system supplies enough voltage to make fuse burn break. The operating principle of the fuse burn break system is found in the follow-up statement. The fuse current is designed to be blown. The system must determine the fuse blown-point voltage and current. We restricted the study to a smaller voltage at the V_{ID} end. HP 4155A is an electronic instrument for measuring and analyzing the I–V curve as shown in Fig. 4. A V_{ID} of higher than 3.6 V indicates a blown fuse. Therefore, the fuse-blow voltage was 3.6 V. At a value of V_{GS} equal to 15.5 V, blown fuse parameter analysis can be performed. The threshold voltage value is shown in Fig. 5. A linear regression revealed that the I_D current equals 54.36 mA, as shown in Fig. 6.

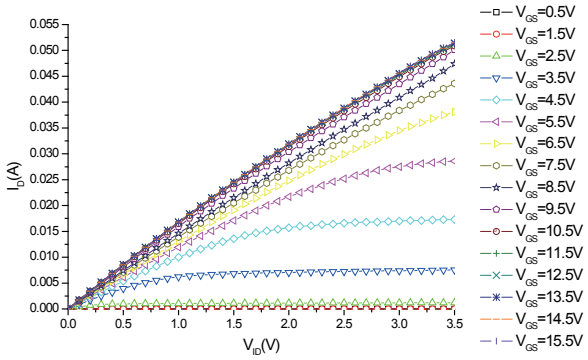

Fig. 4. (Color online) I_D–V_{ID} curve of fuse driver (nMOS).

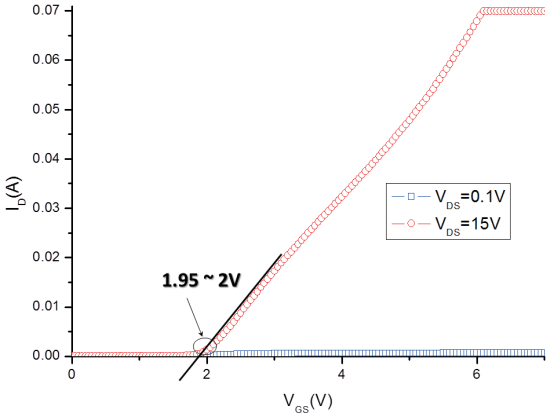

Fig. 5. (Color online) MOS driver threshold voltage.

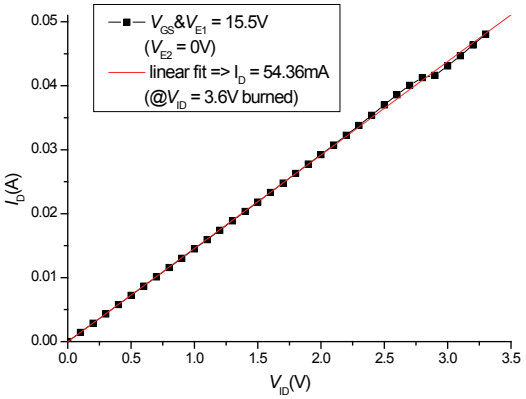

Fig. 6. (Color online) I_D–V_{ID} curve by linear regression I_D current.

We measured the I_D–V_{GS} curve as shown in Fig. 4. To protect the circuit and load heater, we set the current limit to 70 mA. The threshold voltage value was between 1.95 and 2 V. The threshold voltage value should be in the MOS operating range. In particular, it should be in the fuse burn break operations. This is a key element. If this value is too high, the open starting voltage of the MOS element will be high, which is not good for fuse burn break, even the MOS element does not have a larger current. In contrast, if this value is too low, the open starting voltage of MOS element will be too low. Despite this, the MOS element has a larger I_D current. It is a large current through the fuse and then burn break.

To let fuse burn break, the identification MOS driver is designed without field oxide (FOX). A FOX layer is formed on the substrate to define an active region. A gate structure is formed on the active region, where the gate structure has a gate oxide layer, a first gate layer, and a cap layer on the gate layer. The two polygates of each MOS are in parallel. These gates sharing an MOS source have a common design. Thus, in the cross-sectional analysis, the AlCu polyfinger structure was repeated, as shown in Fig. 7. The polygate is 4 μm wide, the source and drain widths are 6.3 μm, and the contact hole diameter is 1.7 μm.

4.1 Fuse profile and current density

The fuse has a funnel-shaped appearance. The relevant dimensions are shown in the label; the narrowest middle part is 4.72 μm, and TaAl is used for the fuse structure.

Figure 8 shows the top view of the identification fuse. Its dimensions are indicated in the figure. The middle part is bare TaAl. The narrow middle part is made of TaAl. The narrowest part is 4.72

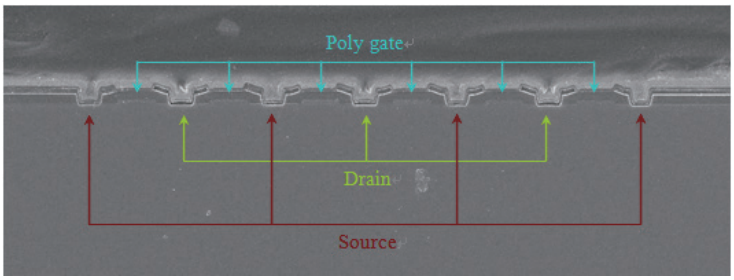

Fig. 7. (Color online) Poly-finger structure of MOS driver.

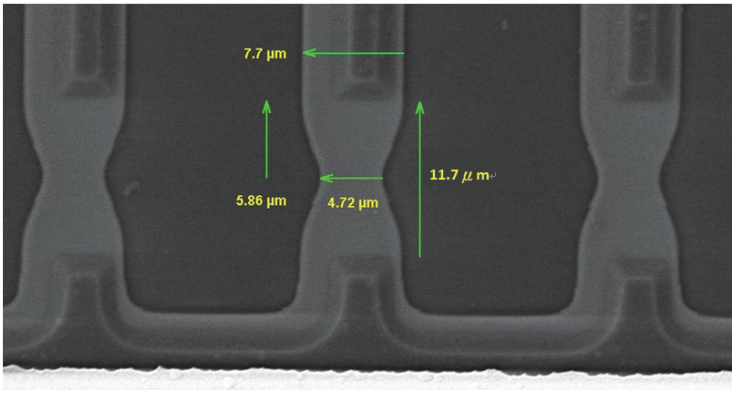

Fig. 8. (Color online) Scanning electron microscopy (SEM) top view of ID fuse.

μm. The supply current for this structure is blown. The sheet resistance value of TaAl is 29 Ω/square.

The impedance value is calculated as follows.

$$\text{Impedance value} = \frac{11.7/2}{(7.7+4.7)/2} \times 29 \times 2 = 54.73\ \Omega \tag{1}$$

$$\text{The area of fuse} = \frac{(7.7+4.7)}{2} \times \left(\frac{11.7}{2}\right) \times 2 = 72.54\ \mu m^2 \tag{2}$$

The current I_D is 54.36 mA. The current density can be calculated as follows.

$$\text{Current density} = \frac{I^2 R_{fuse}}{A_{fuse}} = \frac{(54.36\ \text{mA})^2 \cdot 54.73\ \Omega}{72.54\ \mu m^2} = 2.2294 \times 10^{-3}\ \text{W}/\mu m^2 \tag{3}$$

4.2 SEM cross-section and EDX analysis

Figure 9 is an enlarged view of the fuse. The thickness of each layer is marked in the figure [SiC/SiN layer = 340–360 nm, AlCu layer = 500 nm, TaAl fuse layer = 78–85 nm, phosphosilicate glass (PSG) = 1.05–1.1 μm, and tetraethyl orthosilicate (TEOS) = 135–175 nm]. The difference is that the heater fuse does not directly cover the Ta layer. After the heater helps in bubble growth, it forces a return when the bubbles dissipate. Therefore, a Ta protective layer is formed on top of the heater. Such a framework reduces the strength of the return and prolongs heater life. The main function of this framework is to blow the fuse during the different modes of operation so that the structure does not need to be covered with Ta.

Figure 10 shows the top view during energy dispersive X-ray (EDX) analysis. The X-ray passes from the top down into the fuse circuit. The elemental composition of all layers, from the upper layer SiC/SiN to the Si substrate, was analyzed and determined to be Si, C, N, Ta, Al, P, and O, among others. Because most layers contain Si, the Si peak was the largest.

The fuse circuit was examined by microscopy. It is a large current through the fuse and then burn break. Figure 11 shows the driver circuit and fuse architecture. The principle is to use electric current to flow through the fuse to blow the line architecture. Such a principle can be applied to the model number and serial number and for color identification purposes.

The identification MOS of the gate terminal is connected to the A side, wheras the A side is connected through the output by the multiplexer. Therefore, the operating voltage of the identification MOS gate terminal is 15.5 V. We know the voltage applied to the terminal identification. The instantaneous current flowing through the MOS identification must be analyzed.

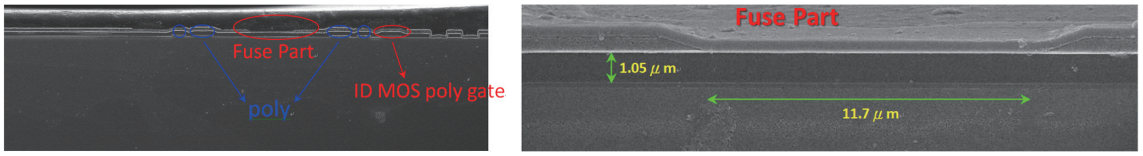

Fig. 9. (Color online) An enlarged view of the fuse.

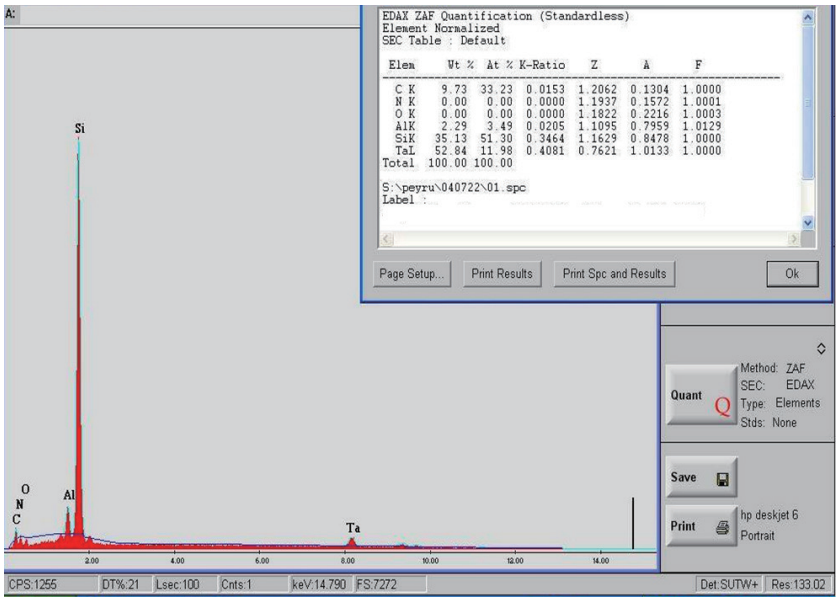

Fig. 10. (Color online) Identification fuse EDX analysis (top view).

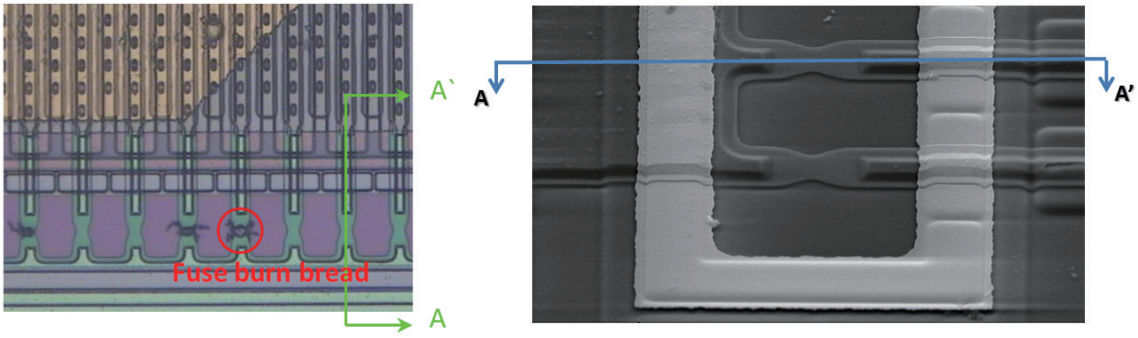

Fig. 11. (Color online) Driver circuit and fuse architecture.

5. Conclusion

In this study, we have successfully designed and demonstrated an inkjet print head chip with identification fuse sensors. When V_{ID} is higher than 3.6 V, the fuse is blown. Therefore, a V_{ID} of higher than 3.6 V indicates a blown fuse. At a value of V_{GS} equal to 15.5 V, blown fuse parameter analysis was performed. A linear regression showed that the I_D current was 54.36 mA. The integration of multifunctional logic has enabled the creation of powerful thermal inkjet products and should increase their market demand in the future.

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