S & M 0132

Layout Design Rules for Microstructure Fabrication Using Commercially Available CMOS Technology

M. Parameswaran and M. Paranjape¹

School of Engineering Science, Simon Fraser University, Burnaby, BC, Canada V5A 1S6

Department of Electrical Engineering, University of Alberta, Edmonton, Alberta, Canada T6G 2G7

Key words: CMOS compatible micromachining, layout design rules

(Received February 19, 1993; accepted May 6, 1993)

In the area of integrated transducer research, micromachining techniques are often employed as a means of implementing certain sensor and/or actuator functions on a single silicon substrate. The possibility of fabricating signal processing or support circuitry along with the transducer microstructure makes this technique suitable for implementing many instrumentation functions. With existing complimentary metal oxide semiconductor (CMOS) processes commercially available, it is possible to incorporate both integrated circuit design and CMOS-compatible micromachining design. In order to acquaint designers with this technology, in this paper we will discuss a set of standard layout design rules and techniques which may be followed in the development of microstructure layout. These design methodologies cover a wide range of possible structures which can be implemented using standard CMOS processes. Experimental structures fabricated using some well-known CMOS processes have been used as a basis to verify these design rules.

1. Introduction

Recently, micromachining has emerged as one of the primary techniques associated with the fabrication of integrated micromechanical structures for sensor and actuator applications. (1,2) The potential for merging CMOS-compatible micromachining with integrated circuit design using a standard process will provide an economical and easy approach to the fabrication of certain micromechanical