

Hydrogen Flame Detector with Bioinspired Optoelectronic Integrated Circuit and Field-Programmable Gate Array Using Integrated Three-Dimensional System Architecture

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We introduce an integration concept between a bioinspired optoelectronic integrated circuit (OEIC) and a field-programmable gate array (FPGA) to realize a single-chip smart ultraviolet (UV) imaging sensor. The bioinspired OEIC stacks the Pt/n-Al_{0.49}Ga_{0.51}N backside-illuminated (BSI) Schottky barrier diode (SBD) photodiode array onto the complementary metal oxide semiconductor (CMOS) edge detection circuits (EDCs). The EDC mimics the outer vertebrate retina that has the purpose of reducing the digital analysis information by extracting the edge from the detected object before being processed by the FPGA, and thus decreasing the power consumption. The binary images produced by the bioinspired OEIC are analyzed in the FPGA using a histogram projection circuit to generate information about the location, size, moving speed, moving direction, and spreading status of the detected object, which is the UV radiation coming from the hydrogen flames. In this study, an EDC chip of 1 × 16 pixels was fabricated and integrated with the FPGA using wires. We evaluated the speed calculation performance of the system with a moving object in the range of 1.7–2,049 pixels/s.

1. Introduction

In Japan, the Hydrogen Society plan has been implemented since 2015 for promoting the usage of hydrogen to reduce fossil fuel dependence as well as greenhouse gas emission.⁽¹⁾ Regarding the safety of hydrogen, the leakage of hydrogen gas during its manufacture, storage, and distribution is a concern. When hydrogen gas is mixed with air, it may self-ignite.⁽²⁾ It is difficult to see the hydrogen flame in daylight since it produces a pale blue color.⁽³⁾ Considering that the hydrogen flame emits a strong ultraviolet-C (UV-C) radiation (200–280 nm), which has a solar-blind property, detecting the hydrogen flame at sea level even in daylight can be realized.^(3,4)

It is necessary to have a continuous monitoring system for the area where the hydrogen is being used. The monitoring system sends an alert when a hydrogen flame occurs and provides the position of the hydrogen flame's source to prevent further damage on that area. Commercial UV-C detectors for detecting the hydrogen flame are available in the market. The flame detector UV TRON R2868 from Hamamatsu Photonics K.K. reveals whether the flame is present or not, but

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it cannot locate the flame position. Another UV-C detector with array configuration such as the Si photodiode array S4111-46Q from Hamamatsu Photonics K.K. or the ICX407BLAUV imaging system from PCO-TECH Inc. can locate the flame source. However, they utilize a processing unit such as a computer to process the captured images and to extract some useful information. In this study, we aim to realize a single-chip smart UV sensor that not only detects the presence of the hydrogen flame, but also generates information about the flame related to the location, size, moving speed, moving direction, and spreading status without a computer system.

In the flame analysis field, the hydrogen flame is categorized as a high-speed object. Therefore, for a real-time analysis, the image data from the sensor should be transferred to the processing unit as soon as possible. Furthermore, it is necessary to recognize the edge of the flame as well.⁽⁵⁾ Addressing these requirements, the proposed smart UV sensor introduces a three-dimensional (3-D) integration system architecture between the bioinspired optoelectronic integrated circuit (OEIC) and the field-programmable gate array (FPGA). The 3-D integration deals with the data transfer issue, and the bioinspired OEIC acts as the preprocessing unit that has a function as edge detection for the FPGA. Having a preprocessing unit is very useful for reducing the tasks in the FPGA as the main processing unit. OEIC is a technology that integrates photonic devices and electronic circuits monolithically or heterogeneously. As bioinspired OEIC, we would like to integrate the focal plane array as the photonic device with the edge detection circuit, which mimics the outer vertebrate retina, as the electronic circuit. Figure 1(a) shows the vertebrate retina structure.⁽⁶⁾ The outer retina, which has a function as edge detection, consists of photoreceptor cells, horizontal cells, and bipolar cells. Figure 1(b) illustrates the model of the outer vertebrate retina. The AlGaN on a sapphire substrate backside-illuminated Schottky barrier diode (BSI-SBD) photodiode array, which represents the photoreceptor cells, has been fabricated in our laboratory.⁽⁷⁾ The horizontal cells and bipolar cells were fabricated as a CMOS-based edge detection circuit (EDC) described in this paper. The EDC converts a filled object into an outline object to reduce the number of pixels being activated, which leads to the decrease in the power consumption. Since the bioinspired OEIC is a pixel-based analog processing circuit, no clock is required. Moreover, the image data can be transferred in parallel to the processing unit at once. Therefore, rapid data transfer with edge detection capability and low power consumption can be obtained by implementing the bioinspired OEIC.

A smart sensor has four units, namely, a sensor device, an analog front end, an analog-to-digital (A/D) converter, and a digital processor, as shown in Fig. 2.⁽⁸⁾ Following this concept, our smart UV sensor units, as shown in Fig. 3, are the Pt/n-Al_{0.49}Ga_{0.51}N BSI-SBD photodiode array as the

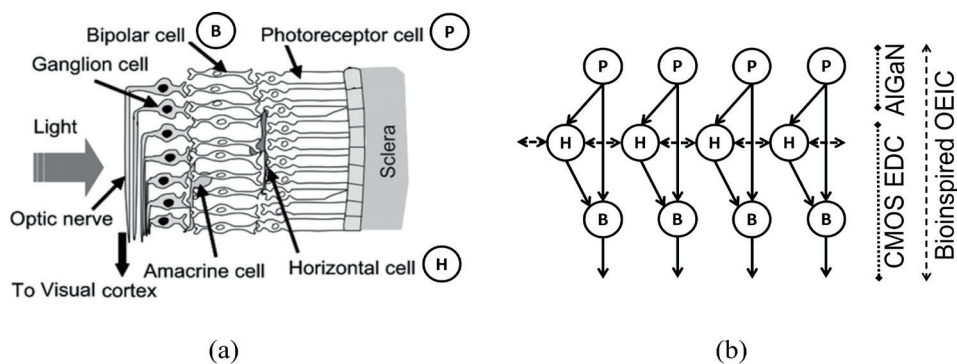


Fig. 1. Bioinspired OEIC. (a) Vertebrate retina structure.⁽⁶⁾ (b) Model of the outer vertebrate retina.

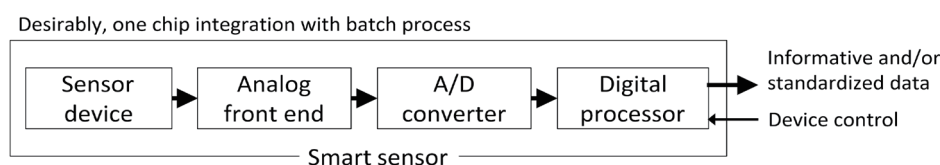
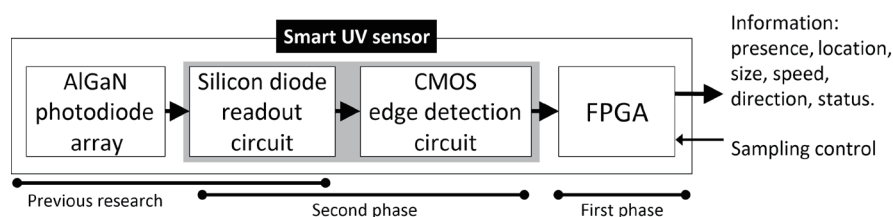
Fig. 2. Concept of smart sensor.⁽⁸⁾

Fig. 3. Proposed smart UV sensor.

sensor device, the silicon diode as the readout circuit, the CMOS-based EDC as the preprocessing unit that generates binary images, and the FPGA as the image analyzer that produces information related to the detected hydrogen flame. The digitized circuit was added into the output stage of the EDC to substitute the A/D converter for producing binary images. Thus, the EDC's output can be connected to the FPGA's input directly. The FPGA detects the object motion by finding the edge location of the object within the binary images generated by the EDC. In addition, from those edge locations, the FPGA calculates the centroid, size, moving speed, moving direction, and spreading status of the object. The moving speed measurement will be useful for analyzing the flame speed. The moving direction can be used to indicate where the flame moved. The spreading status informs whether the flame expands, remains steady, shrinks, or disappears from the image. The motion object detection algorithm in the FPGA has been implemented at the first phase.⁽⁹⁾ In this second phase, the EDC along with the readout circuit was fabricated.

The proposed smart UV sensor integrates its units by stacking to form a single chip. In 2011, Xilinx introduced the first commercially available 2.5-D integrated system architecture FPGA device XC7V2000T with the Stacked Silicon Interconnect (SSI) technology.⁽¹⁰⁾ The SSI technology integrates homogeneous or heterogeneous dies onto the silicon interposer. The silicon interposer is an electrical interface routing between one chip/die and to another. We propose an integration concept between the bioinspired OEIC and the FPGA as shown in Fig. 4. By utilizing the SSI technology, the outputs of the bioinspired OEIC are connected to the FPGA logics via a silicon interposer as illustrated by Fig. 4(a). When the FPGA vendor allows a custom vertical stacking with heterogeneous dies in the future, we would like to have an integration structure as shown in Fig. 4(b).

In this paper, we describe the second phase, which is the fabrication of the EDC chip along with the silicon diode. The fabricated photodiode array in the previous research was not used in this paper. The currents generated by a microcontroller were used to simulate the photocurrents. Then, the fabricated EDC chip was integrated with the FPGA using wires followed by the evaluation of the speed calculation performance. The EDC chip was fabricated by following the requirements derived from the fabricated photodiode array. The motion object detection circuit in the FPGA should also be able to detect an object with the requirements as listed in Table 1. The expected

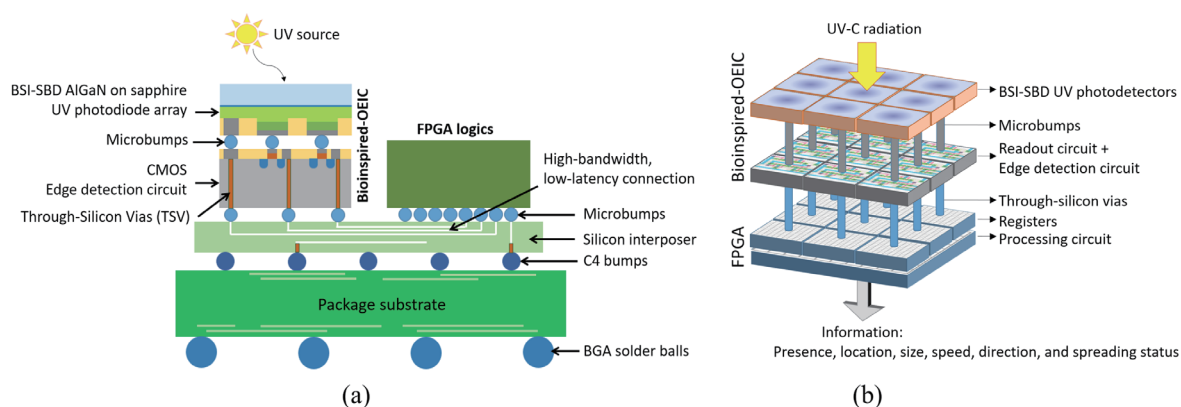


Fig. 4. (Color online) Integration concept between the bioinspired OEC and the FPGA with (a) 2.5-D/3-D integration with the SSI technology or (b) true 3-D integration.

Table 1

Requirements for the EDC and the motion object detection in the FPGA.

Detection power	10 pW/mm ² –10 μW/mm ²
Photocurrent ($\eta = 10\%$)	14.1 fA–14.1 nA
Hydrogen flame speed	18.6 m/s
Distance between flame and sensor	~10 m

detection power for the sensor is 10 pW/mm²–10 μW/mm². Thus, the fabricated photodiode with a sensing area of $250 \times 250 \mu\text{m}^2$ will be expected to generate a photocurrent of 14.1 fA–14.1 nA for an external quantum efficiency (η) of 10%. The smart UV sensor was expected to detect a hydrogen flame 10 m away from the sensor with a flame speed of 18.6 m/s. The hydrogen flame speed of 18.6 m/s was chosen as a target for the system. The maximum possible flame speed of a deflagration burning hydrogen flame is given by the speed of sound in the unburnt gas mixture, which is 975 m/s for a stoichiometric H₂-air mixture.⁽¹¹⁾

2. Materials and Methods

2.1 Previous research on a Pt/n-Al_{0.49}Ga_{0.51}N Schottky barrier diode

An AlGaIn BSI-SBD photodiode on a sapphire substrate with an AlN template as buffer layer was chosen because of four reasons. The first is that it was easy to fabricate using the standard CMOS process. The second is that a Schottky structure offers fast response and little persistent photoconductivity.⁽¹²⁾ The third is that an AlN template is the best option for avoiding cracks and absorption losses (in a BSI photodetector) compared with a GaN template.⁽¹²⁾ The fourth is that the BSI structure can be stacked with the readout circuit using microbumps or other bonding techniques.⁽¹³⁾

The structure of the fabricated AlGaIn BSI-SBD photodiode array was composed of a 300 μm sapphire substrate, a 100 nm AlN buffer layer, a 1500 nm n⁺-Al_{0.64}Ga_{0.36}N contact layer, a 400 nm n⁻-Al_{0.49}Ga_{0.51}N active layer, a 100 nm platinum Schottky metal, a 140 nm four-layer (Ti/Al/Ti/Au) ohmic contact, and a 500 nm Au pad contact. The sensing area of one photodiode was 250

$\times 250 \mu\text{m}^2$ with a $500 \mu\text{m}$ pitch between the centers of two adjacent photodiodes. It was reported that the mesa patterning by inductively coupled plasma reactive-ion etching (ICP-RIE) for a depth of 500 nm caused a surface interface defect. The result was improved by boiling the sample in a HCl solution at $108 \text{ }^\circ\text{C}$ as a damage treatment. Another treatment is that before Schottky contact evaporation, the sample was boiled in a HCl solution at $50 \text{ }^\circ\text{C}$. The amount of the generated photocurrent (I_P) is described in Eq. (1).

$$I_P = (SP\lambda\eta q) / (hc) \quad (1)$$

Here, S is the sensing area of the photodiode ($250 \times 250 \mu\text{m}^2$), P is the radiation power at the photodiode (10 pW/mm^2 – $10 \mu\text{W/mm}^2$), λ is the wavelength of the UV radiation (280 nm), η is the external quantum efficiency, q is the elementary particle charge ($1.602 \times 10^{-19} \text{ C}$), h is Planck's constant ($6.626 \times 10^{-34} \text{ Js}$), and c is the speed of light ($3.0 \times 10^8 \text{ m/s}$). For the given radiation power ranges of 10 pW/mm^2 – $10 \mu\text{W/mm}^2$ and the external quantum efficiency of 10% , the photocurrent will be 14.1 fA – 14.1 nA . The lowest radiation power of 10 pW/mm^2 received by the photodiode is lighter at 10 m away from the photodiode without an optical subsystem. Figure 5 shows the top view of the fabricated photodiode array and the I – V characteristic under illumination. Under the dark condition, the leakage current of the photodiode was 10^{-13} A . Under the illumination with an ultraviolet wavelength of 296 nm and a radiation power of $6.4 \mu\text{W/mm}^2$, the photodiode showed a photocurrent of $8 \times 10^{-11} \text{ A}$ and a responsivity of $2 \times 10^{-4} \text{ A/W}$. The shifting of the cross section between the reverse bias and the forward bias from 0.0 to 1.0 V was due to the charge traps in the depletion region, which might be created during fabrication processes or caused by crystal defects. In addition, above the bias voltage of 1.25 V in the forward bias, the current line bends, which shows that the current is limited by series resistance within the photodiode structure.

2.2 Silicon diode readout circuit and edge detection circuit fabrication

The readout circuit using a silicon diode was investigated in our laboratory.⁽¹²⁾ The silicon diode was applied with a current-to-voltage converter structure to convert the photocurrent generated by the photodiode into voltage continuously. This is because the trapped electric charge

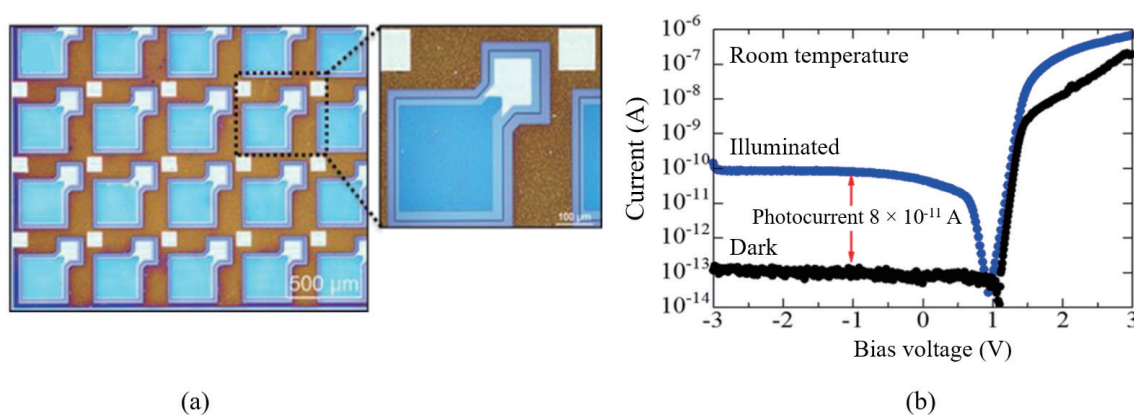


Fig. 5. (Color online) Fabricated photodiode array. (a) Top-view microscopy image. (b) I – V characteristic under illumination.

in the deep levels of the AlGaIn device should be discharged by using a short-circuit current. The silicon diode has a logarithmic profile as well. Hence, a wide dynamic range of the radiation power received by the photodiode can be obtained.

Figure 6 shows the edge detection architecture inspired by the outer vertebrate retina.⁽¹⁵⁾ The outer vertebrate retina consists of photoreceptor cells, horizontal cells, and bipolar cells. The horizontal cells (H) smooth the photocurrent signals from the photoreceptor cells (P) by spreading the photocurrent signals to its neighbor cells. The bipolar cells (B) subtract the photocurrent signals from P and the currents from H . Thus, at the edge position, B generate a spiking signal. The digitized cells (D) produce binary voltage signals by comparing the threshold current (I_{TH}) with the current from B . The I_{TH} is generated by applying a threshold voltage (V_{TH}) externally. The schematic for the silicon diode as the readout circuit and the edge detection circuit as the coprocessor shown in Fig. 7 is referred as a pixel unit. To have a one-dimensional array, the horizontal cell, which is called a resistive network, connects two adjacent pixel units. The R1 is connected to the previous pixel unit's R2 and the R2 is connected to the next pixel unit's R1. The first pixel unit has the unconnected R1 and the last pixel unit has the unconnected R2.

The pixel unit circuit was simulated as a one-dimensional array as well as a two-dimensional array using a simulation program with integrated circuit emphasis (SPICE) model parameter level 3. Since the SPICE model parameter level 3 cannot simulate the subthreshold region, the pixel unit circuit was forced to work in the saturation region by adding an offset voltage V_{OFS} on the cathode of the silicon diode D1. The resistive network, which connects the two adjacent pixel units, was built using a PMOS transistor with the body terminal tied to the V_{DD} and the gate terminal tied to the ground.

To determine how many pixels should be fabricated, the basic optical lens equation that describes the relationship between the field of view and the lens focal length, as shown in Eq. (2), can be used as an approach. Adding a lens in front of the sensor will make the sensor have a better focused object and increase the received photon flux.

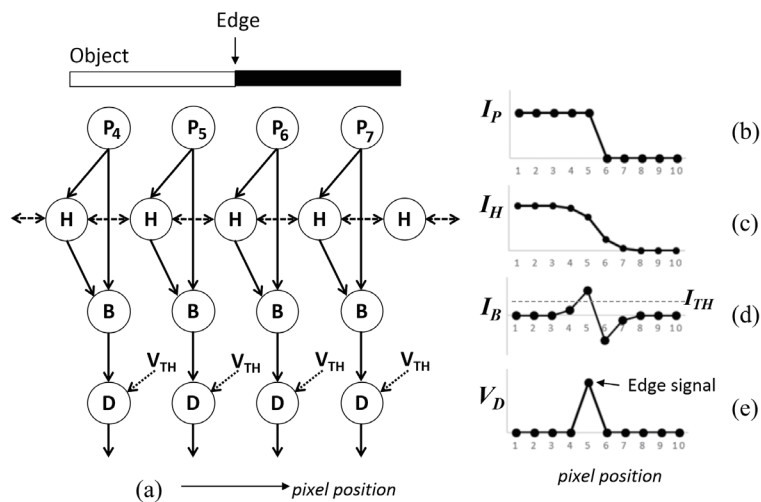


Fig. 6. Edge detection architecture.⁽¹⁵⁾ (a) Model based on the outer vertebrate retina. (b) Output signals of photoreceptor cells (P). (c) Output signals of horizontal cells (H). (d) Output signals of bipolar cells (B). (e) Output signals of digitized cells (D).

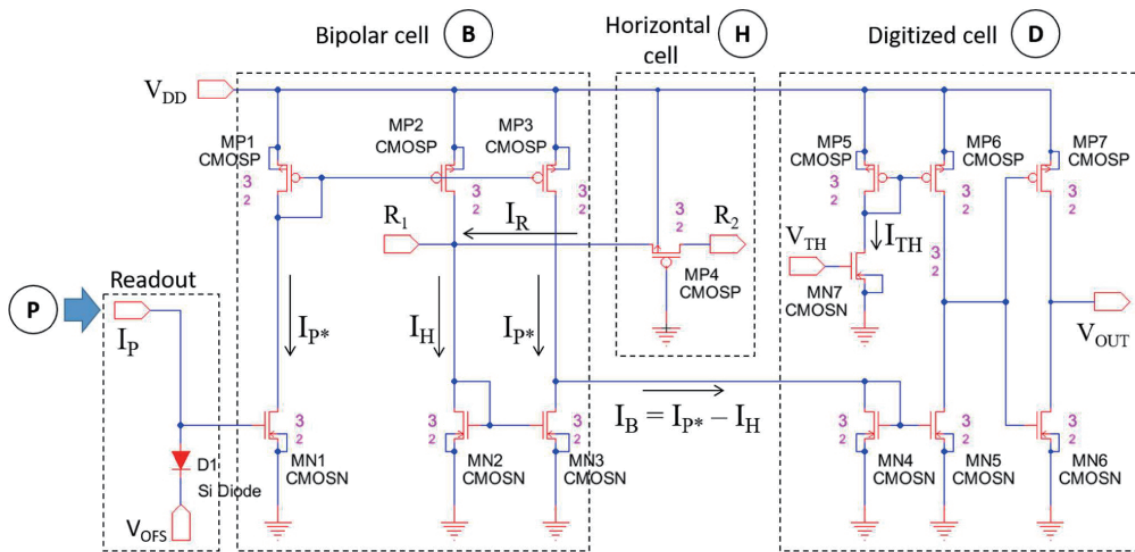


Fig. 7. (Color online) A pixel unit consists of a readout circuit, a bipolar cell circuit, a horizontal cell circuit, and a digitized cell circuit.

$$S/H = F/D \quad (2)$$

Here, S is the sensor resolution, H is the field of view or the height of the object, F is the lens focal length, and D is the object distance from the lens. For example, the smart UV sensor is designed to be placed 10 m away from the hydrogen flame and a lens with a focal length of 3 mm is added in front of the sensor. If we assume that the hydrogen flame has a height of 5 m, then the hydrogen flame will be seen by the sensor as an object with a height of 1.5 mm. Therefore, using the fabricated photodiode array with a pitch of 500 μm will require at least 3 pixels in one column. The relationship between the actual object speed and the pixel speed can be derived as well. An object with a speed of 18.6 m/s will reach a height of 5 m in 0.27 s. At the sensor's surface, the object will have a speed of 3 pixels/0.27 s or 11.16 pixels/s. In other words, a real object speed of 18.6 m/s will be converted to 11.16 pixels/s. In this paper, the one-dimensional array of 1×16 pixel units was fabricated using 1.5 micron process technology and 5 micron design rules in our laboratory.

2.3 One-dimensional array motion object detection in FPGA

The motion of an object can be detected by optical flow methods. Computer vision algorithm methods such as Lucas & Kanade's approach, Horn & Schunck's algorithm, or elementary motion detection (EMD) method can be used to calculate the vector of each pixel in the image.^(16–18) Taking the vector resultant for a corresponding object would be complicated because their pixels should be clustered beforehand. To simplify the calculation of the vector resultant, we implemented a motion object detection using a histogram projection algorithm that projects the object vertically and horizontally.

Figure 8 shows the comparison for calculating the vector resultant of a moving object between the optical flow method and the histogram projection algorithm. In this paper, the term "image"

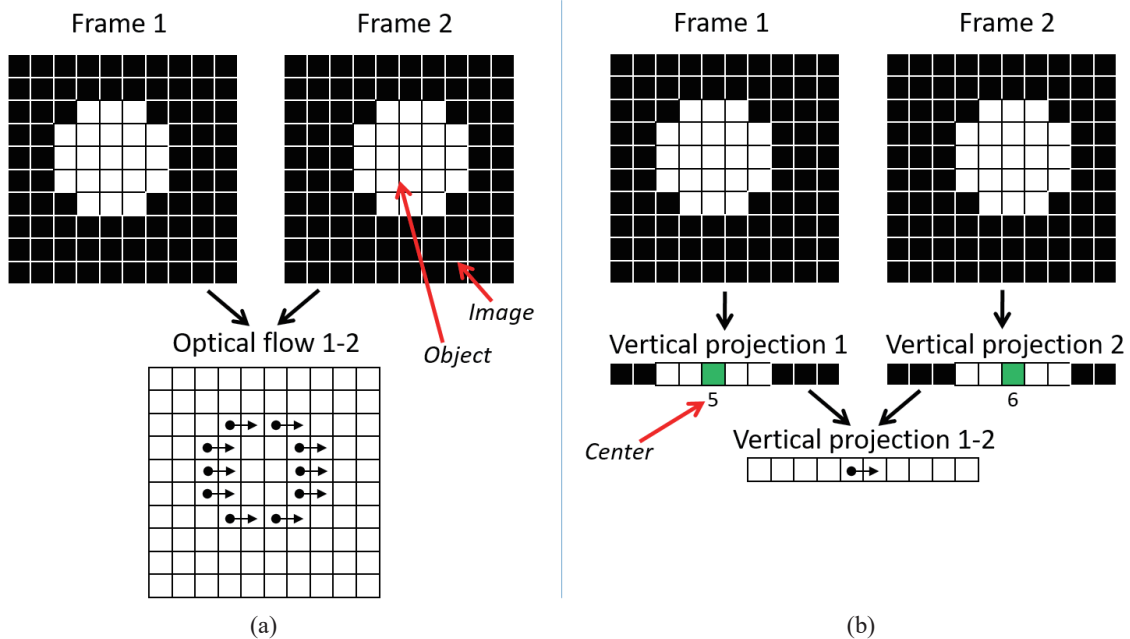


Fig. 8. (Color online) A comparison for calculating vector resultant of a moving object between (a) optical flow method and (b) histogram projection algorithm.

refers to the observation area of the system and the term “object” refers to the representative of the captured UV radiation generated by the hydrogen flame. Figure 8(a) is an example of the optical flow method between two consecutive frames. To obtain the vector resultant of the moving object, the vectors must be clustered to the corresponding object. Figure 8(b) shows the histogram projection algorithm that produces two vectors from each center of the projected object (in the vertical projection as well as in the horizontal projection). The horizontal projection is not shown in Fig. 8(b) to display a clean figure. With only two vectors, it is easy to obtain the vector resultant of the moving object. Moreover, the projected objects not only provide the speed and direction of the object, but also the object presence itself, the object centroid, the object size, and the object spreading status. The implementation of the motion object detection in the FPGA was described in the first phase.⁽⁹⁾ In the first phase, the hydrogen flame was modelled as a moving circle object. It was not a realistic model for the actual hydrogen flame, which is usually formed as a burst or a spurt with a fixed initial position. However, in this step, we would like to verify that this method can measure the speed and direction of the given object, which can be extended for a more realistic model.

3. Results

A one-dimensional array simulation of 1×70 pixels was performed to determine the working range of the circuit as shown in Fig. 9. In this simulation, the threshold voltage of the PMOS was -1.5 V, the threshold voltage of the NMOS was 1.5 V, the V_{DD} was set to 3.0 V, the offset voltage V_{OFS} was set to 1.6 V, and the threshold voltage V_{TH} was set to 1.64 V to generate a threshold current I_{TH} of 110 nA. The photocurrent I_P was set as step stairs from 1 pA to 1 μ A. From Fig. 9, the EDC could detect the edges for 6 orders.

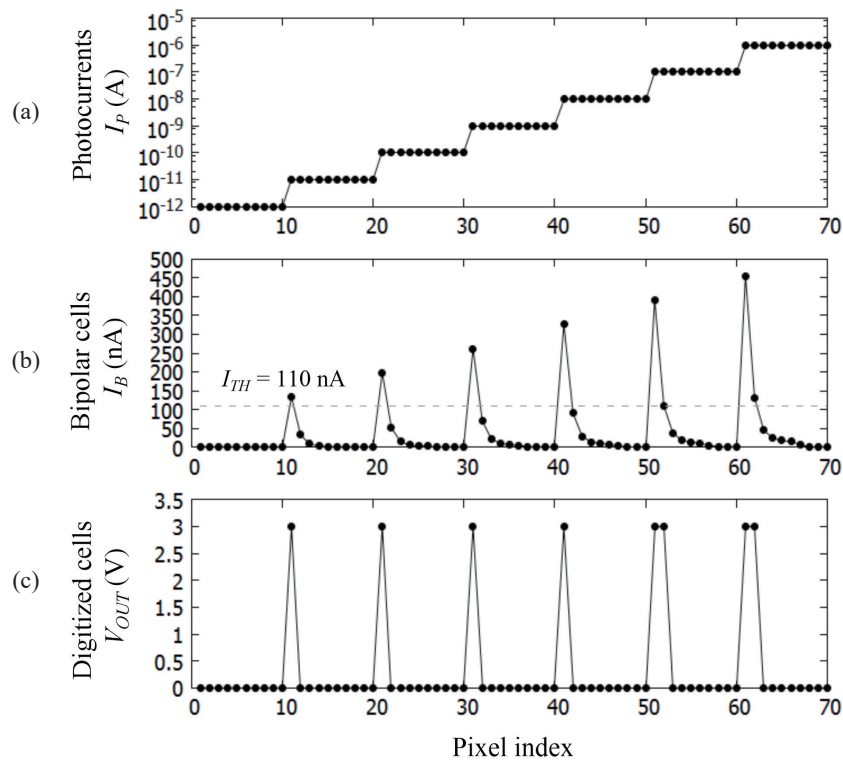


Fig. 9. EDC of 1×70 pixels' simulation result with (a) photocurrents I_P , (b) bipolar cells' currents I_B with the threshold current I_{TH} , and (c) output voltage of digitized cell circuits V_{OUT} .

Next, a two-dimensional array simulation of 45×45 pixels was carried out to see the response of the system for a given two-dimensional object. As shown in Fig. 10, an object with a candle-flame shape was simulated in three different current ranges. The simulated photocurrents at the first, second, and third columns had ranges of 1 pA–1 nA, 1 pA–10 nA, and 1 pA–100 nA, respectively. It is shown in Fig. 10 that the binary image was thicker when the given photocurrent was larger. As confirmed in Fig. 9, a step or an edge with a large photocurrent (I_P) produces a large output current (I_B). Since the threshold current (I_{TH}) was fixed at 110 nA, the binary image became thicker for the same object pattern. On the basis of Figs. 9 and 10, it is concluded that the design of the EDC is as expected.

The fabricated EDC chip size was $8 \times 8 \text{ mm}^2$ as shown in Fig. 11. The threshold voltages of NMOS and PMOS are 1.6 and -1.6 V, respectively. The silicon diode D1 had a forward voltage of 0.58 V. The leakage current at -1.0 V is 0.67 nA. The large leakage current of the silicon diode is likely due to the defect during the fabrication processes. During the chip measurement, the offset voltage V_{OFS} was set to 2.2 V and the V_{DD} was set to 5.0 V.

After confirming the threshold voltage of the MOS transistors as well as the forward voltage of the silicon diode, the next step is to determine the threshold voltage V_{TH} to digitize the image. A current source generator was used to simulate the photocurrent inputs with a pattern of “0001110000000000” to the fabricated EDC chip. The logic-0 represents a current of 0 A, while the logic-1 represents a current from 5 nA–100 μ A. For each current input value, the threshold voltage V_{TH} was adjusted until the outputs of the EDC chip showed a pattern of “0001010000000000”. Here, the logic-0 represents a voltage of ~ 6.5 mV and the logic-1 represents a voltage of ~ 1.8 V.

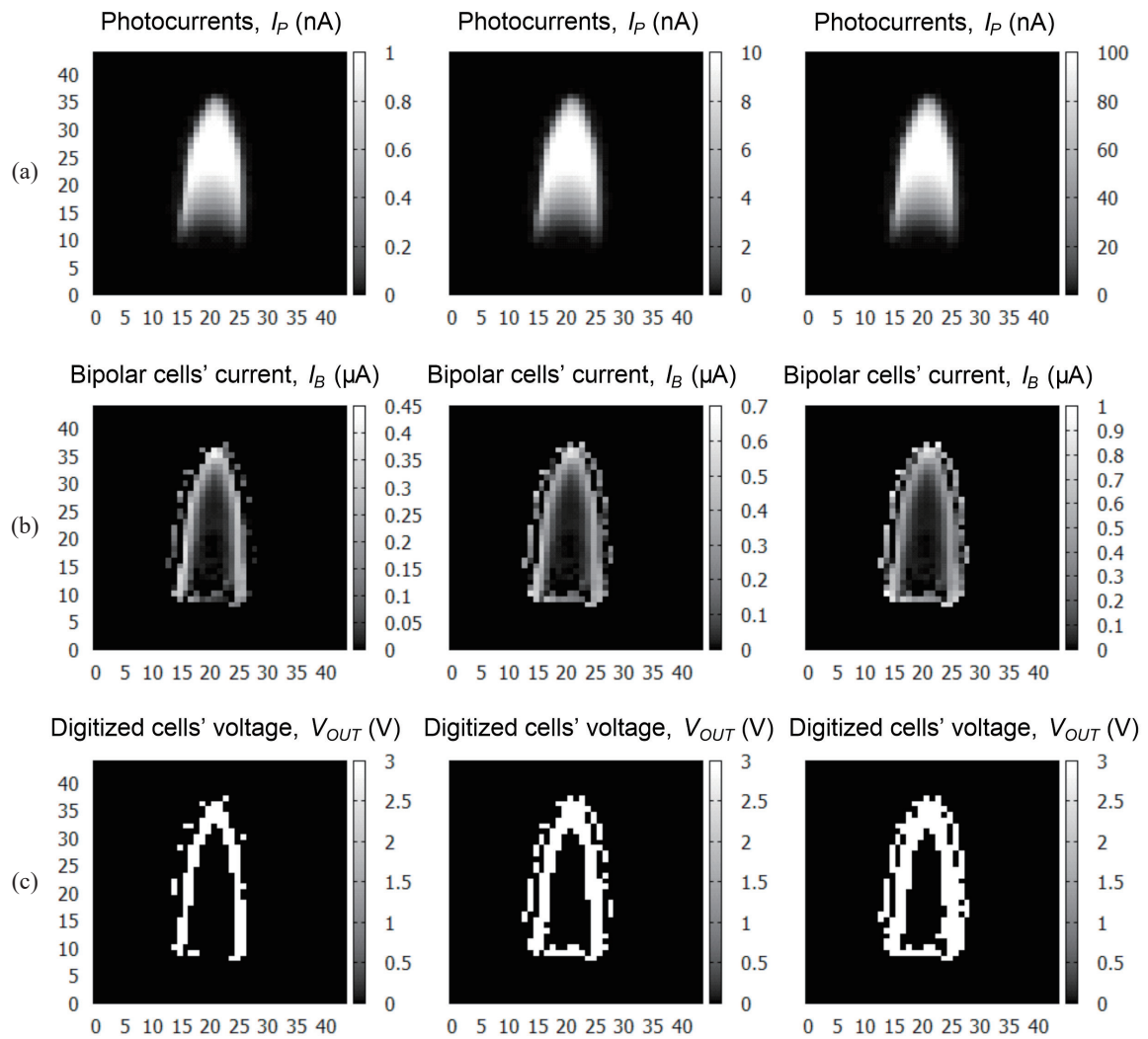


Fig. 10. A two-dimensional edge detection's simulation result with (a) simulated photocurrents (I_p) in different current ranges, (b) output current of bipolar cell circuits (I_B), and (c) output voltage of digitized cell circuits (V_{OUT}).

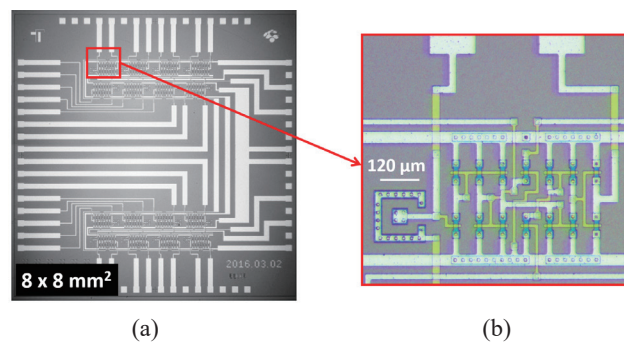


Fig. 11. (Color online) Micrograph of (a) the fabricated edge detection circuit chip and (b) the zoomed version of the pixel unit.

The output of the EDC chip cannot reach the V_{DD} level because the output stage of the EDC was not equipped with output buffers. However, by enabling the LVCMOS18-option for the FPGA's input pins, the maximum voltage level for logic-0 (V_{IL}) and minimum voltage level for logic-1 (V_{IH}) of the FPGA's input pins become 380 mV and 0.8 V, respectively. Thus, the output pins of the EDC chip can be connected to the input pins of the FPGA directly. Figure 12 shows the relationship between the selection of the threshold voltage V_{TH} and the working range of the fabricated EDC chip. In this case, a threshold voltage V_{TH} of 2.2 V was selected, which makes the fabricated EDC chip have a working range for the photocurrent I_P of 100 nA–50 μ A.

To evaluate the speed calculation of the wired-integration system between the fabricated EDC chip and the FPGA, a microcontroller was utilized to generate the photocurrent I_P for the EDC chip. The output voltage of the microcontroller's pins was 3.3 V. The microcontroller's output pins were connected to the EDC chip's inputs in series with 100 k Ω resistors. With the V_{OFS} set to 2.2 V, a photocurrent I_P of 5.2 μ A was expected to flow from the microcontroller into the EDC chip. The motion object detection circuit inside the FPGA was modified to process the moving object with the image resolution of 1×16 pixels. The data width of the information generated by the

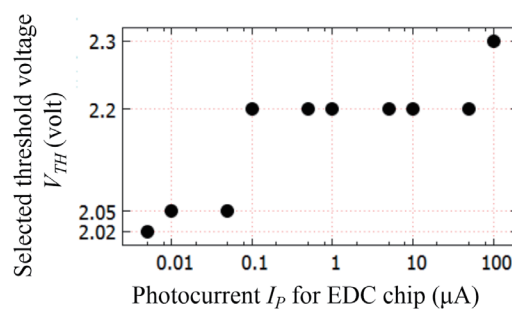


Fig. 12. Working range of the fabricated EDC chip for a selected threshold voltage V_{TH} .

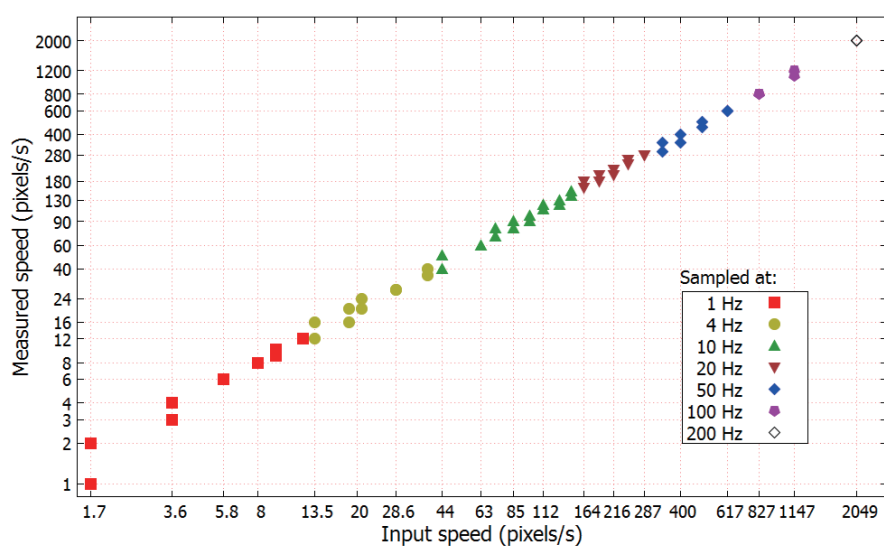


Fig. 13. (Color online) Measured speed result of the system.

FPGA was 64 bits. The information consists of 8-bit location, 4-bit size, 16-bit speed, 8-bit angle, 4-bit status, 8-bit sampling frequency, 8-bit checksum, and 8-bit timestamp. The microcontroller was programmed to generate a moving pattern in a speed range of 1.7–2049 pixels/s. Figure 13 shows the relationship between the input speed generated by the microcontroller and the measured speed produced by the FPGA circuit. The measured speed indicates the maximum and minimum readings by the FPGA circuit. The motion object detection circuit uses integer operations for the calculation. Therefore, the result of the measured speed is the nearest integer of the multiple value of the selected sampling frequency. For instance, the speed of 1.7 pixels/s was read as 1 pixel/s or 2 pixels/s with the sampling frequency of 1 Hz. The sampling frequency of the motion object detection circuit in the FPGA was set differently for different ranges of the given input speed, which is represented with different colored patterns in Fig. 13. This is due to the range of the detectable speed in this system as described in Eq. (3).⁽⁹⁾

$$V_{min/max} \text{ (pixel/s)} = D_{min/max} \text{ (pixel)} / T \text{ (s)} \quad (3)$$

Here, $D_{min/max}$ is the minimum and maximum displacement of the object inside the image and T is the sampling rate of the motion object detection in the FPGA. From Fig. 13, the measured speed of the system was 1–2,000 pixels/s. This equals to 1.7–3,333 m/s for the actual speed if the system uses a lens with a focal length of 3 mm and the hydrogen flame is located 10 m away from the sensor.

4. Discussion

There are two points to be considered for stacking the previous fabricated photodiode array and the fabricated EDC chip as the bioinspired OEIC. The first is that both should have the same working range. The experiment results showed that the fabricated EDC chip had a larger working range than the design requirement. In this case, adding an amplifier circuit to boost the photocurrent or placing an optical lens to increase the photon incident on the photodiodes' surface can address this issue. The second is that the size of the photodiode should be larger than the EDC to obtain a fill factor of 100%. The fabricated EDC chip had an area of $875 \times 600 \mu\text{m}^2$ and the photodiode had an area of $250 \times 250 \mu\text{m}^2$. Scaling the design rules from 5 to 1 micron will achieve an area of $175 \times 120 \mu\text{m}^2$, which is sufficiently fit under the photodiode array.

There is a case when the size of the object is larger than the image area. For instance, when the hydrogen flame occurs at a short distance from the sensor or the actual size of the hydrogen flame is indeed large, the EDC will not generate edge. Then, since there is no edge signal from the EDC, the motion object detection circuit in the FPGA decides this condition as no object. As a result, the system fails to detect the presence of the hydrogen flame. To meet a fail-safe design, an additional circuit can be added into the EDC. The additional circuit senses the level of the photocurrent at a certain threshold value to trigger a dedicated signal to the FPGA circuit indicating that the UV-C radiation is present. Hence, the system can still generate an alert signal, even if the object size is larger than the image area of the sensor. However, when the dedicated signal is triggered by a spike of UV-C radiation that might be produced by another source such as arcs, the FPGA circuit should add some delays preventing false alarms. Then, a calibration might be required for determining the suitable delays.

The 3-D structure of the OEIC can be extended for a multispectral image detector. Since the AlGaIn on a sapphire structure is transparent to light, an additional silicon-based photodetector can be fabricated along with the EDC. For instance, adding an infrared (IR) photodetector will result in the sensor capturing both UV radiation and IR radiation at the same time. The captured IR radiation can be used to locate the heat generated by the object or human.

The speed calculation requires a specific sampling frequency for a different range of object speed. In the experiments, the sampling frequency can be adjusted manually. However, for a real application, this will cause a problem. Designing a multi-sampling frequency will be carried out in the future. Multiple speed calculator units with different sampling frequencies can be implemented within the FPGA simultaneously. Then, a decision algorithm selects one of the speed calculator units to be selected as the result.

To be an Internet of Things (IoT)-enabled device, the smart UV sensor can be connected to a radio communication module on board. Generally, to have a small form factor, a battery-powered device is preferable. The communication protocols for IoT devices have a low data rate as well as small packet data to be transmitted/received to reduce power consumption. Regarding the packet data, the bluetooth low energy (BLE) has a payload of ~20 bytes.⁽¹⁷⁾ The smart UV sensor with a resolution of 1×16 pixels generates data of 8 bytes, which is fit for the BLE. Further image resolution scaling to 250×250 pixels may require only 12 bytes of data. This confirms that the number of data generated by the smart UV sensor is applicable to an IoT device.

5. Conclusions

The wired integration of a fabricated edge detection circuit chip of 1×16 pixels and the FPGA has been described. The integrated system was capable of calculating the speed of a given moving object with a speed of 1.7–2,049 pixels/s at different sampling frequencies from 1 to 200 Hz. The bioinspired architecture opens the possibility of 3D integration for a massive parallel data transfer. The reprogrammable feature of an FPGA and the SSI technology that allows for stacking heterogeneous dies such as OEICs and logics might create a wide area of applications, especially for a high-speed imaging system.

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