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Low Noise CMOS Temperature Sensor with On-Chip Digital Calibration

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In this paper, we present a low-noise CMOS temperature sensor with an on-chip digital calibration circuit. The low-voltage bandgap reference circuit is designed to generate current proportional to absolute temperature (PTAT) using a parasitic NPN bipolar junction transistor (BJT). To adjust the output offset and gain of the temperature sensing core, an additional calibration stage based on the differential to the single amplifier (D2S) using a differential difference amplifier (DDA) is designed. A calibration circuit with low power and small size can be implemented using the D2S. Also because of the D2S, the conventional multistage offset and gain calibration circuits can be reduced to a single-stage circuit. The analog output is converted to a digital output using a 12-bit successive approximation register (SAR) analog-to-digital converter (ADC). A coarse calibration with 5-bit resolution is performed in the analog domain using a DDA-based calibration circuit, and a fine calibration using a 16-bit arithmetic engine is performed in the digital domain. The temperature sensor IC is implemented using a CMOS 0.18 μm process with an active area of 0.2216 mm^2. The power consumption is 48.6 μW with a 1.8 V supply. The IC can measure temperatures from 10 to 60 °C. The measured gain is 28.36 mV/°C. The input-referred temperature noise is measured to be 0.26 $°C_{RMS}$ with a 200 Hz bandwidth.

1. Introduction

Recently, the development of the wearable healthcare systems has begun to accelerate. Body temperature is one of the most important parameters to detect in healthcare systems, and various temperature-sensing systems have been reported.[1] In conventional temperature sensors based on bipolar junction transistors (BJTs), the complementary to absolute temperature (CTAT) characteristic of the base-emitter voltage (V_{BE}) and the proportional to absolute temperature (PTAT) characteristic of the difference between two base-emitter voltages (ΔV_{BE}) are used to determine body temperature.[2–5]

In this paper, we propose a low-power CMOS temperature sensor with an on-chip calibration circuit. The proposed CMOS temperature sensor can adjust the output offset and gain using a temperature-sensing amplifier (TSA), which is implemented using a differential difference amplifier (DDA).

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To enhance the accuracy of the sensor, temperature sensors with analog domain calibration or digital domain calibration have been evaluated.[4,6–8] To achieve high output accuracy while reducing the overhead of the calibration hardware, a two-step calibration architecture was adopted for the proposed temperature sensor: a coarse calibration in the analog domain, and a fine calibration in the digital domain. In the proposed sensor, a coarse calibration with 5-bit resolution is performed in the analog domain using a DDA-based calibration circuit, and a fine calibration using a 16-bit arithmetic engine is performed in the digital domain. The circuit design and the measurement results are described in Sects. 2 and 3, respectively. The discussions and conclusions are presented in Sect. 4.

2. Design of Temperature Sensor

2.1 Top-level architecture

A block diagram of the proposed low-power CMOS temperature sensor with an on-chip calibration circuit is shown in Fig. 1. The sensor is composed of a bandgap reference circuit, a TSA with programmable gain and offset, a lowpass filter (LPF), and a 12-bit succesive approximation resistor (SAR) analog-to-digital converter (ADC). The bandgap reference circuit measures the temperature of users using two NPN BJTs, and the temperature is converted to voltage based on the BJT characteristics. The TSA with programmable offset and gain adjusts the output voltage. The 12-bit SAR ADC converts the calibrated voltage into a digital signal through the LPF. The coarse calibration with 5-bit resolution is performed in the analog domain using the DDA-based calibration circuit, and the fine calibration using a 16-bit arithmetic engine is performed in the digital domain.

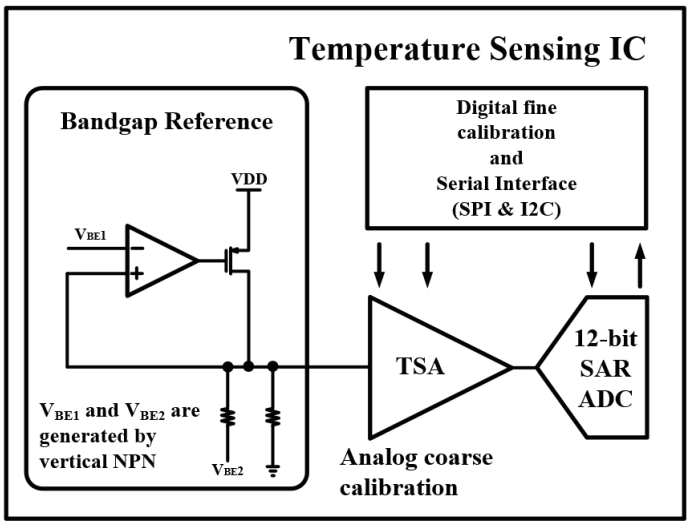

Fig. 1. Block diagram of the proposed temperature-sensing IC.

2.2 Bandgap reference circuit

The temperature sensing core is implemented using the NPN BJTs. The vertical structure of the NPN BJT is illustrated in Fig. 2. The NPN BJTs use a deep *N*-well in this design. The unit emitter area is 10 × 10 μm^2. The base-emitter voltage V_{BE} can be expressed as

$$V_{BE} = \eta \cdot (kT / q) \cdot \ln (I_C / I_S), \tag{1}$$

where η is a process-dependent nonideality factor where the value is nearly 1, k is the Boltzmann constant, q is the electron charge constant, I_C is the collector current, and I_S is the saturation current. The architecture of the bandgap reference circuit is shown in Fig. 3. The bandgap reference is a modified version of a previously reported low-voltage bandgap reference.[5] The voltage V_{BE1} has CTAT characteristics. If the temperature increases, V_{BE1} decreases. The output V_{TEMP} also decreases owing to the virtual short of the operational amplifier between V_{BE1} and V_{TEMP}.

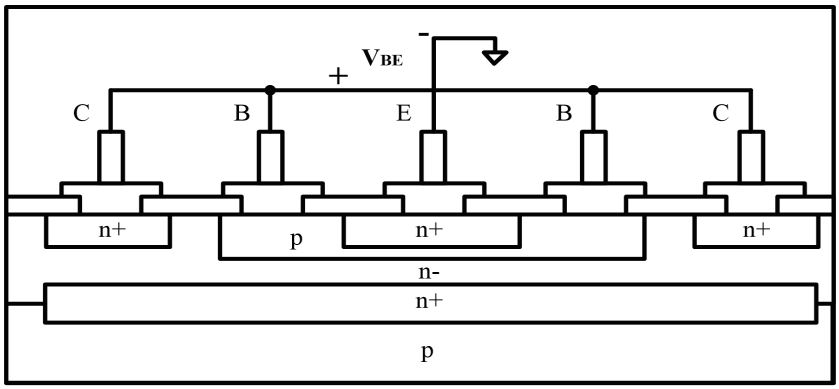

Fig. 2. Structure of the diode used for NPN BJT.

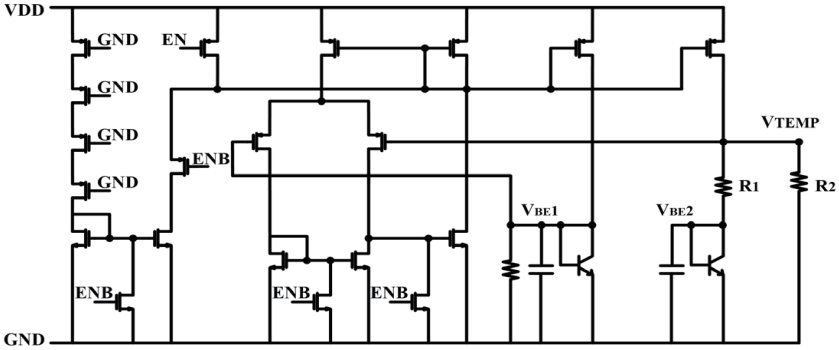

Fig. 3. Architecture of the bandgap reference circuit.

2.3 TSA

A schematic of the TSA is shown in Fig. 4. The offset and gain of the temperature-sensitive input signal, V_{TEMP}, is adjusted in this stage. The V_{CO}, the offset control voltage for offset compensation, is generated by resistive dividing of the reference voltage V_{REF}. V_{REF} can be trimmed by the 4-bit digital control code OFFSET<3:0>. The gain variations are adjusted using the digitally programmable feedback resistors, Gain<3:0>, in the differential to single amplifier (D2S). The D2S is implemented using noninverting amplifier configurations using the DDA.

3. Measurement Results

A chip microphotograph of the temperature sensor IC is shown in Fig. 5. The chip was fabricated using the Magnachip 0.18 μm 1P6M CMOS process with the deep N-well option. The overall active area of the temperature sensor IC is 0.2216 mm^2. Here, the size of the bandgap

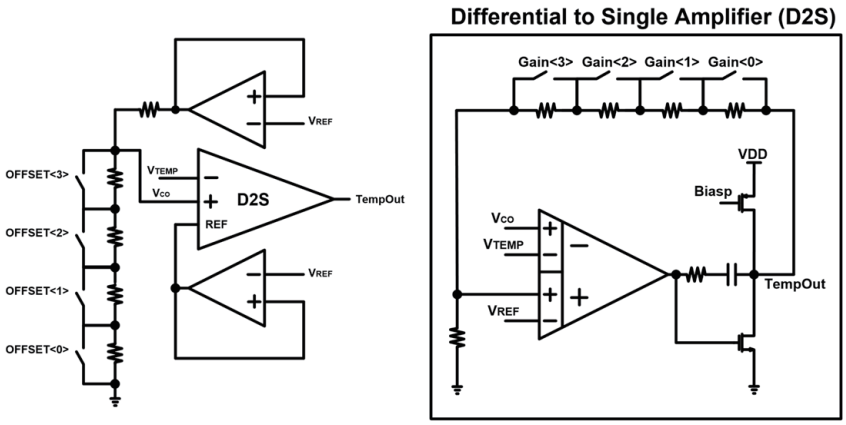

Fig. 4. Architecture of TSA.

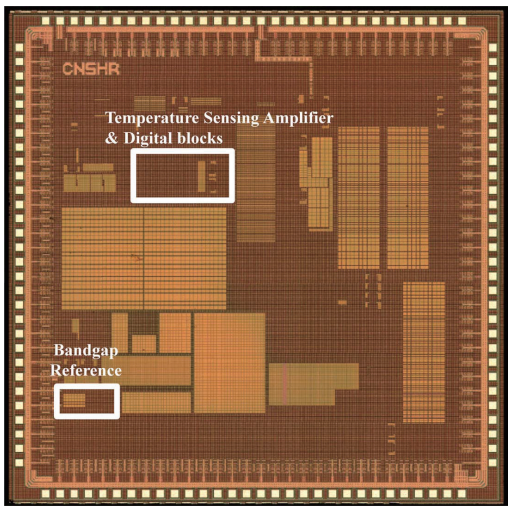

Fig. 5. (Color online) A chip microphotograph of temperature sensor IC.

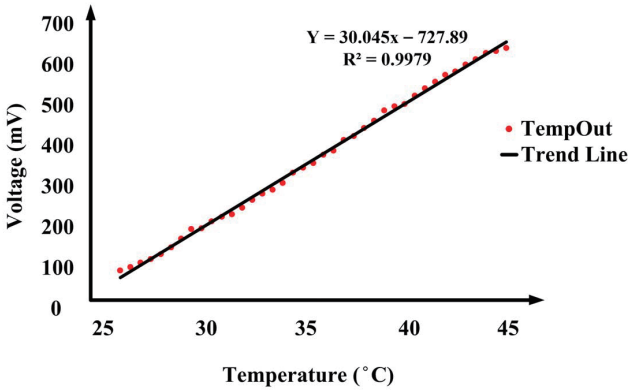

Fig. 6. (Color online) Results of measurements by temperature sensor IC.

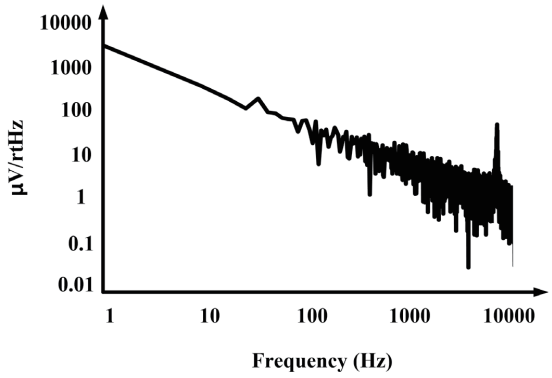

Fig. 7. Output noise of the proposed IC.

Table 1
Performance specifications and comparison to previous studies.

Parameter	**This work**	Ref. 2	Ref. 6	Ref. 7	Ref. 8
Technology (μm)	**0.18**	0.18	0.18	0.18	65 nm
Supply (V)	**1.8**	1.2	1.2	1.2	1
Input-referred noise (°C_{RMS})	**0.261**	0.3	0.3	0.3 °C/LSB	0.94
Temperature range (°C)	**10–60**	0–100	0–100	0–100	0–110

reference circuit is 160 by 440 μm^2, and the size of the TSA and digital blocks is 270 by 560 μm^2. The supply voltage, supply current, and power consumption are 1.8 V, 27 μA, and 48.6 μW at 25 °C, respectively. The input–output characteristics of the temperature sensors after calibration are shown in Fig. 6. The temperature sensitivity and the nonlinearity are 28.36 mV/°C and 2.57% full scale output (FSO), respectively. The output noise measurement is shown in Fig. 7. The integrated output noise is 7.4 mV_{RMS} with a 200 Hz bandwidth. Therefore, the input-referred temperature noise is 0.26 °C_{RMS}. The performance specifications and comparison with previous studies are summarized in Table 1.

4. Conclusions

In this paper, we described a low-power CMOS temperature sensor with an on-chip calibration circuit. This design of a temperature sensor IC with calibration can achieve low power, minimum area, and low noise. The chip was fabricated in a 0.18 μm Magnachip 1P6M CMOS process with an active area of 0.2216 mm^2. The proposed temperature sensor IC consumes 48.6 μW with a 1.8 V supply. The input-referred noise is 0.261 °C_{RMS} with a 200 Hz bandwidth.

Acknowledgments

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