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80–100 V Low-Side Lateral Double-Diffused Metal Oxide Semiconductor Device with Sided Isolation of 0.35 μm Complementary Metal Oxide Semiconductor-Compatible Process

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In this study, a novel 80–100 V multiple reduced surface field (RESURF) lateral double-diffused metal oxide semiconductor (LDMOS) transistor with shallow trench isolation (STI) on both sides of the structure is developed and simulated using a Sentaurus process simulator. The proposed multiple RESURF LDMOS structure achieves benchmark specific on-state resistance while maintaining breakdown voltages of 80 and 100 V with better safe-operating area (SOA) performance. The key feature of this novel n-channel LDMOS (NLDMOS) device is the presence of linear p-top rings in the n-drift region. The optimization of the linear p-top mask design and concentration of p-top in the region is performed in order to achieve benchmark on-state resistance with the desired breakdown voltage. Linear p-top helps the diffusion current to move faster in the drift region, which helps to reduce on-state resistance.

1. Introduction

A lateral double-diffused metal oxide semiconductor (LDMOS) transistor is widely used in smart power technologies. Its applications are mainly in display drivers, power switching, digital audio, and power management devices. Sensor applications like biosensors, gas sensors, and pressure sensors use natural biopolymer materials of LDMOS. It has recently attracted attention due to its compatibility with a complementary metal oxide semiconductor (CMOS) and it can be easily developed in high-voltage LDMOS devices, which have a great deal of high-speed switching capability and prospective applications in consumer electronics. To broaden the applicability of LDMOS devices, it is necessary to enhance their electrical performance characteristics, such as breakdown voltage, low on-state resistance, and high current-driving capability.[(1–4)] The semiconductor revolution that started in the 1960s has led to tremendous developments in the area of device design. For many years, experiments have been carried out to improve breakdown voltage while reducing on-state resistance to be as low as possible. While bipolar junction transistors (BJTs) were the foundation of earlier circuits, they gave way to MOSFETs due to

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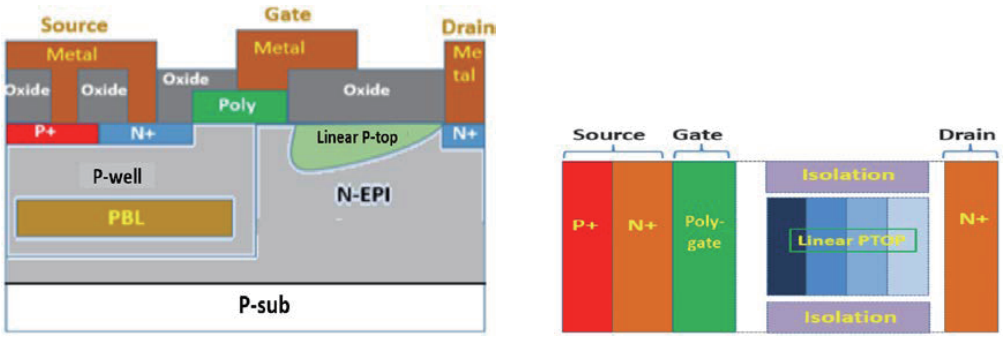
their many inherent advantages. However, all these devices were used in low-voltage (LV), low-power circuits, mostly for signal conditioning. Traditionally, the high-voltage operation has been realized in LV processes using circuit techniques.[5,6] However, these techniques increase both the complexity of the circuit and the power requirements. High-voltage LDMOSs make it possible to integrate LV circuits with high-voltage parts instead of using discrete devices.[7–9] The drift region is present laterally in this case as opposed to power LDMOS structures in which the drift region is vertical.

One point to note is that LDMOS devices are restricted to a niche of high-voltage and low-current circuits, such as cellular telephony, analog power management, "smart" power application, and automotive and audio electronic circuits. They cannot handle high power and therefore cannot be used as a substitute for discrete devices in power electronics circuitry.[10–12] This device technology offered significant advantages over the previous incumbent device technology, which is the silicon bipolar transistor, providing superior linearity, efficiency, gain, and lower-cost packaging solutions.

In this paper, we discuss how far an n-channel LDMOS (NLDMOS) can be used with its limitations in terms of breakdown voltage and on-state resistance. In this paper, the NLDMOS structure with the concept of multiple reduced surface field (RESURF) and a linear p-top ring is being proposed.[13–16] Based on the simulation experiments, an 80–100 V low side is obtained with benchmark on-state resistance (R_{sp}). Double and multiple RESURF methods were developed instead of single RESURF technology to improve the junction/weak avalanche leakage in high-electric-field regions, and an additional layer of opposite conductivity (p-top layer) is incorporated inside the n-drift region.[17,18]

The main purpose of the linear p-top in the NLDMOS is to increase the current-driving capability and maintain the optimum charge balance in the drift region to reduce specific on-state resistance but without sacrificing breakdown voltage, which is the requirement for today's industries.[19] Figures 1(a) and 1(b) show the schematic structure of the proposed NLDMOS device with side isolation in the front and top views, respectively. The p+ buried layer (PBL) clearly shown in Fig. 1(a) is inserted to improve safe-operating area (SOA) performance.[20]



(a) (b)

Fig. 1. (Color online) Schematic view of low-side NLDMOS structure with side isolations in (a) front and (b) top views.

2. Device Design and Simulation

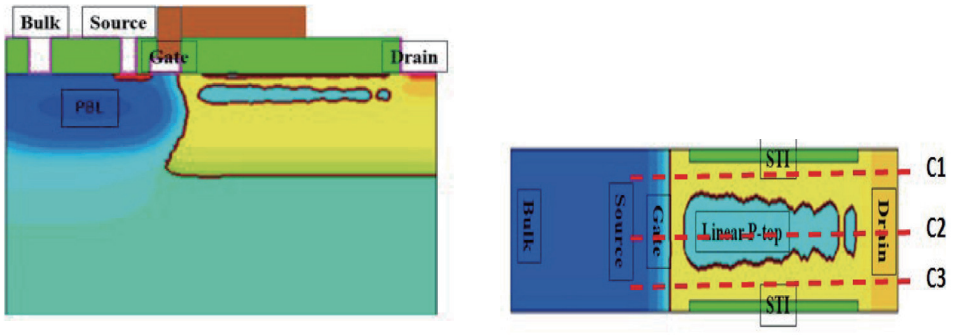
Various design techniques can be used to optimize the device behavior and integrate high-voltage devices in the circuit. High blocking voltage and low on-state resistance are of special interest when low power losses are under consideration. To achieve a cost-efficient device, designing the device is one of the most important constraints that should be optimized.

The device structure is designed by side isolation techniques to reduce the beta gain, thereby to avoid the Kirk effect and reduce the leakage current. Figures 2(a) and 2(b) respectively show the front and top views of the proposed NLDMOS unit cell structure with shallow trench isolation (STI) regions on both sides of the n-drift region, which are obtained by entaurus process simulation. NLDMOS on-state resistance depends mainly on the driving capability in the drift region. Linear p-top maintains the optimum charge balance in the drift and also increases the driving capability in the drift region without reducing the breakdown voltage.

A linearly varying doped (LVD) p-top layer with improved performance for RESURF LDMOS, which can improve the influence of interconnection-related breakdown better than a conventional RESURF structure, has been utilized and proposed. It is clear from Figs. 2(a) and 2(b) that the linear p-top layer is being placed in the n-drift region in order to create higher p–n charges. For process conditions, a substrate with a p-type <100> orientation and a doping concentration of about 6.9×10^{14} cm^{-3} was used. An epitaxial n-type layer of 0.6 μm thickness was grown on a Si substrate with a doping concentration of about 5.7×10^{16} cm^{3}.

3. Results and Discussion

The proposed NLDMOS structure with side isolation is simple and cost-effective, is developed by a CMOS-compatible process, and exhibits benchmark on-state resistance and desired breakdown voltage. The device design is simple and can be used as a multicell structure by keeping devices side by side like an array. The process technology of the devices is made the same by adjusting the p-top mask and drift length that we developed for both 80 and 100 V devices. Thus, it is easy to develop a number of devices with different voltages after some optimization. 3D simulations were carried out to obtain the desired breakdown voltages of more than 80 and 100 V for the unit cell device, having possible lower on-state resistance.

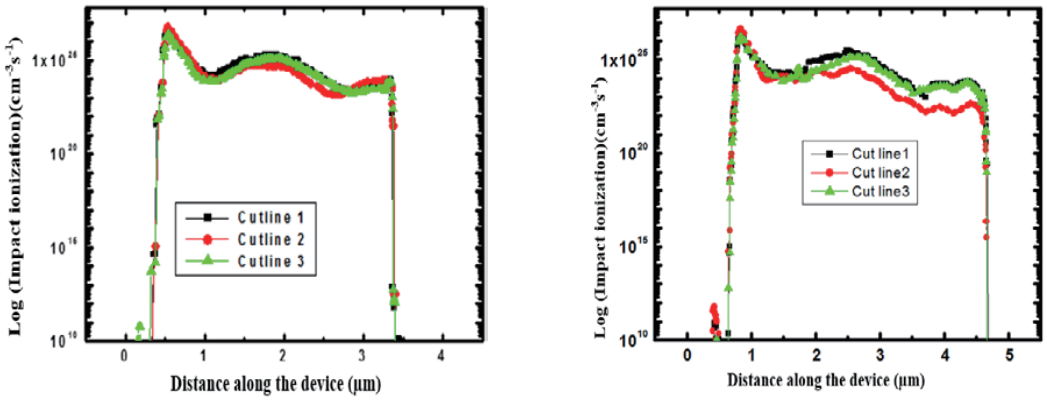


(a) (b)

Fig. 2. (Color online) Proposed low-side structure in (a) front and (b) top views.

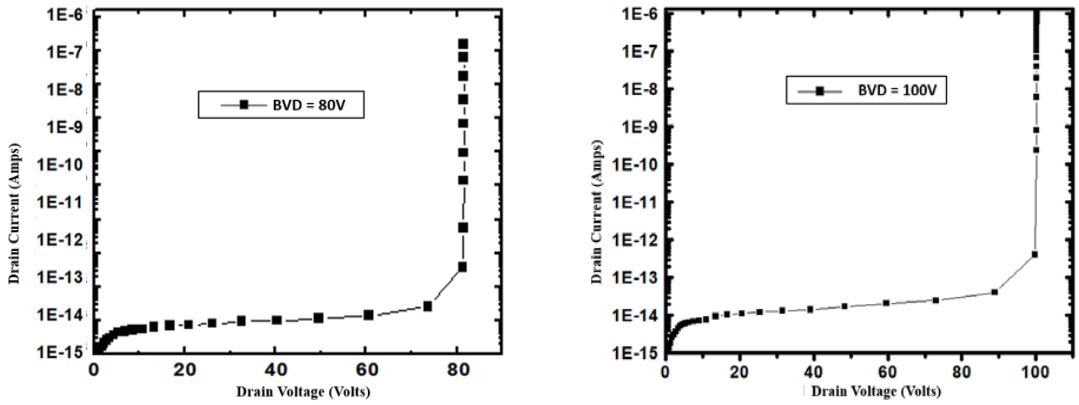
To obtain the desired trade-off between the breakdown voltage and the specific on-state resistance, the linear p-top mask condition has been varied. The main purpose of the linear p-top in the device is to minimize the on-state resistance while reaching the desired breakdown voltages of more than 80 and 100 V. Figure 2(b) shows the 3D simulation structure (top view) with different cut lines. C1 and C3 are the cut lines near the side isolation and C2 is in the middle, over the p-top region. Figures 3(a) and 3(b) show the impact ionization curves for different cut lines at different points in the devices for the proposed 80 and 100 V NLDMOS structures, respectively. The impact ionization point moved towards the drain side due to gate contact field plate extension. The impact ionization peak near the gate decreased and spread towards the drain side. The SOA performance of the device was improved by PBL insertion. The dose and energy of the PBL were varied under various conditions to obtain better SOA characteristics.

From Figs. 4(a) and 4(b), it can be seen that the breakdown voltages of both device structures are more than 80 and 100 V, respectively. The leakage current of the proposed structure is very low.



(a) (b)

Fig. 3. (Color online) Surface impact ionization distributions of proposed (a) 80 and (b) 100 V NLDMOS unit cells.

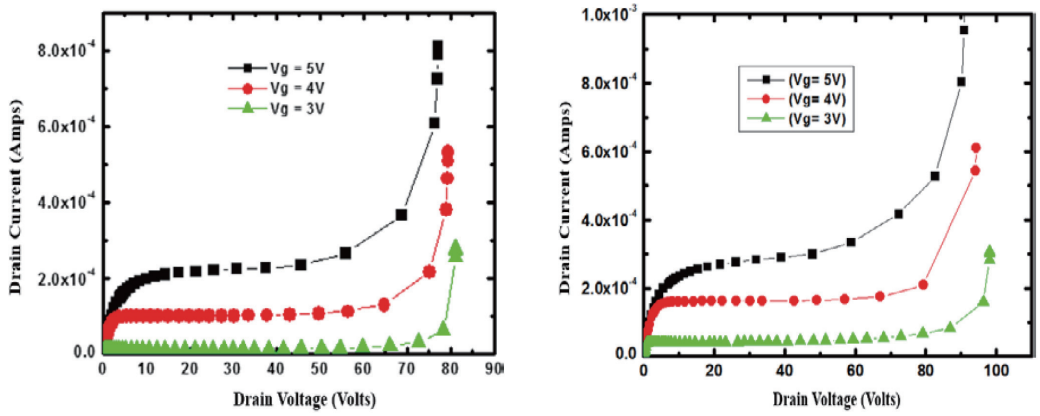


(a) (b)

Fig. 4. Breakdown curves for proposed (a) 80 and (b) 100 V NLDMOS unit cells.

In Figs. 5(a) and 5(b), the on-state breakdown voltages of the proposed NLDMOS devices are shown, indicating a good trade-off between the on-state breakdown voltage and the off-state breakdown voltage. PBL insertion has a considerable impact on SOA performance. Without the PBL, saturation and the Kirk effect were observed in SOA performance, which is optimized by inserting the PBL and varying the dose and energy of the PBL.

The on-state resistances of the proposed 80 and 100 V structures are 50.8 and 78.6 mΩ·mm^2, respectively, which are lower than the previously proposed 0.13, 0.18, and 0.25 μm technologies in Fig. 6. These structures can be extended up to 120 V with some optimization.



(a) (b)

Fig. 5. (Color online) SOA curve for proposed (a) 80 and (b) 100 V NLDMOS unit cells.

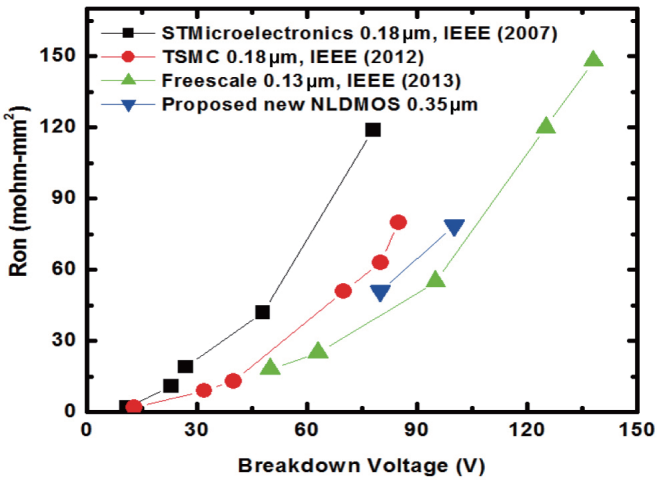


Fig. 6. (Color online) Comparison of benchmark off-state breakdown vs on-state resistance (R_{on}) for different technologies.

4. Conclusions

The device structure developed in this study is very competitive in achieving the desired breakdown voltage and benchmark on-state resistance and, additionally, we have proven it to have a better SOA performance. This device structure has a better impact ionization, so it will maintain the hot carrier reliability better. We believe that this device structure can be used for future autoelectronics industries and applications.

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