

CMOS-MEMS Resonators and Oscillators: A Review

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In this paper, we summarize research activities and technological progress in the field of current CMOS-MEMS resonators and oscillators for portable sensor node and timing applications. By employing CMOS-based fabrication technologies, we can monolithically integrate MEMS devices and their associated application-specific integrated circuits (ASICs), thereby enhancing their overall performance as compared with their stand-alone counterparts. Owing to the diversity of post-CMOS processing techniques, in this review, we mainly focus on the devices achieved by so-called foundry-orientated CMOS-MEMS platforms. On the basis of how the mechanical structure is achieved, in the paper we focus on two major strategies: (i) additive back-end-of-line (BEOL) compatible layers and (ii) machining of standard CMOS layers for device fabrication. Given their superior CMOS integration capability, the circuitry design concepts, testing results, and potential merits of state-of-the-art CMOS-MEMS oscillators are also presented.

1. Introduction

Nowadays, owing to the increasing demand for the interaction between physical objects and the real world, MEMS-based subsystems with versatile functionality are now widely adopted in most Internet of Things (IoT) and wireless sensor network (WSN) applications.⁽¹⁾ IoT was coined in 1999 to describe the communication between versatile sensor nodes using modern wireless technology, later facilitating smart living for humans. Toward the goal of smart living, machine-to-machine communication (M2M) technology attracts significant attention for developing emerging IoT systems in different domains, including: consumer electronics, automotive safety, transportation system, energy grids, and healthcare facilities. To satisfy the requirement of the aforementioned applications, mechanical resonators usually serve as an essential element for frequency selection (i.e., filter),⁽²⁾ timing (i.e., oscillator),⁽³⁾ and inertial detection (i.e., gyroscope),⁽⁴⁾ as well as mass/chemical sensing^(5,6) purposes. Considering data communication, off-chip mechanical transducers, such as quartz, ceramic, and surface acoustic

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wave (SAW) devices, have been commonly used in front-end systems to provide the promising features of excellent power handling and reasonable Q -factor for frequency control and signal conditioning over the past couple of decades. As a viable alternative, MEMS-based vibrating devices take advantage of lower cost and smaller form factor as compared with their bulky conventional counterparts, thanks to the rapidly revolutionized and matured microfabrication technology in recent years.⁽⁷⁾

In particular, to not only attain a comprehensively functional system for communication between analog and digital domains⁽⁸⁾ but also meet the requirement for vacuum-sealed conditions,⁽⁹⁾ the potential methodologies of a reliable IC-compatible integrated platform have fueled substantial debate and been thoroughly explored in vibrating MEMS applications. Figure 1 depicts two major strategies to combine MEMS structures and customized application-specific integrated circuits (ASICs), known as (i) System in Package (SiP) and (ii) System-on-Chip (SoC) methods. The SiP solution is available to bridge mechanical components and associated interfaces through wafer- or chip-level bonding techniques [e.g., through silicon via (TSV) and wire interconnection], thus accomplishing a complete system with the necessary functionality. From the requirement of system specification, this hybrid multichip approach allows the optimal design of the CMOS circuitry and MEMS devices using the appropriate and individual technology node.⁽¹⁰⁾ One of the most prominent products in the current consumer market is the MEMS-based programmable oscillator implemented by SiTime Inc. in which the proprietary “MEMS-First” two-chip solution is used to integrate epi-sealed MEMS and CMOS circuitry together.⁽¹¹⁾ Even if the hybrid approach is a mainstream strategy from the commercial viewpoint owing to its high accessibility and flexibility for most MEMS designers and manufacturers, the nature of considerable bonding parasitics and cost for MEMS combo

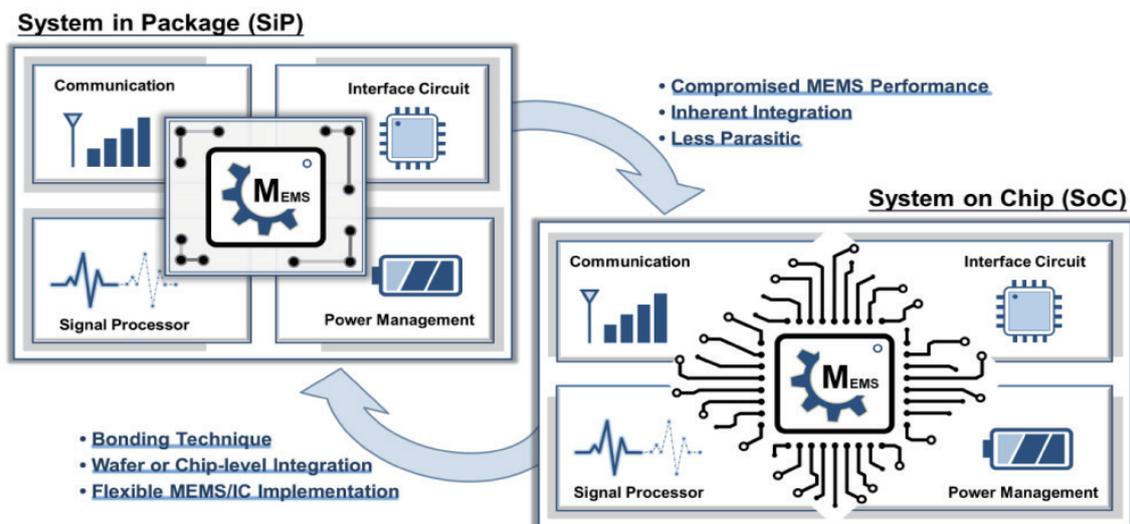


Fig. 1. (Color online) Mainstream strategies for integration of MEMS subsystem and its associated IC, including (i) SiP and (ii) SoC approaches.

integration become the main challenges toward future wearable/IoT implementation. On the other hand, the SoC approach provides a generic solution to monolithically integrate the overall system by cofabricating MEMS and IC on the same substrate. As a consequence, this monolithic approach offers several merits, including fewer capacitance paths (i.e., undesired parasitics), smaller footprint, fast prototyping, and turnaround time only at the cost of restricted material properties and dedicated foundry sources. With respect to the sequence of MEMS fabrication, the CMOS-MEMS technologies, referred to as the pure monolithic approach in this paper, can be categorized as pre-CMOS, intra-CMOS, and post-CMOS.^(12–14) Among these diverse CMOS-MEMS processes, in this review, we emphasize the domain of post-CMOS implementations, especially for vibrating MEMS resonators, in order to deeply investigate and evaluate the capability and possibility of foundry-orientated solutions toward practical frequency sensing, generation, and selection applications. In this manner, this paper covers various post-CMOS approaches and is divided into four main sections. In the first part, the process with additive back-end-of-line (BEOL)-compatible layers and relevant research results are presented under the thermal budget limitation of CMOS interconnect. In the second and third parts, the states-of-the-art are sorted by various CMOS-BEOL machining technologies (i.e., maskless postprocess), showing their own features and advantages. The prevalent circuitry design, comparison for oscillator application, and frequency stability regarding the pure monolithic approach are presented in the last section.

2. CMOS-MEMS Technologies

The CMOS-MEMS solution is currently treated as an ultimate goal toward the smart integrated system of the future by cofabricating many building blocks on a single chip, such as sensors, actuators, and interface circuits on the same chip.^(15,16) In this technology, the monolithic MEMS platform can be categorized into three different types according to its postfabrication sequence. Considering the subsequent thermal budget of CMOS electronics, the pre-CMOS (so-called “MEMS-first”) and intra-CMOS platforms were developed in the early 1990s. From the process-flow perspective, the typical pre-CMOS needs to overcome several process challenges toward practical implementation, such as the (i) surface planarization of the following CMOS circuitry and (ii) reluctance to deal with the MEMS prefabricated wafer in the standard CMOS line owing to contamination. As a demonstration of pre-CMOS integration, the SOI CMOS-MEMS platform has recently been proposed to address the planarization issue.⁽¹⁷⁾ A hybrid e-beam/deep ultraviolet (DUV) lithography is implemented to facilitate the wiring of NEMS structures, resulting in a compact and functional nanosystem for physical sensing applications.⁽¹⁸⁾ On the other hand, the intra-CMOS MEMS approach addresses these issues by a dedicated MEMS manufacturer but it still suffers from the additional cost associated with such a complicated, intertwined postprocess. Therefore, post-CMOS manufacturing becomes an attractive solution and will be specially emphasized in this article. According to the structural materials of MEMS devices, two major approaches are mentioned in the following paragraph, including post-CMOS fabrication based on (i) additive BEOL-compatible layers and (ii) existing standard CMOS layers. In contrast to the pre- or intra-CMOS MEMS, the conventional

CMOS circuits are firstly formed in post-CMOS technology, followed by a MEMS process to attain MEMS-above-IC monolithic integration. In this regard, the post-CMOS MEMS is a method amenable to most universities and academic researchers because of the independence of IC and MEMS portions. In other words, the standardization of the CMOS process portion allows design flexibility and accessibility in the selection of the CMOS foundry as well as the technology node depending on system requirement and cost.

2.1 Post-CMOS fabrication based on BEOL-compatible layers

To simultaneously attain monolithic integration and circumvent the thermal budget limitation, the post-CMOS technology has been employed for many years. The Digital Micromirror Device (DMD),⁽¹⁹⁾ a well-known display element developed by Texas Instruments (TI), is exemplary in this category.

For state-of-the-art vibrating MEMS, in the same manner, the refractory metallization and low-temperature structure deposition are commonly utilized to accommodate the required on-chip integration. For instance, to raise the limitation of the CMOS thermal budget, a monolithic oscillator using a high- Q poly-Si resonator has been demonstrated⁽²⁰⁾ where the low-resistance CMOS interconnection realized by tungsten (W) metal is used to withstand high-temperature annealing during MEMS fabrication. In the structural aspect, the poly-SiGe provides several promising material properties for the MEMS process while the poly-Ge serves as a sacrificial material. Instead of poly-Si, the doped, low-resistive poly-SiGe structure promises a comparable Q -factor and low-temperature deposition on the CMOS chip.⁽²¹⁾ Moreover, this design strategy is particularly useful for a low-power oven system because of the low thermal conductivity realized by the poly-SiGe material.⁽²²⁾ As a potential alternative, the materials tabulated in Table 1, such as SiON,⁽²³⁾ nickel,⁽²⁴⁾ and SiC,^(25,26) also possess low-temperature (<300 °C) manufacturing capability to realize an add-on MEMS resonant body. Pursuant to the reduction in considerable loss commonly seen in capacitive transduction, the AlN via piezoelectric transduction provides an efficient solution for a BEOL-compatible structure as demonstrated by Sandia National Laboratories (SNL).⁽²⁷⁾ On the basis of SNL's 0.35 μm CMOS on SOI process, the fully integrated piezo-MEMS oscillators, centered at 20/80 and 100 MHz, were reported with a feedthrough cancellation scheme. By virtually removing the undesired feedthrough path through an additional dummy device, the clear transition of the frequency response can be observed in both high frequency (HF) and very high frequency (VHF) ranges, thereby showing a decent close-in phase noise for timing application.

A similar concept has also been adopted in standard CMOS technology. Through SiTerra MEMS on CMOS process, a modified CMOS-MEMS platform presents a possibility to enable ultrahigh frequency (UHF) thin-film surface acoustic wave resonator (TFSAW) and bulk acoustic wave resonator (TFBAW) with a zero-level vacuum package over conventional ceramic, metal, and plastic methods.⁽²⁸⁾ As a proof of concept, although the spurious signals near the main resonance are still problematic, the released 4.6 GHz TFBAW structure exhibits the highest fQ product of 10.5×10^{12} in CMOS-MEMS technology to date. This MEMS release approach has also been transferred to capacitive transduction.⁽²⁹⁾ By removing the sacrificial polymer, a capacitive CMOS-MEMS resonator with a 25 nm transduced gap is successfully

Table 1
Representative CMOS-MEMS resonators realized by additive BEOL-compatible layers.

Reference	Representative Post-CMOS Resonators Machined by BEOL-compatible Layers						
	Affiliation (IC Manufacturer)	Gap/Cavity Sacrificial Layer	Structure Material	Device Motion	Resonant Frequency	Q-factor	Comment
C. T.-C. Nguyen, <i>et al.</i> , 1999 ⁽²⁰⁾	UC-Berkeley (BSAC)	Phosphosilicate glass (PSG)	P-doped polysilicon	Lateral comb	18.83 kHz	51000 (20 mTorr) 80000 (< 20 mTorr)	· Tungsten interconnect with TiSi ₂ contact barriers for consideration of thermal budget
A. E. Franke, <i>et al.</i> , 1999 ⁽²¹⁾	UC-Berkeley (BSAC)	Poly-Ge	p+ Poly-SiGe	Lateral comb	32.479 kHz	30000 45 (Air)	· Individual chip anneal of 550 °C is used to lower the resistivity of the poly-Ge film
S. Pacheco, <i>et al.</i> , 2006 ⁽²³⁾	Freescale Semiconductor	Polymethylglutarimide (PMGI)	TaN & SiON	Vertical CCB	11.278 MHz	2200	· 100 nm transduced gap · CMOS back-end compatible low temperature process
W.-L. Huang, <i>et al.</i> , 2008 ⁽²⁴⁾	UC-Berkeley (TSMC)	Parylene-C	Nickel	Flexural disk-array	11.7 MHz	1651	· 100 nm transduced gap · Overall post-fabrication steps never exceed 50 °C
F. Nabki, <i>et al.</i> , 2009 ⁽²⁵⁾	McGill University (CMC Microsystems)	Oxide	SiC	Vertical CCB	11.6 MHz.	1600	· Improved MEMS process enables deposition of a-SiC at low temperatures (<300 °C)
K. E. Wojciechowski, <i>et al.</i> , 2009 ⁽²⁷⁾	Sandia National Laboratories	Silicon	AlN	Extensional BAW	100 MHz	1257	· First fully released contour mode AlN microresonators integrated above CMOS ICs
R. Jansen, <i>et al.</i> , 2011 ⁽²²⁾	IMEC	Oxide	Poly-SiGe	Extensional BAW	24 MHz	24000	· Capable of low-power oven system due to the low thermal conductivity of SiGe
L. Huang, <i>et al.</i> , 2015 ⁽²⁶⁾	Princeton University (IBM)	Al	n+ a-SiC	Vertical CCB	2.89 MHz	362	· MEMS structure deposited by PECVD at a maximum temperature of 175 °C
A. Uranga, <i>et al.</i> , 2015 ⁽²⁹⁾	UAB (Silterra)	Polymer	BiMetallic nitride	Torsional paddle	24.5 MHz	~1500	· Achieve vertical gaps of 25 nm · MEMS above IC's with zero-level vacuum package
M. Soundara Pandian, <i>et al.</i> , 2016 ⁽²⁸⁾	UAB (Silterra)	N/A (for SAW) Polymer (for BAW)	AlN	TFSAW TFBAW	302 MHz 2.36 GHz	>3000 (TFSAW) 446 (TFBAW)	· Capable of nonplanar piezoelectric thin-film device · MEMS above IC's with zero-level vacuum package

achieved via SilTerra 0.18 μm commercial CMOS technology. While reducing the motional impedance via the nanogap implemented in this work, the phase noise (PN) floor of -120 dBc/Hz was reported to facilitate reconfigurable oscillation in dual mode.

2.2 Oxide-removal postfabrication approach

In contrast to post-machining additive BEOL-compatible layers as described in the previous section, CMOS-MEMS structures can be created using BEOL layers existing in the standard

CMOS technology, including interconnect-metal, gate/resistance polysilicon, and interlayer dielectric.^(30,31) In comparison with the aforementioned approach, it is widely accepted that CMOS layer machining allows lower fabrication cost and faster lead time by removing the additional masks and lithography steps for MEMS fabrication. Figure 2 depicts the detailed cross sections of 0.35 and 0.18 μm CMOS processes showing that the advanced technology node possesses more BEOL layers for flexible selection on routing and MEMS structure material. To fabricate CMOS-MEMS devices, intuitively, the oxide-removal approach serves as a viable solution to create metal-rich structures.

As illustrated in Fig. 3 with a chip cross-sectional view of 0.35 μm CMOS node, the maskless oxide postrelease process is very simple by using the buffer HF solution to remove the exposed sacrificial dielectric. By doing so, the versatile motion dimension (e.g., in- or out-of-plane), mechanical boundary (e.g., pin-pin, free-free, and clamped-clamped), and structure composition (e.g., pure metal, metal/oxide composite) can be conducted to achieve greater design flexibility.^(32,33) The SEM images of practical capacitive resonators reported in our previous research works are also provided. However, in such standard CMOS technology, the capacitive transduction often suffers from limited electromechanical coupling (η_e) because of the restricted and mandatory design rule corresponding to CMOS layer patterning. As referred to in Fig. 2, the minimal feature size for oxide release platform is 0.5 μm in the lateral direction which leads to the motional impedance (R_m) of capacitive transducers laid in the $\text{M}\Omega$ region. To relieve such considerable loss for practical application, one can transfer the etching approach into an advanced technology node (i.e., 0.18 μm) in which the minimal lateral spacing of the sacrificial oxide is 0.28 μm , as indicated in Fig. 2. In this manner, the dc-bias for capacitive operation can be reduced, thanks to the smaller feature size and greater transduction area via 6 metal stacking. To further shrink down the effective gap for capacitive resonators, the gap reduction method based on the well-studied pull-in behavior was proposed in our prior work.

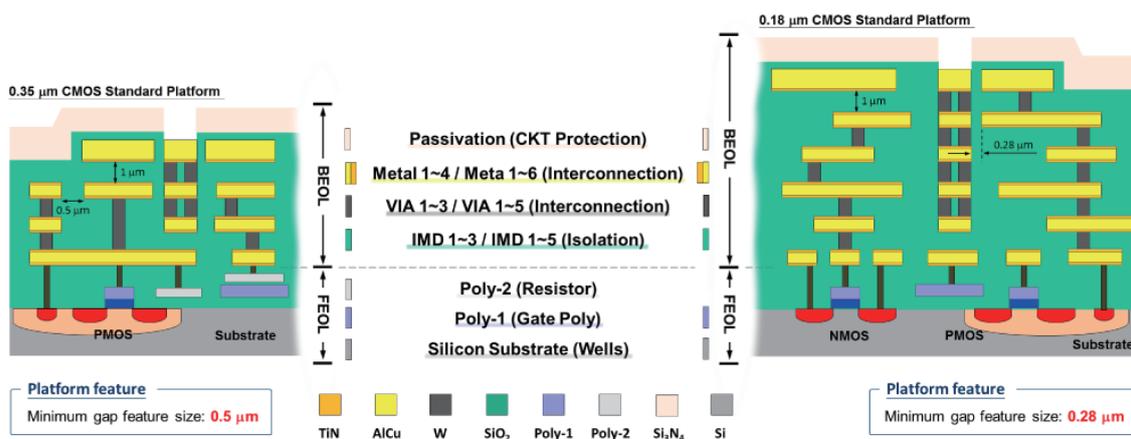


Fig. 2. (Color online) Cross-section view of unreleased CMOS-MEMS chip realized in 0.35 μm (2P4M) and 0.18 μm (1P6M) CMOS technology, showing a specific stacking configuration and an inherent monolithic capability.

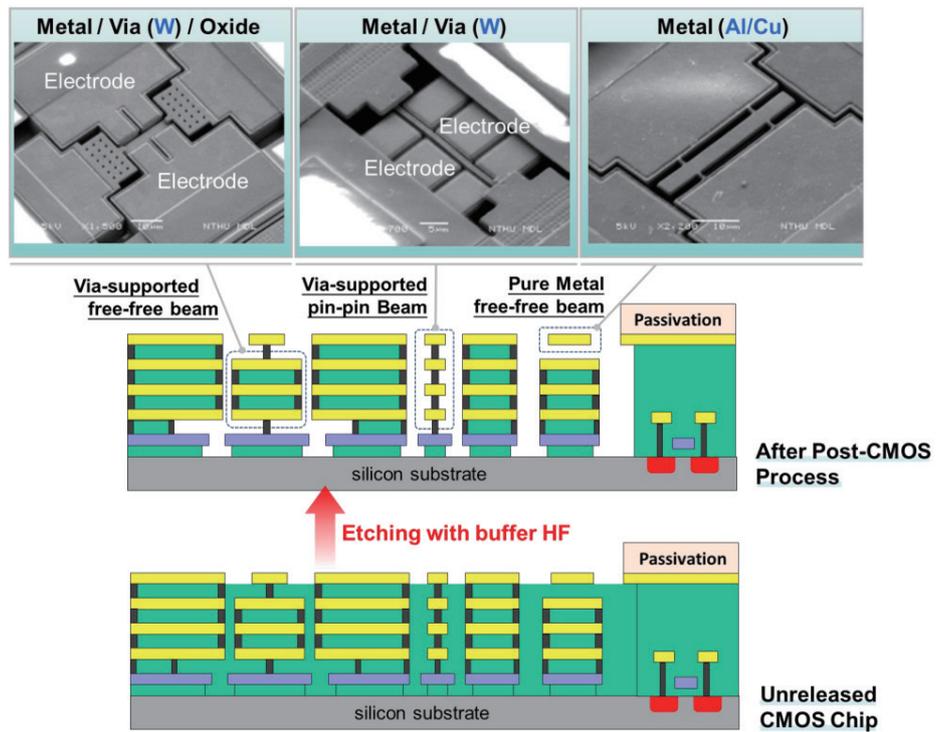


Fig. 3. (Color online) Postprocess flow of various CMOS-MEMS resonators realized by standard 0.35 μm 2P4M CMOS technology with oxide-removal approach.

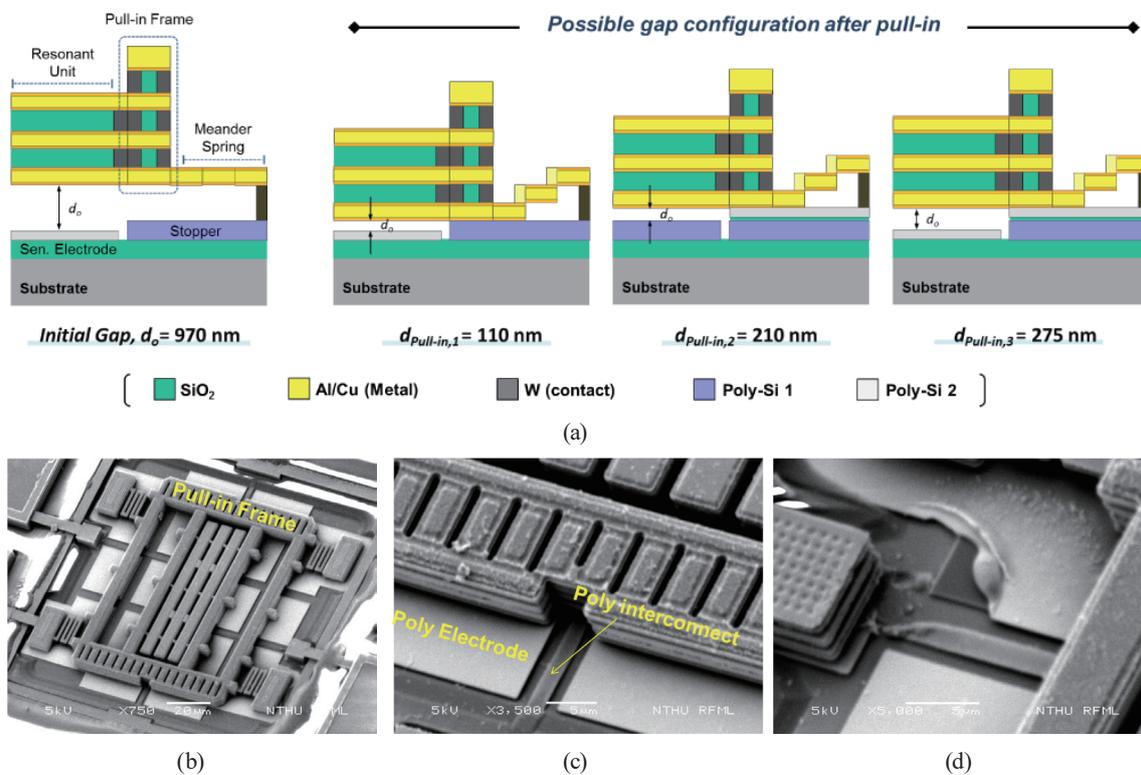


Fig. 4. (Color online) (a) Manifold gap configurations in 2-poly CMOS technology node while the pull-in method is carried out. SEM images of (b) CMOS-MEMS resonator with pull-in frame, (c) suspended poly-Si interconnect magnified view, and (d) failure structure caused by an undesired undercut.

Figure 4(a) shows comprehensive gap configurations depending on different combinations of two distinct poly-Si layers (i.e., poly-1 and poly-2) existing in 0.35 μm 2P4M CMOS node when the electrostatic pull-in effect is induced.^(36,37) Apart from the special structure design, a submicron gap of 40 nm, the smallest spacing among existing CMOS BEOL layers, can be realized by removing the inter-poly oxide where poly-1 and poly-2 are tightly arranged.⁽³⁸⁾ However, from the process point of view, although the oxide-removal postfabrication has been used with some success [as referred to in Fig. 4(b)], this time-controlled wet etching process still places a bottleneck on device yield. Apparently, the embedded polysilicon interconnect and electrodes are suspended owing to severe undercut, as shown in Fig. 4(c), thus reducing the mechanical robustness for such a region. Consequently, Fig. 4(d) indicates that an undesired undercut is the primary cause of the low yield in the postfabrication of MEMS devices during or after release.

In addition to wet etching, the oxide dry release approach implemented by dielectric RIE serves as a promising solution, which resolves not only the unwanted undercut within the release window but also the considerable curling of suspended thin-film structures. From this concept, the CMOS substrate silicon can be involved in MEMS structures by an additional backside etching.⁽³⁹⁾ Thanks to the remaining single-crystal silicon patterned by deep reactive-ion etching (DRIE), the transduction area and stiffness of in-plane motion MEMS structures are markedly enhanced, thereby alleviating the possible loss and curling issue encountered in a conventional motion sensor.⁽⁴⁰⁾ Moreover, owing to the benefit from the inherent high-quality nature offered by single-crystal silicon, such a CMOS-MEMS resonator possesses a sufficient Q characteristic in the frequency domain. In agreement with this concept, a multiuser multichip SOI CMOS-MEMS process has been demonstrated with MEMS-last manner.⁽⁴¹⁾ Note that the dry-etching release process can result in a higher CMOS-MEMS yield and lead to a much easier standardization from the process aspect, which implies that CMOS-MEMS monolithic systems can be accomplished independently by a commercial CMOS foundry without any in-house release process.⁽⁴²⁾

2.3 Metal-removal postfabrication approach

To again address the undesired undercut issue caused by the above-mentioned time-based oxide wet etching Postprocess, the metal-removal wet etching process, as an appropriate solution, is widely used for CMOS-MEMS transducers.⁽⁴³⁾ The fundamental fabrication flow can be seen in Fig. 5(a). It begins with a prepared CMOS-MEMS chip where the exposed sacrificial metal layer is etched to form an oxide-rich MEMS structure through the etchant containing heated sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). Then, the probing pads for device testing are opened via reactive ion etch (RIE). It is worth saying that this maskless etching process features satisfactory etching selectivity between the metal and the dielectric material, resulting in nearly 100% device yield for both 0.35 μm 2P4M⁽⁴⁴⁾ and 0.18 μm 1P6M⁽⁴⁵⁾ standard processes.

From the material point of view, the CMOS-MEMS composite structure with oxide-rich feature enables the low-loss characteristic since the high intrinsic Q (i.e., Q_{material}) nature is provided by the oxide layer. In our previous research, the improvement of mechanical Q -factor

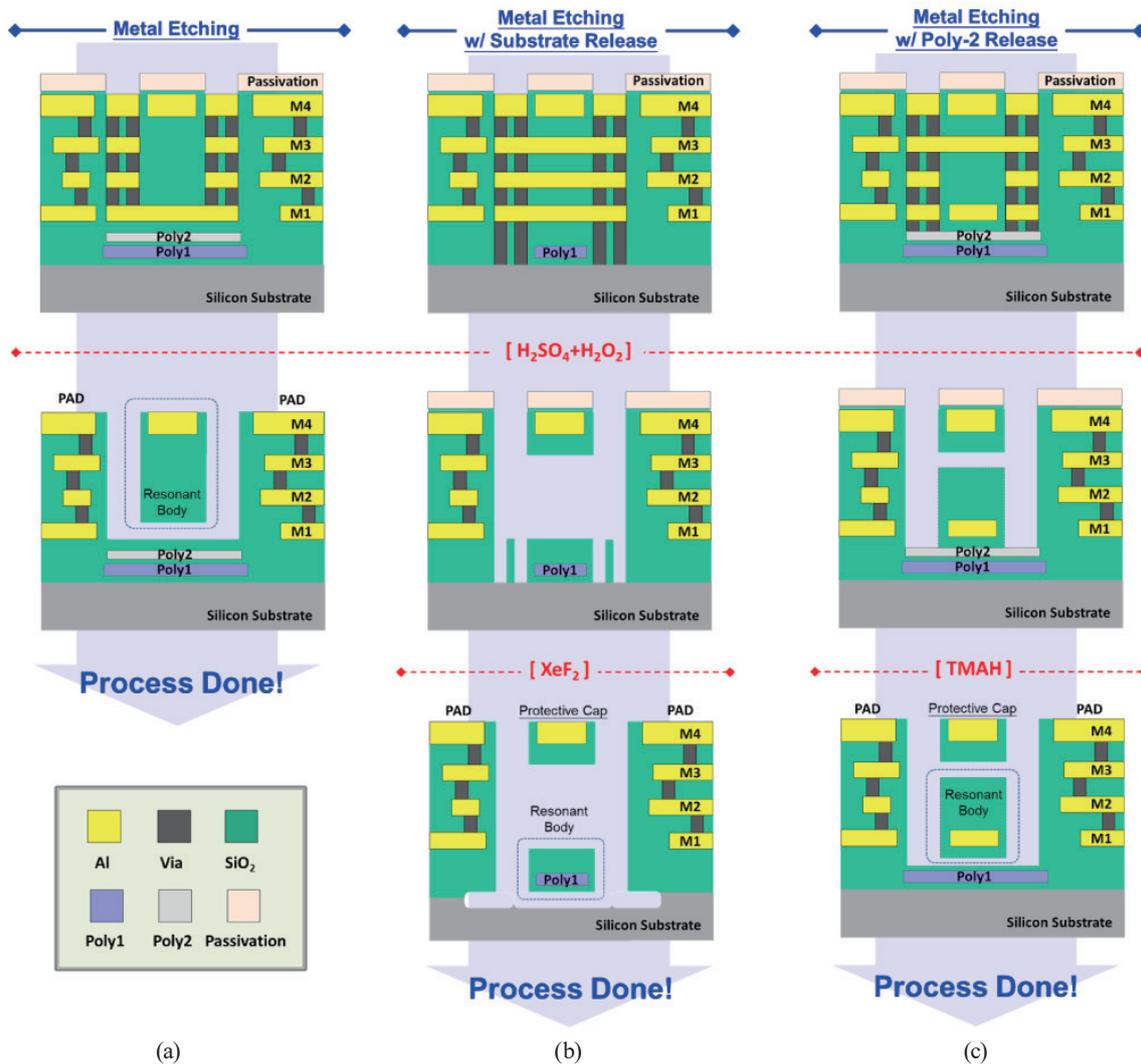


Fig. 5. (Color online) Comprehensive postprocess flows of oxide-rich devices, including (a) general metal etching, modified metal etching with (b) Si substrate release, and (c) poly-2 layer release.

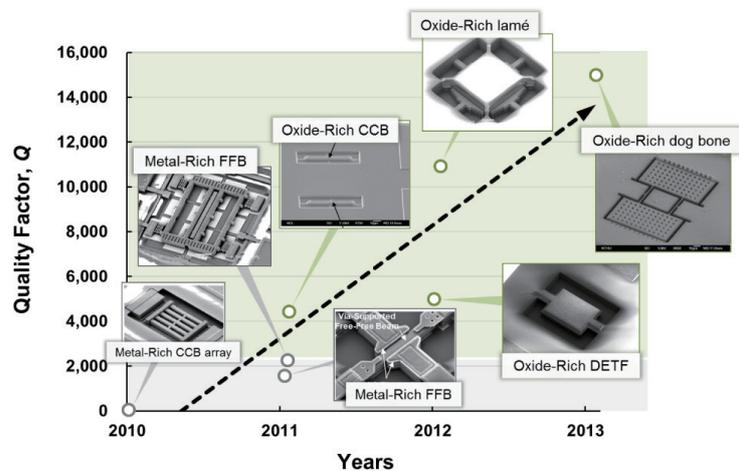


Fig. 6. (Color online) Breakthrough on Q -factor of CMOS-MEMS resonators, which is dominated by the amount of constituent BEOL oxide.

has been made through different post-CMOS processes, as shown in Fig. 6. It is clear that the use of oxide-rich stacking together with bulk-mode vibration anchored in nodal points⁽⁴⁶⁾ can easily attain a Q larger than 15000.⁽⁴⁷⁾ Apart from the Q enhancement, the BEOL silicon dioxide is generally considered as key for passive temperature compensation, thus further enhancing the frequency stability over a wide temperature range. In the common convention, the temperature coefficient of frequency (TC_f) of CMOS-MEMS composite resonators is highly related to their own material selection and arrangement. This characteristic is utilized to manipulate the frequency variation versus environmental temperature,⁽⁴⁸⁾ given by

$$TC_f = \frac{TC_{f,mat1} + \gamma TC_{f,mat2}}{1 + \gamma}, \quad \gamma = \frac{E_{mat2} I_{mat2}}{E_{mat1} I_{mat1}}, \quad (1)$$

where I and E represent the moment of inertia and Young's modulus of associated materials used in the resonant structure, respectively. Consequently, the temperature–frequency dependence is evidently validated by TC_f comparison illustrated in Fig. 7 in terms of distinct oxide composition, indicating that the increased silicon dioxide portion with positive temperature dependence (TC_f) is capable of engineering the thermal stability of such oxide-coating vibrating components.

Depending on the released region defined by designers, the standard polysilicon layer can be included to serve as part of the mechanical structure after the modified metal-removal post-CMOS process, as depicted in Fig. 5(b). Thanks to the sufficiently high thermal expansion and piezoresistance coefficients (i.e., α and π), the thermal driving and piezoresistive sensing mechanism are also widely studied in CMOS-MEMS technology.^(49–52) To alleviate the

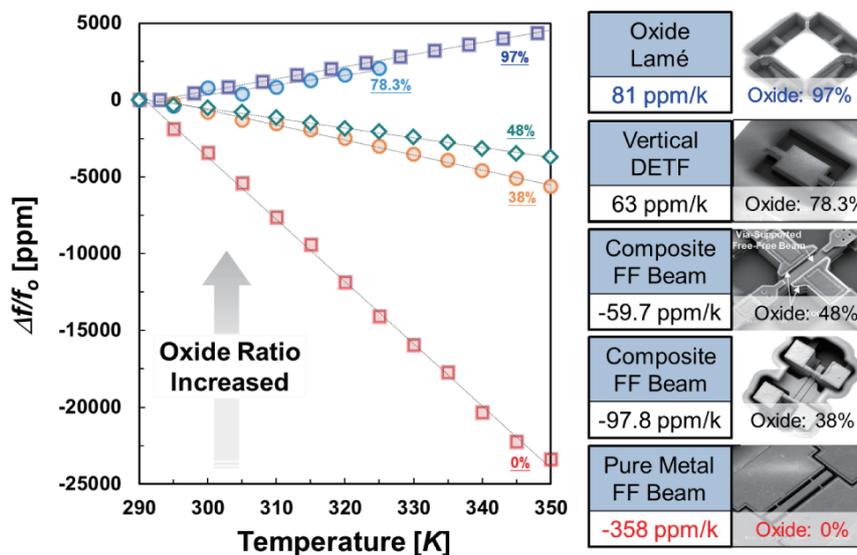


Fig. 7. (Color online) Comparison of thermal stabilities of various CMOS-MEMS resonators, exhibiting the dependence between the oxide ratio and the associated TC_f value.

problematic feedthrough signal caused by low structural resistance, the CMOS-MEMS II-BAR array realized by an oxide-coated polysilicon with differential topology is adopted to create a 38 dB reduction on background feedthrough.⁽⁵⁰⁾ By taking advantage of two available polysilicon layers in 0.35 μm 2P4M technology, the embedded poly-1 and poly-2 are designated as actuator and sensor, respectively, in our previous work.⁽⁵¹⁾ Thereby, one can fully decouple the actuating and sensing sectors to avoid the resistive feedthrough existing in conventional thermal-piezoresistive resonators (TPRs). Note that the flexible routing of standard CMOS technology enables the low thermal capacitance (C_{th}) feature for a TPR-based sensor, thus greatly enhancing not only transduction efficiency but also detection sensitivity, which paves the way toward future MEMS particulate matter (PM) sensors for air pollution detection.⁽⁵²⁾

2.4 Metal-removal-based poly-2 etching approach

Benefitting from the high accessibility and excellent etching selectivity, the aforementioned CMOS-MEMS metal-removal process (e.g., oxide-rich structure) demonstrates the acceptable frequency stability and repeatability^(53,54) in the same batch for timing and sensing application. Although the process steps are very simple, the motion impedance (R_m) usually lies in the $\text{M}\Omega$ level owing to a 1 μm effective gap spacing. To overcome this considerable loss, an advanced two-step poly-2 etching process is proposed for strong coupling by creating a deep submicron gap.⁽⁵⁵⁾ As referred to in Fig. 5(c), similar to the generic metal-releasing process, the postfabrication starts from metal wet-etching through a mixture of H_2SO_4 and H_2O_2 to remove the sacrificial metal. The sacrificial polysilicon layer (poly-2) in 0.35 μm 2P4M technology is then released by tetramethylammonium hydroxide (TMAH) solution, hence providing a tiny air-gap spacing of only 180 nm. In the final step, oxide RIE is again employed to etch the top Si_3N_4 passivation layer for aluminum pad opening.

Figure 8 reveals several representative cross sections of a metal-removal-based approach. By creating the 297 nm effective gap (i.e., metal-to-polysilicon gap configuration) through a poly-2 etching process, the capacitive R_m can be greatly reduced by 140 times compared with the conventional metal-removal approach described in the previous section, thus facilitating the implementation of monolithic timing⁽⁵⁶⁾ and filtering⁽⁵⁷⁾ building blocks. To further suppress the R_m value of the metal-to-polysilicon gap design, the contact array design is a feasible alternative capable of gap reduction without any special structure design (e.g., pull-in frame) based on the poly-2 releasing approach. With the intensive pillar array of tungsten contact defined by computer-aided design (CAD) tool, the contact-array-assisted gap⁽⁵⁸⁾ can contribute an additional sixfold reduction in motional impedance by means of only a 190 nm equivalent gap. Under the dc bias of 30 V, the comparison of measured R_m shown in Fig. 8(b) shows good agreement with formula predictions. Here, the slight discrepancy between experimental data and analytic result mainly comes from the reduced transduction area implemented in contact-array design owing to the fabrication limitation of the standard CMOS process. Note that the inset SEM image provides the FIB view for both contact-array-assisted and metal-to-polysilicon gaps, showing the different resonant body compositions as well as electrode-to-resonator gaps.

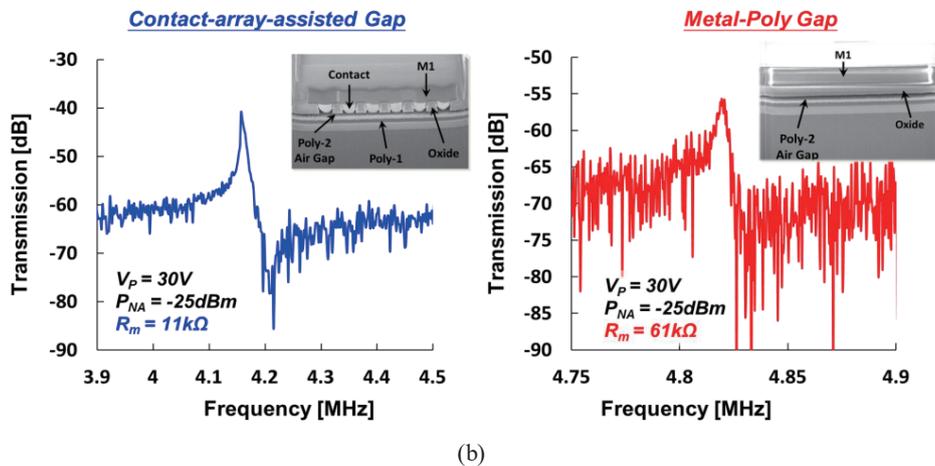
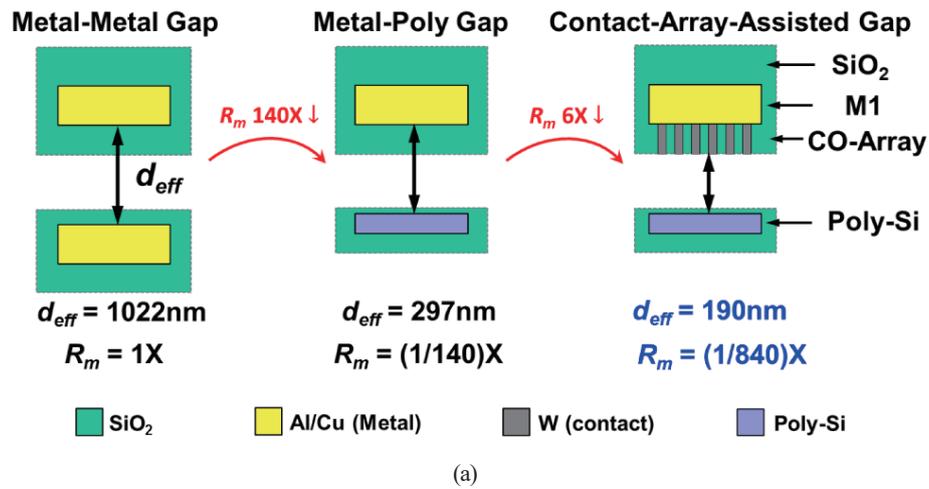


Fig. 8. (Color online) (a) Prediction of reduced capacitive motional impedance with effective gaps of 1 μm , 297 nm, and 190 nm, (b) frequency spectrum under different gap configurations based on ploy-2 release process, showing an obvious improvement of R_m via contact-array-assisted design.

2.5 TiN-C CMOS-MEMS platform

On the basis of metal-released postfabrication, although the oxide-rich feature can address most of the issues existing in metal-rich counterparts for resonant application, such as Q -factor and device yield, the remaining dielectric charging issue is perceived as a major challenge for capacitive MEMS resonators. By relying on the positive TC_f value, the dielectric coating layer (e.g., silicon dioxide) can effectively engineer the TC_f for pure silicon devices as shown in prior work.⁽⁵⁹⁾ However, the induced charge will accumulate and be trapped in the intergap dielectric layer while a dc bias is applied for capacitive transduction. In this manner, the undesired charge behavior will significantly affect the electrostatic spring constant (k_e) and cause the frequency drift on device resonant frequency.

In the current CMOS-MEMS technology, which is limited by the fixed stacking material configuration from the standard platform, especially for such oxide-rich resonators, the charge

issue becomes problematic in terms of frequency stability.⁽⁶⁰⁾ Therefore, a novel post-CMOS fabrication process, so-called TiN-C CMOS-MEMS platform,⁽⁶¹⁾ is established by removing the AlCu metal core and preserving the TiN layers as electrodes. By doing so, one can simultaneously attain decent electromechanical coupling and charge elimination for capacitive transduction.

To achieve a TiN-C (i.e., TiN composite) structure, Fig. 9 illustrates the proposed post-CMOS process in considerable detail. First, the structure profile is defined by removing the metal sacrificial layers. Next, the exposed dielectric and TiN materials are then etched away by oxide and metal RIE processes, respectively. After the dry etching process, a commercial Al etchant is used to remove the AlCu metal core of the CMOS interconnect for MEMS structure release. Finally, a two-step RIE process is again adopted to open the probing pad region for the following device testing. From the cross-sectional SEM image, a proposed TiN-C free-free beam (FFB) resonator is successfully fabricated where the oxide fin structure provides the electrical isolation capability for multiport operation. Moreover, the AlCu etching step can

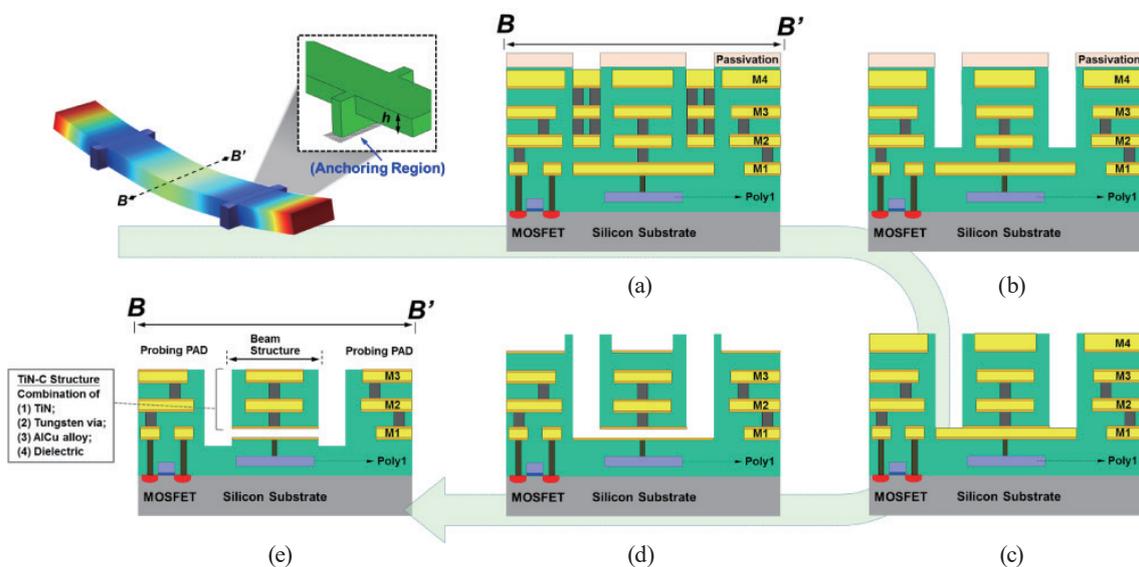


Fig. 9. (Color online) Full postfabrication process for TiN-C CMOS-MEMS platform: (a) unreleased CMOS-MEMS chip, (b) metal wet etching process for structure definition, (c) dry released process for removing the exposed oxide and TiN layers, (d) structure released by Al etchant, and (e) probing pad opening by two-step RIE processes.

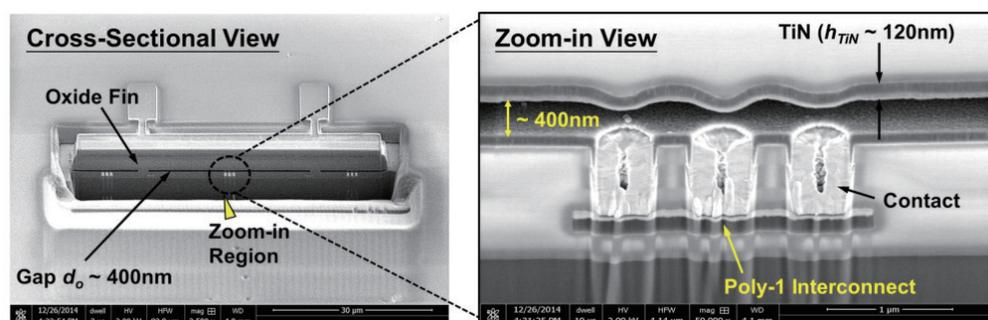


Fig. 10. (Color online) SEM image of TiN-C FFB resonator, showing TiN parallel electrodes and a 400 nm transduced gap for capacitive transduction.

create a 400 nm transduction gap as shown in Fig. 10.

Figure 11 shows the measured results of frequency drift over time for both traditional oxide-rich and TiN-C resonators. To investigate how the charge issue affects the resonant behavior of a capacitive transducer, the frequency spectra for the first 30 min are recorded. Apparently, there is no significant drift for the TiN-C FFB resonator. However, the oxide-rich double-ended tuning-fork (DETF)⁽⁶²⁾ shows more than 2000 ppm frequency deviation owing to the built-in voltage induced by inter-gap charge. On the other hand, for TC_f characteristics as shown in Fig. 12, unlike pure-metal FFB and oxide-rich Lamé mode resonators showing very negative and positive TC_f value, the TiN-C FFB resonator achieves the lowest TC_f for passive temperature compensation in CMOS-MEMS technology to date, thanks to the proper material selection.

Despite the restricted selection and physical property control (i.e., Young's modulus, residual stress, and so on) of the BEOL material, which places a main bottleneck in current monolithic CMOS-MEMS technology, it is confirmed that such platform technology that integrates “acoustic”, “mechanical”, and “electrical” domains would lead to a single-chip MEMS-based solution for

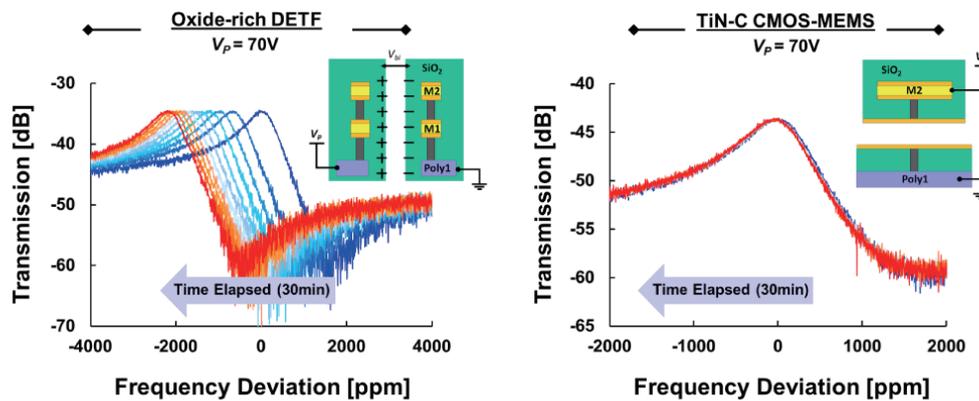


Fig. 11. (Color online) Measured results of frequency responses over time for traditional oxide-rich DETF and TiN-C.

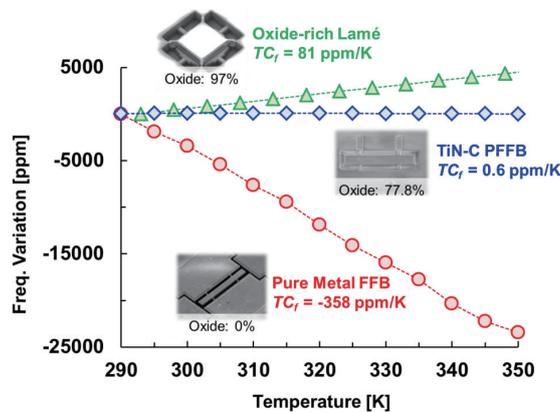


Fig. 12. (Color online) TC_f comparison among oxide-rich Lamé, pure-metal FFB, and TiN composite FFB resonators, showing distinct TC_f values owing to their different oxide compositions.

a signal processor in future wearable/IoT electronics. Table 2 summarizes the unique feature of various resonators realized by the foundry-orientated CMOS-MEMS platforms. Note that the tabulated prior arts are sorted on the basis of different postfabrication approaches of BEOL layers.

3. CMOS-MEMS Oscillator

One major application for CMOS-MEMS resonators is being a frequency-generating element as a closed-loop oscillator. In contrast to most crystal and FBAR oscillators^(71,72) that exploit the parallel resonance of the resonator using Pierce and Colpitts topologies, transimpedance amplifier (TIA)-based series resonant oscillators are commonly used in CMOS-MEMS technology to overcome the MΩ-scale motional impedance.⁽⁶²⁾ Figure 13 illustrates the conceptual schematic of a TIA-based oscillator, which is composed of three functional stages: (1) motional current to voltage conversion (I - V converter), (2) loop phase compensation, and (3) voltage amplification. Note that to save power and chip area, the phase compensators are not designed as a dedicated stage in most of the implementations. To meet the oscillation criterion, the overall transimpedance gain should be greater than the resonator impedance (typically in the kΩ to MΩ range), so a voltage amplifier is often added to relax the gain-bandwidth trade-off of the front-end TIA. Table 3 summarizes the published state-of-the-art CMOS-MEMS oscillators.^(62,73–79)

3.1 Selection of the TIA topology

TIA is the most critical block for series resonant CMOS-MEMS oscillators since it directly affects the phase noise and linearity. Recall the nonlinear phase noise expression in Lesson's form,⁽⁷³⁾

$$S_{PN}(f_m) = \frac{1}{2V_{OUT}^2} \left[4kTR_m + \frac{\overline{i_n^2}}{\Delta f} R_m^2 \right] \left[1 + \left(\frac{f_o}{2Q_L f_m} \right)^2 \right] + \frac{S_{fn}(f_m)}{f_m^2}, \quad (2)$$

where f_o is the oscillation frequency, R_m is the motional impedance of the resonator, $\overline{i_n^2}/\Delta f$ is the TIA input-referred current noise density, V_{OUT}^2 is the RMS output voltage swing, Q_L is the loaded quality factor, f_m is the offset frequency from the carrier, and S_{fn} is the frequency noise spectrum for describing the amplitude-to-phase noise conversion.⁽⁷³⁾ It is readily seen that the phase noise is proportional to $\overline{i_n^2}/\Delta f$ for a high- R_m resonator; therefore, a low-noise topology is desired for improving the phase noise. However, there exists a noise-bandwidth trade-off in a given CMOS technology; thus, the resonator's frequency would inherently affect the selection of the TIA topology.

Figure 14 illustrates the popular front-end TIA topologies that are widely adopted in CMOS-MEMS oscillators, and their gain, bandwidth, and input-referred noise expressions are summarized in Table 4. Apparently, the simplest TIA topology is a resistor directly connected to the resonator [cf. Fig. 14(a)] but it suffers the direct gain-bandwidth trade-off. The negative

Table 2
Comparison of CMOS-MEMS resonators with standard CMOS layer machining technique.

References	Representative CMOS-MEMS Resonant Transducers with Standard CMOS Layers Machining							Comment		
	CMOS Technology	Tech. Scalability	Key Feature	Gap / Cavity Sacrificial Layer	Structure Material	Device Motion	Dielectric Charging		Resonant Frequency	Q-factor
J. Verd, <i>et al.</i> , 2006 (UAB) ⁽³³⁾	AMS 0.35 $\mu\text{m}^{(33)}$	Yes	Easy process, Limited transduction area	CMOS IMD	Metal (M4) ⁽³¹⁾ Metal (M5) ⁽³³⁾	Laterally flexural (CCB)	No	60 MHz ⁽³¹⁾ 24.36 MHz ⁽³³⁾	30 ⁽³¹⁾ 816 ⁽³³⁾	· Considerable R_{in} (M Ω) stemming from limited transduction area · Small footprint
J. L. Lopez, <i>et al.</i> , 2009 (UAB) ⁽³⁵⁾	TSMC 0.35 μm	Yes	Easy process (One maskless postprocessing)	CMOS IMD	Metal (M4)	Vertically flexural (Membrane)	No	39.5 MHz	806	· Yield issue (Time control process) · Single M4 layer as MEMS structure
C.-L. Dai, <i>et al.</i> , 2007 (NCHU) ⁽⁶³⁾	AMS 0.35 μm	No	Timeliest transduction gap for CMOS-MEMS	CMOS IMD	Poly-Si (Poly2)	Laterally flexural (CCB)	No	22 MHz	4400 227 (Air)	· Impressive gap space (40 nm) by etching interpoly oxide · Decent Q-factor due to the use of poly-Si layer
J. L. Lopez, <i>et al.</i> , 2009 (UAB) ⁽³⁵⁾	AMI 1.5 μm	No	Tiny gap for capacitive transduction (55/120 nm)	CMOS dielectric	Poly-Si	Vertically flexural (Dome)	No	51.36 MHz	1020	· Yield issue · Laminated vibrating structure formed by 2-poly platform · High Q-factor response due to polycrystalline silicon (poly) gate layers
M. K. Zhalutdinov, <i>et al.</i> , 2010 (Cornell) ⁽⁶⁴⁾	TSMC 0.35 μm	Yes	(i) Enable manifold structure stacking; (ii) Various boundary conditions	CMOS IMD	Metal, Metal+W, Metal+IMD	Vertically flexural (Plate, FFB) Laterally flexural (Pin-Pin beam)	No	852 kHz (Plate) 3.66 MHz (FFB) 1.45 MHz (PPB)	3550 (Plate) 1770 (FFB) 810 (PPB)	· Flexible resonator design enabling multiple-dimensional motion
W.-C. Chen, <i>et al.</i> , 2011 (NTHU) ⁽³²⁾	TSMC 0.18 μm	Yes	Easy process (One maskless postprocessing)	CMOS IMD	Metal, CMOS IMD	Laterally flexural (DETF)	No	5 MHz	2324	· Verifying the advantage of Q-factor enhancement via monolithic integration
C.-S. Li, <i>et al.</i> , 2012 (NTHU) ⁽³⁴⁾	TSMC 0.35 μm	No	Enable different gap spacings via various stacking of pull-in stopper	CMOS IMD	Metal, CMOS IMD	Vertically flexural (CCB Array)	No	4.1–4.5 MHz (different gap stacking)	36–67	· Low Q-factor for CCB design · Stress-induced curling due to clamp-clamp boundary condition
M.-H. Li, <i>et al.</i> , 2012 (NTHU) ⁽³⁶⁾	AMS 1.2 μm	Yes	Pioneer for foundry-oriented CMOS-MEMS with post bulk machining	Si substrate	Metal, CMOS dielectric, Poly-Si	Vertically flexural (Cantilever)	No	33.29 kHz	7000	· High Q-factor with complex composite structure · Pressure-dependent Q-factor is performed
O. Paul, <i>et al.</i> , 1995 (ETH) ⁽⁶⁵⁾	AMS 0.8 μm	Yes	Electrochemical etch stop technique on the n-well for substrate remaining	Si substrate	Silicon nitride, Metal, CMOS dielectric, Si n-well	Vertically flexural (Cantilever)	(Magnetic Drive / Transistor Sense)	354 kHz	8800 960 (Air)	· High Q-factor response due to remaining Si substrate
D. Lange, <i>et al.</i> , 2002 (ETH) ⁽⁶⁶⁾	IBM 90 nm SOI CMOS	Yes	"Damascene" process enabling multiple MEMS devices	Organic	Copper, Dielectric	Vertically flexural (Cantilever)	Yes (Slight)	4.4 MHz ($V_p = 2\text{ V}$)	1220	· Using copper-based processes for MEMS devices · Dedicated fabrication module for sacrificial organic layer
C. V. James, <i>et al.</i> , 2004 (IBM) ⁽⁶⁷⁾	JAZZ 0.35 μm	Yes	Dry-etching only Postprocessing	CMOS IMD, Si substrate	Metal, CMOS IMD	Laterally flexural (SFR)	Yes (Slight)	17.63 MHz	1400	· Limited configuration
C. C. Lo, <i>et al.</i> , 2005 (CMU) ⁽⁶⁸⁾	JAZZ 0.35 μm	Yes	Dry-etching only Postprocessing with Si substrate remaining	CMOS IMD, Si substrate	Metal, CMOS IMD, Si substrate	Laterally flexural (SiFR)	Yes (Slight)	8.04 MHz	3598	· Si remaining for (i) larger transduction area; (ii) structure curling prevention · Limited configuration
C. C. Lo, <i>et al.</i> , 2007 (CMU) ⁽⁵⁹⁾	UMC 0.18 μm	Yes	Commercially available platform without any in-house postprocessing	CMOS IMD	Metal, IMD (Oxide-rich)	Laterally flexural (Cantilever)	No (Thermal Drive/Piezo-R Sense)	176 kHz	2180 200 (Air)	· No need for in-house released processing · Versatile transduction mechanisms in a single device

BEOL post oxide removal (Dry)

G.-C. Wei, <i>et al.</i> , 2012 (NTHU) ⁽⁶⁹⁾	High yield, Easy process (One maskless postprocessing)	Yes	TSMC 0.35 μm	Yes	Metal (AlCu+TiN)	Metal, IMD (Oxide-rich)	Laterally flexural (Cantilever)	Yes	200 kHz	80 (Air)	<ul style="list-style-type: none"> · PLL enhanced oscillation · Good stability & repeatability of resonant frequency
W.-C. Chen, <i>et al.</i> , 2012 (NTHU) ⁽⁴⁶⁾	High yield, Good etching selectivity for post-CMOS steps	Yes	TSMC 0.18 μm	Yes	Metal+W	Metal, IMD (Oxide-rich ~97%)	Lamé mode	Yes	47.9 MHz	11271 6780 (Air)	<ul style="list-style-type: none"> · Extremely high Q due to the 97% ingredient of oxide
C.-C. Chen, <i>et al.</i> , 2012 (NTHU) ⁽⁵⁰⁾	First CMOS-MEMS VHF thermal-piezoresistive resonator	Yes	TSMC 0.35 μm	Yes	Si substrate	IMD, Poly	Dog bone	No	50.8 MHz	589	<ul style="list-style-type: none"> · N=2 II-BAR array is realized · Fully differential operation is used for severe feedthrough cancellation · Provide Poly-1 & Poly-2 sensing comparison · Thermal stability comparison under different operation modes (CC, CV, & CR)
C.-S. Li, <i>et al.</i> , 2013 (NTHU) ⁽⁴⁷⁾	Only low-loss materials for vibration beam to enable high-Q response	Yes	TSMC 0.35 μm	Yes	Metal+W, Si substrate	Metal, IMD (Oxide-rich)	Dog bone	Yes (Slight)	4.95 MHz	15000	<ul style="list-style-type: none"> · Thermal stability comparison under different operation modes (CC, CV, & CR)
Y.-C. Liu, <i>et al.</i> , 2013 (NTHU) ⁽⁴⁴⁾	High yield, Good etching selectivity for post-CMOS steps	Yes	TSMC 0.35 μm	Yes	Metal (AlCu+TiN)	Metal, IMD (Oxide-rich)	Vertically flexural (CCB)	Yes	7.99 MHz	6102	<ul style="list-style-type: none"> · High DC bias for operation · Excellent stopband rejection via circuit integration (~60 dB) · Charge issue
M.-H. Li, <i>et al.</i> , 2015 (NTHU) ⁽⁶²⁾	On-chip oven for compensating frequency drift	Yes	TSMC 0.35 μm	Yes	Metal+W, Si substrate	Metal, IMD (Oxide-rich)	Laterally flexural (DETF)	Yes	1.17 MHz	3029	<ul style="list-style-type: none"> · 100% yield for Postprocessing · TCF<-1 ppm/k while on-chip oven is activated
C.-H. Chin, <i>et al.</i> , 2014 (NTHU) ⁽⁶⁶⁾	Versatile gap configurations (290 nm ⁽⁶⁶⁾ , 190 nm ⁽⁶⁸⁾)	No	TSMC 0.35 μm	No	Poly-Si	Metal, IMD (Oxide-rich)	Vertically flexural (CCB)	Yes (Slight)	3.7 MHz ⁽⁶⁶⁾ 4.22 MHz ⁽⁶⁸⁾	1700 ⁽⁶⁶⁾ 1000 ⁽⁶⁸⁾	<ul style="list-style-type: none"> · Proprietary gap feature enabling RGFET design · Only for 2-Poly CMOS
M.-H. Li, <i>et al.</i> , 2015 (NTHU) ⁽⁶⁰⁾	TiN layers as transduced electrodes	Yes	TSMC 0.35 μm	Yes	Metal (AlCu)	Metal, IMD (Oxide-rich)	Vertically flexural (PFB)	No	11.5 MHz	1400	<ul style="list-style-type: none"> · Alleviate charge issue of oxide-rich capacitive devices · Complicated postprocessing · TCF of 0.6 ppm/K
R. Marathe, <i>et al.</i> , 2014 (MIT) ⁽⁷⁰⁾	First CMOS-based unreleased RBT with FET sensing	Yes	IBM 32 nm SOI CMOS	Yes	N/A	Poly-Si, Gate dielectric, and Si substrate	Longitudinal acoustic	No	11.1 GHz	30	<ul style="list-style-type: none"> · Footprint less than $5 \times 3 \mu\text{m}^2$ · ABRs for defining acoustic vibration · TCFs between ± 3 ppm/K

Unreleased

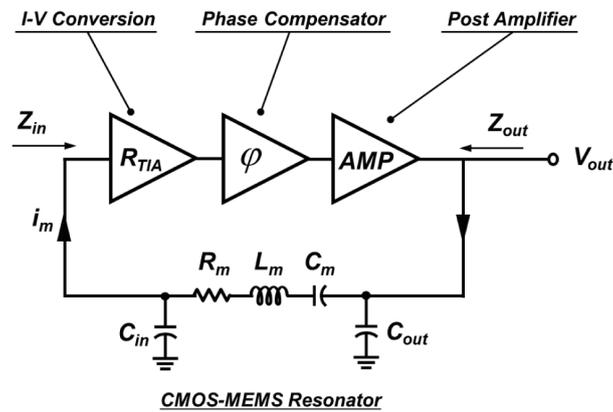


Fig. 13. General schematic for a CMOS-MEMS oscillator.

Table 3
Summary of state-of-the-art CMOS-MEMS oscillators.

Reference	EDL 2008 ⁽⁷⁴⁾	Sens J 2012 ⁽⁷⁵⁾	IEDM 2014/ JMEMS 2015 ^(62,73)		Transducers 2013 ⁽⁷⁶⁾	JMM 2015 ⁽⁷⁷⁾	EDL 2016/IFCS 2016 ^(78,79)		
CMOS process	0.35 μm	0.35 μm	0.35 μm		0.35 μm	0.35 μm	0.35 μm		
Resonator shape	Cantilever	Ring	DETF		DETF	CC-Beam	DETF		
TIA topology	R-termination with buffer	Current amp	R-feedback		C-integrator	RGFET	Integrator-differentiator		
f_o (MHz)	6.32	9.4	1.2		11	4.28	1.23		
Q -factor	100	950	1700		147	1000	1900		
V_{DD} (V)	3.3	3.3	2.5		3.3	1.8	2.5		1.3
⁺ Core power (mW)	5.2	—	1.3		1.5	3.5	0.15		0.065
MEMS dc-bias (V)	45	30	45	70.6	3	60	7	22	20
R_m (W)	—	349k	700k	—	8M	5.6k	16M	1.7M	2M
PN @10 Hz	—	—	-64	-77	10	—	-42	-63	—
PN @100 Hz	-32	—	-94	-97	-20	-80	-72	-93	-90
PN @1 kHz	-55	—	-112	-113	-50	-93	-106	-120	-110
PN Floor	-94	—	-120	-119	-109	-117	-111	-122	-113
FOM1@100Hz (dB)	120.8	—	174.4	176.9	119	167.1	162.2	183	183.6
FOM1@1kHz (dB)	123.8	—	172.4	173.4	129	160.7	176.1	190	183.6
FOM2 ($\text{Hz}^2\Omega^2$)	—	—	2.40×10^{18}		1.7×10^{21}	3.63×10^{14}	1.44×10^{21}	2.04×10^{20}	8.20×10^{19}

⁺Power consumption only accounts for the TIA, phase compensator, and voltage amplifier.

Figures of merit

$$\text{FOM1} = \frac{1}{L(f_m) \times (P_{DC}/1 \text{ mW})} \left(\frac{f_o}{f_m} \right)^2$$

$$\text{FOM2} = \frac{k_B T}{PN \text{ Floor} \times P_{DC}} f_o^2 R_m^2$$

P_{DC} = DC Power

$L(f_m)$ = Phase noise at offset f_m

k_B = Boltzmann constant

T = Absolute temperature ($T = 320 \text{ K}$ is used here)

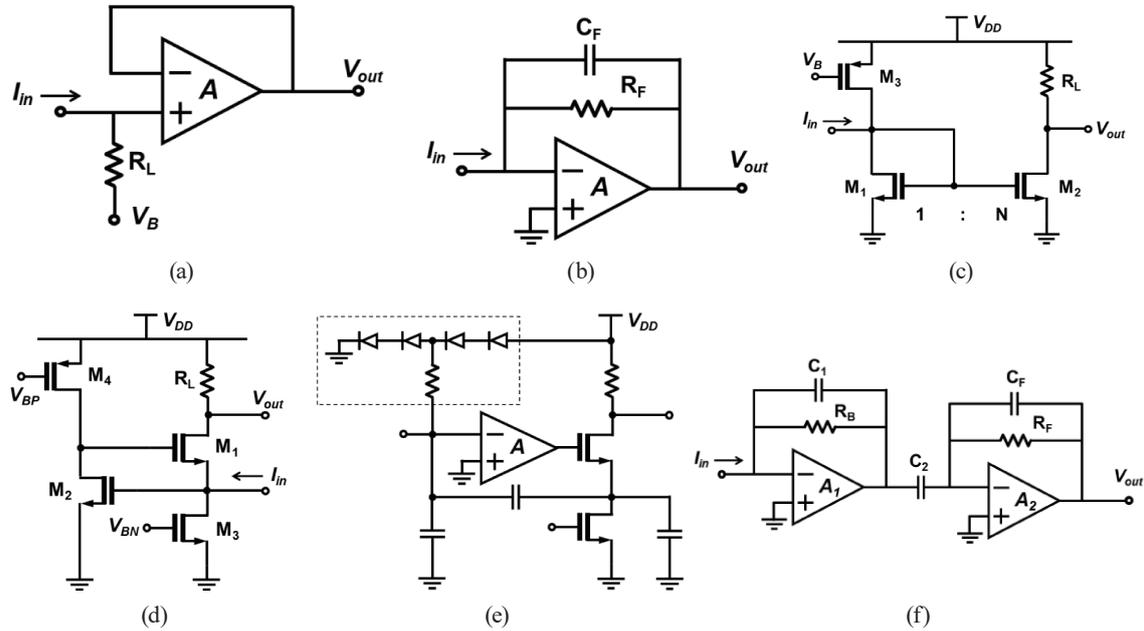


Fig. 14. Topologies for the TIAs: (a) resistive termination with buffer, (b) feedback TIA, (c) current amplifier, (d) regulated-cascode TIA, (e) capacitive feedback TIA, and (f) integrator–differentiator TIA.

Table 4
Analysis of the front-end TIAs (as referred to in Fig. 14).

Topology	TransZ Gain R_{TIA}	**Bandwidth ω_{3dB}	Input-referred Current Noise $i_n^2/\Delta f$
R-termination with buffer (a)	R_L	$\frac{1}{R_L C_P}$	$\frac{4kT}{R_L} + \frac{v_{n,OP}^2}{\Delta f} \omega^2 C_P^2$
Feedback topology (b) (for $R_F \ll R_B$)	R_F	$\frac{\sqrt{2}}{R_F C_F}$ (critical damped)	$\frac{4kT}{R_F} + \frac{v_{n,OP}^2}{\Delta f} \left(\frac{1}{R_F^2} + \omega^2 (C_P + C_F)^2 \right)$
Feedback topology (b) (for $R_F \rightarrow R_B$)	$\frac{1}{\omega C_F}$	$\frac{1}{R_B C_F}$	$\frac{4kT}{R_B} + \frac{v_{n,OP}^2}{\Delta f} \left(\frac{1}{R_B^2} + \omega^2 (C_P + C_F)^2 \right)$
Current amplifier (c)	$N \times R_L$	$\frac{1}{g_{m1} C_P}$	$4kT \gamma (g_{m1} + g_{m3}) + 4kT \left(\gamma g_{m2} + \frac{1}{R_2} \right) \frac{1}{N^2}$
Regulated cascode (d)	R_L	$\frac{1}{g_{m1} g_{m2} (r_{o2} \parallel r_{o4}) C_P}$	$\frac{4kT}{R_L} + 4kT \gamma g_{m3} + \frac{4kT \gamma (g_{m2} + g_{m4}) \omega^2 C_P^2}{g_{m2}^2}$
*Capacitive feedback (e)	$R_L \left(1 + \frac{C_2}{C_1} \right)$	$\frac{\sqrt{2} A g_{m1} C_1}{C_2 (C_1 + C_P)}$	$\frac{1}{(1 + C_2/C_1)} \left(\frac{4kT}{R_L} + \frac{i_B^2}{\Delta f} \right) + \frac{v_{n,OP}^2}{\Delta f} \omega^2 (C_1 + C_P)^2$
Integrator–differentiator (f)	$R_F \left(\frac{C_2}{C_1} \right)$	$\frac{1}{R_F C_F}$	$\frac{4kT}{R_B} + \frac{4kT}{R_F (C_2/C_1)^2} + \frac{v_{n,OP1}^2}{\Delta f} \omega^2 (C_1 + C_P)^2$

In a general assumption, $R_B \gg R_F > R_L$.

C_P is the parasitic capacitance at the TIA input.

* $i_B^2/\Delta f$ is the current noise from the high impedance bias network.

**Assume the TIA output is connected to a light load ($C_L \ll C_P$), so the BW is dominated by C_P or C_F .

feedback technique can solve this issue, such as the shunt-shunt feedback topology depicted in Fig. 14(b). The transimpedance gain can be attained across a wider bandwidth. The current amplifier in Fig. 14(c) and the regulated cascade amplifier in Fig. 14(d) can provide an even wider bandwidth by reducing its input impedance via a local feedback technique as a compromise in the noise performance. Finally, the capacitive feedback [cf. Fig. 14(e)] and integrator–differentiator [cf. Fig. 14(f)] topologies provide very low input referred noise and superior gain, but are only suitable for low-frequency (~MHz) implementations. Once the capacitance ratio (C_2/C_1) is reduced for a wider bandwidth, the noise performance will be degraded. Among all the topologies given, the resistive feedback topology [i.e., Fig. 14(b)] provides the best performance trade-off in terms of gain, bandwidth, and noise.

Table 3 summarizes the state-of-the-art BEOL embedded CMOS-MEMS oscillators with various TIA topologies. In Ref. 74, a modified resistance termination topology is introduced by directly connecting the pseudoresistor across the unity gain buffer in a negative feedback fashion. Such an implementation requires additional phase compensators and voltage amplifiers, hence increasing the power consumption. The same research group provided an advanced design in 2013⁽⁷⁶⁾ using a charge integrator instead of the buffer, showing a great improvement in the power and phase noise. On the other hand, resistive feedback is adopted in Refs. 62 and 73 to provide a low-noise and wide-bandwidth amplification. The phase noise floor of -120 dBc/Hz is reported under a moderate bias voltage of 45 V. To further improve the phase noise, the integrator–differentiator is explored in Refs. 78 and 79 using a similar CMOS-MEMS resonator device, and demonstrates a superior phase noise figure of merit (FOM1) of 190 dB.

3.2 Temperature stability

The oscillator's temperature stability is strongly dependent on the resonator's TC_f and is slightly affected by the circuit across temperature. To address this issue, an ultralow-power consumption micro-oven technique is used in Refs. 62 and 80. Thanks to the low thermal conductivity of the silicon dioxide in the CMOS, the thermal resistance (R_{th}) and heat capacitance (C_{th}) can be properly designed in the CMOS-MEMS resonator platform to achieve an ultralow-power, fast-response micro hotplate. The latest work in Ref. 80 demonstrates a sub-mW 4 ppm temperature stability across a 94 °C span (equivalent to 43 ppb/°C).

4. Conclusions and Future Remarks

In this paper, we report the progress of CMOS-MEMS resonant technology over the past decades, including various fabrication technologies, improvement of resonator performance, bottlenecks and their corresponding solutions. In terms of fabrication platforms, the foundry-oriented approach (i.e., BEOL micromachining) is preferred and emphasized owing to its accessibility, flexibility, fast prototyping, and low cost. Through different post-CMOS release processes, the quality factor Q , the motional impedance R_m , the thermal stability TC_f , and the charging effect require a certain level of trade-off. Finally, a TiN-C process shows

a good balance of all performance indices, which is expected to serve as the main CMOS-MEMS platform in the future to enable high-performance oscillators and filters. In addition to resonator technology, some popular sustaining circuit designs for oscillation are also presented to realize monolithic CMOS-MEMS oscillators. As a future perspective, a potential Sensors System on Chip (S-SoC) through CMOS-MEMS technology becomes feasible to be widely implemented in IoT and Smart Living.

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