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31.6 pJ/Conversion-step Energy-efficient 16-bit Successive Approximation Register Capacitance-to-digital Converter in a 0.18 μm CMOS Process

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In this paper, an energy-efficient 11.49-bit successive approximation register (SAR) capacitance-to-digital converter (CDC) for capacitive sensors with a figure of merit (FoM) of 31.6 pJ/conversion-step is presented. The CDC employs a SAR algorithm to obtain low power consumption and a simplified structure. The proposed circuit uses a capacitive sensing amplifier (CSA) and a dynamic latch comparator to achieve parasitic capacitance-insensitive operation. The CSA adopts a correlated double sampling (CDS) technique to reduce flicker (1/*f*) noise to achieve low-noise characteristics. The SAR algorithm is implemented in dual operating mode, using an 8-bit coarse programmable capacitor array in the capacitance domain and an 8-bit R-2R digital-to-analog converter (DAC) in the charge domain. The proposed CDC achieves a wide input capacitance range of 29.4 pF and a high resolution of 0.449 fF. The CDC is fabricated in a 0.18 μm 1P6M complementary metal–oxide–semiconductor (CMOS) process with an active area of 0.55 mm^2. The total power consumption of the CDC is 86.4 μW with a 1.8 V supply. The SAR CDC achieves a measured 11.49-bit resolution within a conversion time of 1.125 ms and an energy-efficiency FoM of 31.6 pJ/conversion-step.

1. Introduction

Capacitive sensors are widely used in various applications such as pressure, humidity, and acceleration measurements. As capacitive sensors do not consume static current during signal readout, they are suitable for applications with limited energy budgets.(1) A conventional capacitive sensor interface circuit comprises a capacitive sensing amplifier (CSA), which converts capacitance to voltage, and an analog-to-digital converter (ADC), which digitizes the output voltage. However, the CSA and signal conditioning steps consume large amounts of power and require a large area,(2) which has led to the preferential use in recent capacitive

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interface circuits of direct capacitance-to-digital converters (CDCs) to achieve reduced complexity, area, and power consumption.[1–3]

Previous studies have presented CDC design methods for high resolution and low power consumption. ΣΔ CDCs achieve very high resolution through oversampling and noise shaping;[3–5] however, they consume high amounts of power owing to oversampling and digital decimation filtering and have limited capacitance ranges to avoid modulator overload.[3,4] Another technique for capacitive sensor measurement is a semidigital approach[3,6,7] in which the input capacitance is converted to time and subsequently digitized using a time-to-digital converter. Although period or pulsewidth modulation can be used to compensate for the capacitance range when converting input capacitance to time, time-to-digital converters require a fast digital counter and a stable high-frequency oscillator circuit that increases power consumption.[3,7] Interface circuits such as these are not suitable for energy-constrained low-power applications because of their power consumption.

In this paper, an energy-efficient 16-bit successive approximation register (SAR) CDC for capacitive sensors is presented. The proposed CDC applies the SAR algorithm that does not require oversampling and digital filtering to obtain low power consumption and a simplified structure.[3,8] The comparator comprises a CSA and a dynamic latch, with the CSA stage used to enable operation that is insensitive to the parasitic capacitances generated in the sensor capacitors, which would otherwise cause the degradation of the output signal from noise coupling, charge injection, and offset. The CSA uses a correlated double sampling (CDS) technique designed to reduce offset and flicker noise (1/*f*). Although a conventional SAR algorithm using only a capacitor array can digitize a wide range of capacitances within a compact area,[9] this scheme has limited resolution because it adds parasitic capacitance to the circuit as well as in the sensor. To avoid this problem, the SAR algorithm of the proposed circuit is configured to operate in dual operating mode: a capacitance domain using an 8-bit coarse programmable capacitor array, and a charge domain using an 8-bit R-2R digital-to-analog converter (DAC). As the proposed CDC is insensitive to a parasitic capacitor, it achieves a wide input capacitance range. In addition, the charge domain provides a high resolution for sensitive sub-femtofarad measurements.

2. Circuit Operation of Proposed Successive Approximation CDC

A schematic of the proposed 16-bit SAR CDC circuit is shown in Fig. 1. It comprises a CSA, a dynamic latch, SAR control logic, an 8-bit coarse programmable capacitor array (CDAC), and an 8-bit R-2R DAC.

Circuit operation is performed in two phases. In addition to the SAR clock, the SAR CDC requires non-overlapping clocks (P_1 and P_2). Figure 2 shows the operation of the circuit in each phase. During the sampling phase (P_1), the CSA operates as a unit gain buffer to charge the sensor capacitor (C_S) and C_{DAC}. The stored charge is given by

$$P_1 : C_S(V_{ref} - V_{DD}) + C_{LSB}V_{ref}. \quad (1)$$

During the amplification phase (P_2), the charge stored in C_S and C_{DAC} redistributes to the

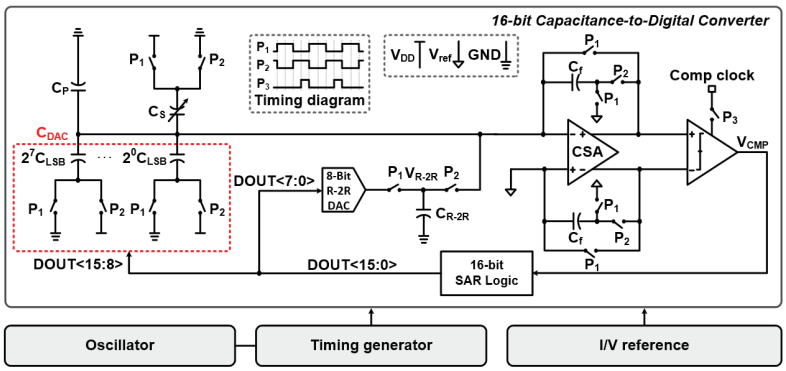
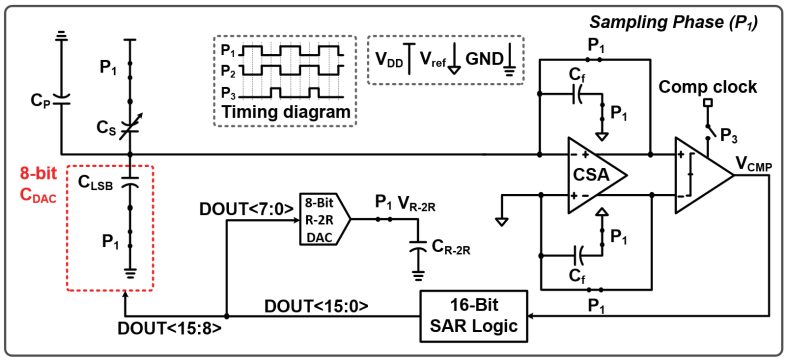
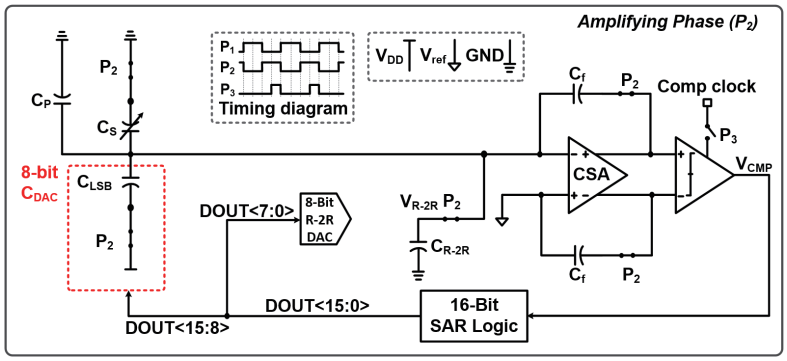


Fig. 1. (Color online) Schematic of the proposed 16-bit SAR CDC.



(a)



(b)

Fig. 2. (Color online) 16-bit SAR CDC operation of each phase.

feedback capacitor (C_f). The charge is given by

$$P_2:\ C_S V_{ref} + C_{LSB}(V_{ref} - V_{DD}) + C_f(V_{ref} - V_O) + C_{R-2R}V_{R-2R}. \tag{2}$$

As the charge is conserved, from Eqs. (1) and (2), the output voltage (V_O) at the CSA is as follows:

$$V_O = \frac{(C_S - C_{LSB})V_{DD} + C_{R-2R}V_{R-2R}}{C_f} + V_{ref}. \tag{3}$$

Thus, the differential input of the comparator is given by

$$\Delta V_O = V_O - V_{ref} = \frac{(C_S - C_{LSB})V_{DD} + C_{R-2R}V_{R-2R}}{C_f}. \quad (4)$$

In addition, the proposed CDC simultaneously performs CDS operations in phases P_1 and P_2. In phase P_1, the input signal and low-frequency noise are stored in C_f. Then, in phase P_2, the signal is amplified as output voltage through C_f and the stored noise is subtracted. The output differential voltage (ΔV_O) is converted to a digital code by a comparator that uses a dynamic latch to achieve low power consumption. Figure 3 shows a schematic of the dynamic latch comparator.

Depending on the comparator output (V_{CMP}), the 16-bit SAR logic, which is based on a binary search algorithm, changes the digital inputs of the capacitance domain and charge domain using the 8-bit C_{DAC} and 8-bit R-2R DAC. The first 8-bit SAR control logic updates the selected 8-bit C_{DAC} of the capacitance domain. The lower 8-bit SAR control logic then operates in the charge domain, with charges determined by the output voltage ($V_{R\text{-}2R}$) of the R-2R DAC during the P_1 phase stored to the R-2R capacitor ($C_{R\text{-}2R}$). During the P_2 phase, the stored charges update the CSA input and are amplified by the CSA stage. This process repeats for 16 cycles until C_S and the updated capacitor values are equal according to the SAR algorithm. With this dual operating mode, the proposed 16-bit SAR CDC achieves a wide input capacitance range of 29.4 pF and a high resolution of 0.449 fF.

3. Prototype Circuit Implementation and Experimental Results

3.1 Prototype circuit implementation and measurement environment

A photograph of the fabricated die form of the 16-bit SAR CDC is shown in Fig. 4. The proposed SAR CDC was fabricated using a 0.18 μm 1P6M complementary metal–oxide–semiconductor (CMOS) process with an active area of 0.55 mm^2 excluding the I/O pads.

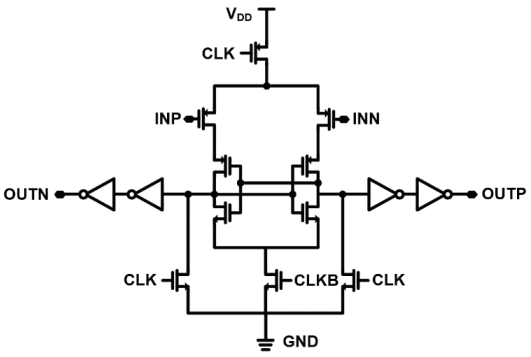


Fig 3. Schematic of the dynamic latch comparator.

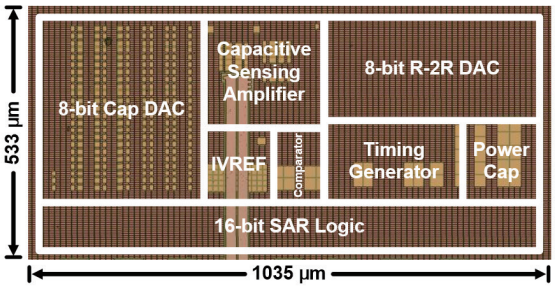


Fig. 4. (Color online) Die photograph of 16-bit SAR CDC.

Figure 5 shows the measurement environment and information on the equipment for measuring the proposed circuit with a *Z*-axis accelerometer. The fabricated chip was implemented on a printed circuit board (PCB) to measure the performance of the circuit. The capacitive sensor uses a *Z*-axis accelerometer with specifications described in Ref. 10. The digital output code is acquired through a digital oscilloscope.

3.2 Experimental results

The simulation results produced by the proposed 16-bit SAR CDC are shown in Fig. 6. Figure 6(a) shows the input signal of sensor capacitance with a capacitance change of 14.7 pF based on a nominal capacitance of 14.7 pF, which was obtained using Verilog-A modeling. The output digital code converted by the proposed circuit is shown in Fig. 6(b).

The measured capacitance results arising from the effects of gravity on the *Z*-axis accelerometer are illustrated in Fig. 7. To measure the performance of the proposed 16-bit SAR CDC, the PCB and *Z*-axis accelerometer were rotated by 180°. The red line shows the results obtained by rotating only the *Z*-axis accelerometer, which were measured using a Keysight 4284A LCR meter. The blue line shows the *Z*-axis accelerometer results for the proposed circuit. The sensitivities of the SAR CDC and *Z*-axis accelerometer were measured as 105 fF/g.

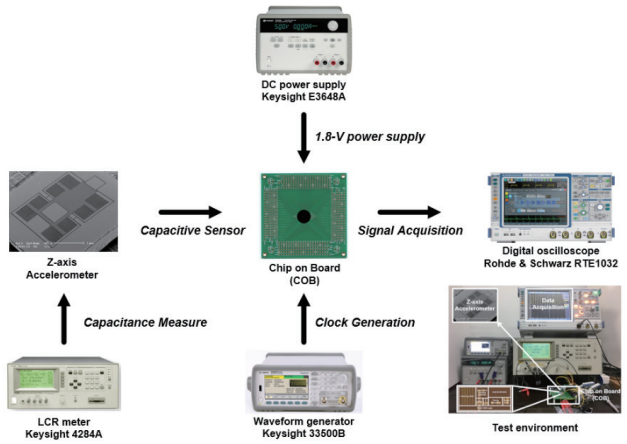
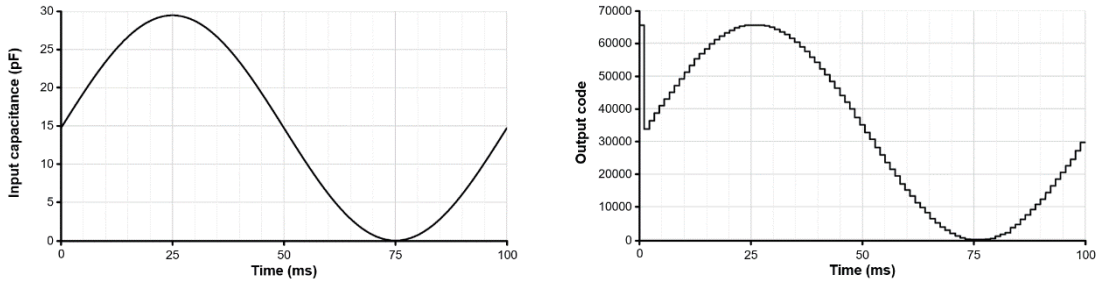


Fig. 5. (Color online) Measurement environment for 16-bit SAR CDC.



(a) (b)

Fig. 6. Simulation result of 16-bit SAR CDC: (a) input signal and (b) digital output code.

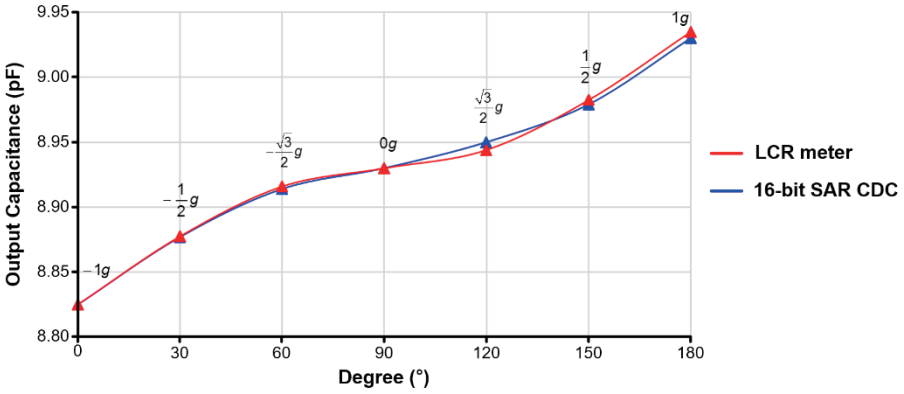


Fig. 7. (Color online) Measured result of *Z*-axis accelerometer.

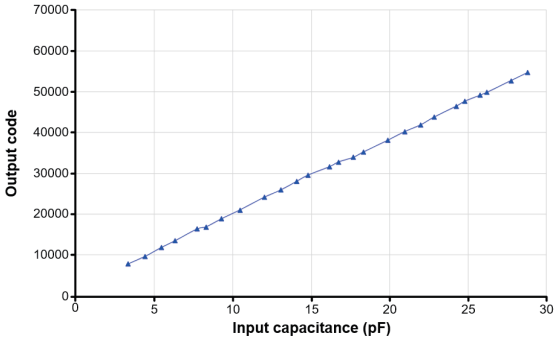


Fig. 8. (Color online) Measured transfer function of proposed CDC.

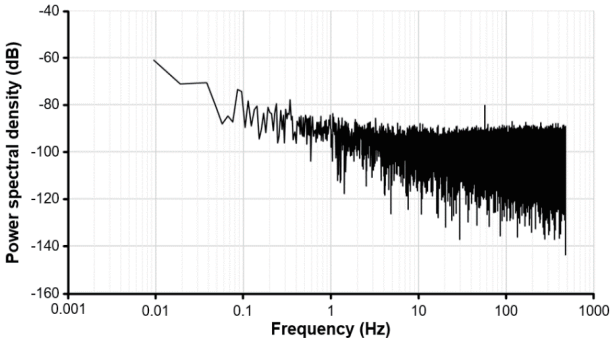


Fig. 9. Measured noise power density.

Figure 8 shows the transfer function, or the results of input conversion when the input capacitance was varied from 3.33 to 28.79 pF in 1 pF steps, of the proposed CDC. The measured characteristic demonstrates the linearity between the input capacitance and the output code over the dynamic range of the CDC.

To calculate an effective number of bits (ENOB), the noise power density of the CDC was measured using a MATLAB fast Fourier transform (FFT) process and found to achieve −70.95 dB within a bandwidth of 475 Hz. The noise power density measurement result is shown in Fig. 9. The CDC achieves 11.49-bit resolution by calculating the output noise density within a conversion time of 1.052 ms.

The total power consumption of the fabricated circuit is 86.4 μW with a 1.8 V supply. To evaluate the energy efficiency of the proposed CDC, an energy-efficiency figure-of-merit (FoM) that is widely used to compare the performance of CDCs was used. The FoM is defined as

$$FoM = \frac{P_{avg} \times T_{conv}}{2^R}, \tag{5}$$

where P_{avg} is the power consumption, T_{conv} is the conversion time, and R is the resolution in bits. The proposed CDC achieves energy efficiency comparable to a FoM of 31.6 pJ/conversion-

Table 1
Performance comparison: summary of measured parameters.

Parameter	This work	[3]	[7]	[8]	[11]	[12]
Architecture	SAR	SAR	C2T*	SAR	2nd-ΣΔ	ΣΔ
Output format	Digital code	Digital code	PM**	Digital code	Bit stream	Bit stream
Technology (μm)	0.18	0.35	0.35	0.18	0.18	0.16
Supply (V)	1.8	3.3	3.3	0.9/1	2.6	1.2
Power (μW)	86.4	303	211	3.84	2340	10.3
Active area (mm^2)	0.55	0.07	0.51	0.1	0.67	0.28
Conversion time (ms)	1.052	0.65	7.6	0.0425	3.07	0.8
Capacitance range (pF)	29.4	16	6.8	16.14	10	0.54–1.06
ENOB (bit)	11.49	12.5	15	11.8	17.4	11.1
FoM (pJ/conversion-step)	31.6	34	49	0.045	37	3.754

*C2T = Capacitance-to-time, **PM = Period modulation

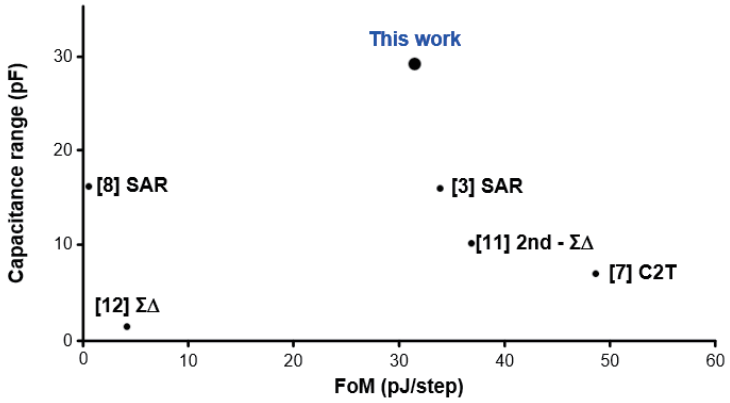


Fig. 10. (Color online) Comparison of capacitance ranges and FoMs.

step. A performance summary of the measured parameters and comparisons with state-of-the-art CDCs are shown in Table 1, and the capacitance ranges and FoMs of these are compared in Fig. 10, from which it is seen that the proposed SAR CDC achieves the widest capacitance range and an excellent energy efficiency. These results suggest that the proposed SAR CDC can be successfully applied to various low-power applications.

4. Conclusions

An energy-efficient 16-bit SAR CDC for use in a variety of capacitive sensors is presented in this paper. In the proposed circuit, the digital output code is directly converted for use by a CSA, dynamic latch, and SAR algorithm. As it relaxes analog block requirements, the proposed circuit has high energy efficiency. Its use of a CSA enables operational insensitivity to problems caused by parasitic capacitance, and noise characteristics are improved by applying a CDS technique to the CSA. The SAR algorithm is implemented in dual mode, with a capacitance domain providing a wide capacitance range of 29.4 pF and a charge domain improving the resolution to 0.449 fF. The chip is fabricated using a 0.18 μm 1P6M CMOS process with an active area of 0.55 mm^2. The total current consumption of the proposed CDC is 86.4 μW with a

1.8 V supply. The SAR CDC achieved a measured 11.49-bit resolution within a conversion time of 1.125 ms and an energy-efficiency FoM of 31.6 pJ/conversion-step.

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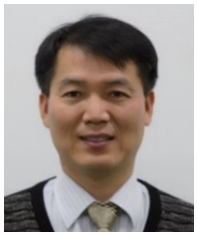

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