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Design Optimization of CMOS Control Circuit for Integrated Photovoltaic Power Transfer

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A CMOS control circuit for an integrated photovoltaic (PV) power transfer/harvesting platform is optimized. The proposed PV power transfer/harvesting platform is based on the concept of charging a small PV current in a capacitor and operating a target circuit intermittently. This architecture is suitable for various types of implantable or Internet of Things (IoT) devices. To realize the integration of PV cells on a CMOS chip, we need to improve the performance of the CMOS control circuit. We refined a self-powered voltage detector circuit in the CMOS control circuit to comply with small-current operation and improved the adjustability of the switching voltages. We describe a strategy and experimentally obtained results of the design optimization.

1. Introduction

Currently, various types of wireless power transfer technologies have been realized and utilized in both consumer and industry fields. Noncontact wireless power and data transfer for batteryless card terminals are commonly used in transportation and retailers. Wireless power transfer is also used to charge a battery in a cell phone and other gadgets. Most of the current wireless powering technologies are realized electromagnetically. Both power transmitter and receiver are equipped with cm-sized coils, and the inductive coupling between two (primary and secondary) coils is used for power transfer. The electric power is once transformed into alternative current (AC) and rectified into direct current (DC) in power-receiving devices.

However, in terms of small devices such as implantable or distributed Internet of Things (IoT) nodes, there is no de facto standard of the wireless power transfer technology. For these types of applications, there are constraints in device dimensions and weight. In the field of implantable electronics and distributed IoT technologies, device dimensions less than 1 cm or even 1 mm are expected for the reduction in invasiveness (implantable electronics) or the aesthetics of items (IoT nodes).

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In the case of electromagnetic wireless transfer,[1–10] the reduction in device size requires a reduction in the size of the secondary coil (diameter and number of turns). It causes a marked decrease in power transfer efficiency. It also requires a close placement of the primary and secondary coils. Consequently, for very small implantable or IoT devices, it is not reasonable to use the electromagnetic power transfer schemes.

The authors propose to use photovoltaic (PV) power[4,11–14] transfer, thus, using solar cells for powering very small electronic devices.[15] In general, the reduction in coil size for electromagnetic power transfer causes the reduction in both voltage and current. On the other hand, as a nature of solar cells, a reduction in the size of solar cells only leads to a reduction in generated photocurrent. The voltage from solar cells under sufficient illumination scarcely depends on the size of solar cells. We propose to take advantage of this intrinsic characteristic of solar cells. We use series-connected small solar cells as a power receiver with sufficient voltage and insufficient current.

Figure 1 shows the concept of the proposed PV power transfer scheme.[15] Figure 2 shows a block diagram of the proposed PV power transfer/energy-harvesting platform. We integrate series-connected solar cells with a capacitor to charge the generated electric power. Adopting series-connected solar cells, we can obtain sufficient voltage for the operation of the target circuit without a voltage-boosting circuit such as a switching capacitor circuit.[12,13,16,17] We can wait to obtain a preset capacitor voltage and operate the target circuit for a short time. Thus, the target circuit should be designed to be compatible with the intermittent operation. This operating scheme is suitable for various types of implantable sensors and IoT micronodes with intermittent functionality. The proposed operating scheme has a nature of adaptiveness to the available power from the light. Operating frequency is automatically adjusted to fit the available energy.

On the basis of this concept, we realized an optically powered, batteryless optical ID transmission device.[15] We used a set of 0.8 × 0.9 mm^2 discrete photodiodes as PV cells. We successfully obtained the optically powered operation of the device with an adaptiveness to

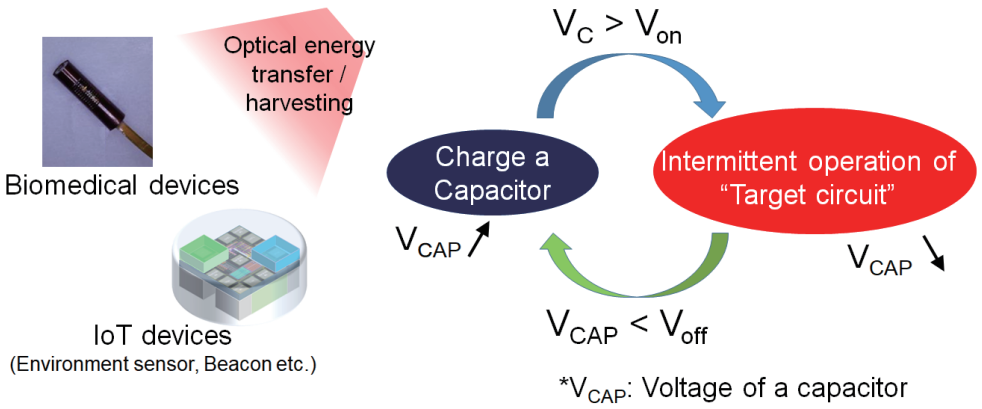


Fig. 1. (Color online) Concept of the CMOS-controlled PV power transfer scheme.

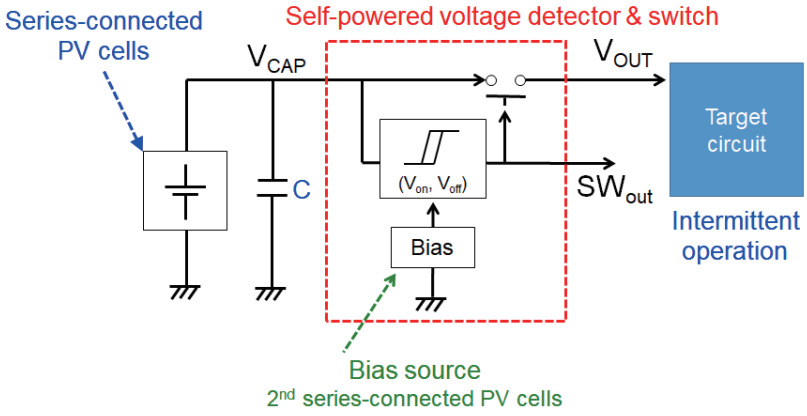


Fig. 2. (Color online) Block diagram of the CMOS-controlled PV power transfer platform.

the illumination. However, we found that relatively high intensity illumination is required to operate the device. The reduction in minimum operating intensity, i.e., photocurrent from series-connected PV cells, is required to realize mm-sized, batteryless microdevices.

In this work, we describe the optimization of the CMOS circuit design to reduce the minimum operating current. We also greatly improved the adjustability of the threshold voltages V_{on} and V_{off}, which are essential in the operation.

2. Basic Design and Circuit Operation of the Proposed PV Power Transfer/ Energy-harvesting Platform

The system shown in Fig. 2 consists of two sets of series-connected PV cells, a capacitor, a CMOS chip including a self-powered voltage detector, a powering switch, and a load circuit (target circuit). Off-chip loads such as light-emitting diodes (LEDs) can also be used. One of the series-connected PV cells is used for powering. The highest voltage node is connected to the capacitor, and photocurrent is accumulated in the capacitor. As the charge in the capacitor increases, the voltage of the capacitor, V_{CAP}, increases. Finally, we expect that V_{CAP} can reach a maximum value that corresponds to the open-circuit voltage × number of series-connected PV cells. We can choose the appropriate number of PV cells to obtain a specific voltage range required to drive the load circuit. In this work, we adopted 10-series PV cells integrated on the CMOS chip. The typical open-circuit voltage of the integrated PV cells is 0.4 V, and the maximum V_{CAP} is approximately 4 V.

V_{CAP} is monitored by a self-powered voltage detector, and the connection from the capacitor to the load circuit is controlled by a CMOS switch. The self-powered voltage detector turns the CMOS switch on and off. To supply current to the load circuit for a specific duration, the voltage detector is designed to have a hysteresis. When V_{CAP} reaches V_{on}, the output of the voltage detector, SW_{out}, becomes high and the CMOS switch is closed to operate the load circuit. Once the voltage detector transits to high, the transition voltage from high to low is V_{off}, which is lower than V_{on}. The operation of the load circuit causes a discharge of the capacitor and a

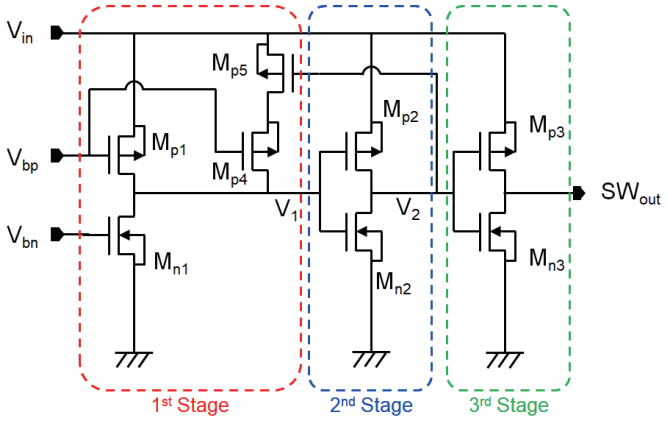
decrease in V_{CAP}. The CMOS switch is kept on before V_{CAP} goes down to V_{off}. V_{on} and V_{off}, as well as capacitance, should be designed to match with the voltage range and current required for the operation of the load circuit. For example, in the case of driving a blue LED as a load, V_{on} = 3.5 V and V_{off} = 2.5 V can be adopted as threshold voltages. The capacitance should be chosen to match with an expected operation duration of the LED. The self-powered voltage detector itself is driven by the voltage that the circuit monitors. Currently, the voltage detector needs some additional constant bias voltages independent of the powering voltage. We used the second set of series-connected PV cells to provide the bias voltages for the self-powered voltage detector. We take bias voltages at intermediate nodes of the second series-connected PV cells. These bias voltages are connected only to gates of MOS transistors in the circuit. Since no continuous current flows into the gates of MOS transistors, as soon as the PV cells are illuminated, all the intermediate nodes of the second series-connected PV cells rapidly reach a quasi-terminal state in which we obtain an open-circuit voltage from each cell. As a drawback of this simple approach, there is a constraint that we can use only quantized voltages and thus a simple multiplication of the open-circuit voltage of the on-chip PV cell (~0.4 V). It should be noted also that the voltages delivered from the series-connected PV cells slightly depend on the illumination.

Figure 3 shows two versions of the self-powered voltage detector circuit. Figure 3(a) shows the original circuit configuration employed in the previous work.[15] Figure 3(b) shows the improved circuit described in this work. We introduced two additional MOS transistors (M_{n4} and M_{n5}) and one additional bias input (V_{bp2}). The functions of the additional elements are described in the next section.

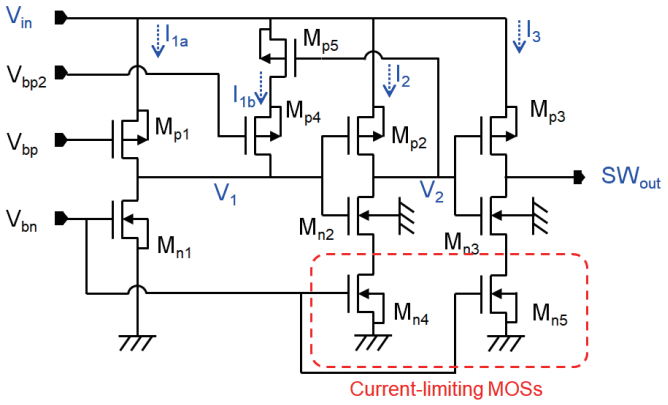
The basic self-powered voltage detector circuit [Fig. 3(a)] consists of series-connected three stages of digital components. The second and third stages are conventional inverters. The main features of the circuit, i.e., self-powered voltage detection and hysteresis, are realized by the first-stage switch. Different from the conventional inverter, the gates of the PMOS (M_{p1}) and NMOS (M_{n1}) transistors are biased with fixed voltages, which come from the second set of series-connected PV cells shown in Fig. 2. The operation of the voltage detector shown in Fig. 3(a) is as follows.

In the initial stage of the operation, when the first (powering) and second (biasing) series-connected PV cells are illuminated, both sets of PV cells generate photocurrent. Since the powering PV cells are connected to the capacitor, the photocurrent is charged to the capacitor and V_{CAP} increases gradually. On the other hand, in terms of the biasing PV cells, only some nodes are connected to MOS transistors in the CMOS circuit, and there is no current-draining path. The biasing PV cells rapidly get to a stable state and provide bias voltages to the CMOS circuit.

The initial switching behavior is determined by the two MOS transistors M_{n1} and M_{p1}. The source and gate terminals of M_{n1} are at fixed voltages, thus the source-gate voltage V_{GS} is equal to V_{bn}. M_{n1} gives some conductivity for the whole range of drain voltage V_1, the output voltage of the first-stage inverter. On the other hand, the source voltage of M_{p1} is $V_{in} = V_{CAP}$ and the gate voltage is V_{bp}. Therefore, the V_{GS} for M_{p1} depends on V_{CAP}. In the start-up stage of the PV power supply, V_{CAP} is low and V_{GS} (we use $V_{GS} = V_S - V_G$ for PMOS) is negative. Because of



(a)



(b)

Fig. 3. (Color online) (a) Basic[15] and (b) improved[18] circuits of the CMOS voltage detector circuit.

the negative V_{GS}, M_{p1} is turned off. The conductive M_{n1} and the resistive M_{p1} pull down V_1 to 0 V, and it gives $V_2 = V_{in}$ and $SW_{out} = 0$ V. The additional current pathway that consisted of two PMOSs, M_{p4} and M_{p5}, is not activated because $V_{GS} = 0$ for M_{p5}.

When PV cells are continuously illuminated, the photocurrent provided by the powering PV cells flows into the capacitor and V_{CAP} gradually increases. The V_{GS} of M_{p1} will turn positive and finally reach the threshold voltage of M_{p1} (typically 0.4–0.6 V for a 0.35 μm process that we use in this work) and higher. When the conductivity of M_{p1} becomes larger than that of M_{n1}, V_1 becomes high (= V_{in}). It causes transitions of the second- and third-stage inverters and gives $V_2 = 0$ V and $SW_{out} = V_{in}$. We mention the V_{in} level for this transition as the "turn-on threshold voltage V_{on}". SW_{out} is the output of this voltage detector circuit that controls the connection between the capacitor (power source part) and the load (power-consuming part). In the configuration shown in Fig. 2, the CMOS switch between the capacitor and the load is connected and the electric power is delivered from the capacitor to the target load circuit.

At the same time, $V_2 = 0$ turns on M_{p5} and activates the additional pathway in the first-stage switch. The additional current path configured by M_{p4} and M_{p5} gives additional conductivity between the V_1 node and V_{in}, which helps to keep V_1 high (= V_{in}).

In most cases, the photocurrent available from the powering PV cells is smaller than the current that flows into the load circuit, and it causes a discharge of the capacitor and a decrease in V_{CAP} (= V_{in}). However, since the M_{p4}–M_{p5} current path is activated, the first-stage switch does not turn off at V_{on}. The first-stage switch turns off at V_{off}, which is lower than V_{on}.

Figure 4 shows an experimentally obtained cyclic operation between the charging phase and the discharging phase. V_{CAP} (= V_{in}) repeatedly goes up to V_{on} and down to V_{off} during the operation. The charging time depends on the photocurrent from the powering PV cells, thus illuminating the cells. Figure 5 shows the start-up charging time as a function of the charging current. The start-up charging time is the time to charge the capacitor from $V_{CAP} = 0$ to V_{on}. The start-up charging time in Fig. 5 was measured in a bench-top evaluation using a current source to charge the capacitor and voltage sources to provide V_{bn} and V_{bp}. We obtained 2 µA as the minimum charging current for the automatic charge and discharge operation. The voltage detector shown in Fig. 3(a) did not correctly work with a current smaller than 2 µA.

The hysteresis of the first-stage switch, thus, the mismatch between V_{on}–V_{off}, determines what amount of charge will be provided from the capacitor to the load circuit. The capacitance C and the impedance of the load circuit also affect the operation duration of the load circuit.

Figure 6 shows the threshold voltages (a) V_{on} and (b) V_{off}, and (c) hysteresis V_{on}–V_{off} as functions of V_{bn} and V_{bp}. As shown in Figs. 6(a) and 6(b), the threshold voltages depend on both V_{bn} and V_{bp}. We can adjust V_{on} and V_{off} by changing the bias conditions. On the other hand, as shown in Fig. 6(c), the hysteresis V_{on}–V_{off} is almost independent of V_{bp}. In fact, although V_{on}–V_{off} slightly depends on V_{bn}, it is difficult to change V_{bn} only to adjust the hysteresis. An increase in V_{bn} causes a larger continuous current during the operation and a poor circuit performance.

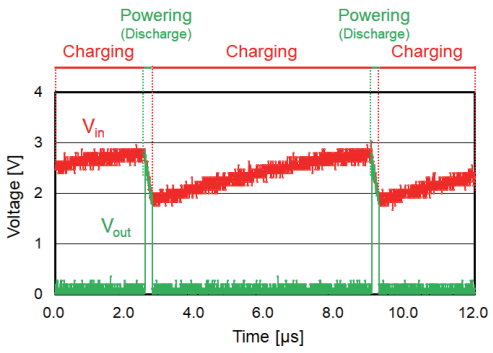


Fig. 4. (Color online) Experimental trace showing the charge and operation cycle.

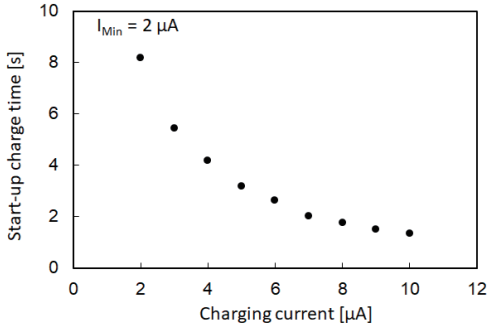


Fig. 5. Start-up charging time as a function of charging current.

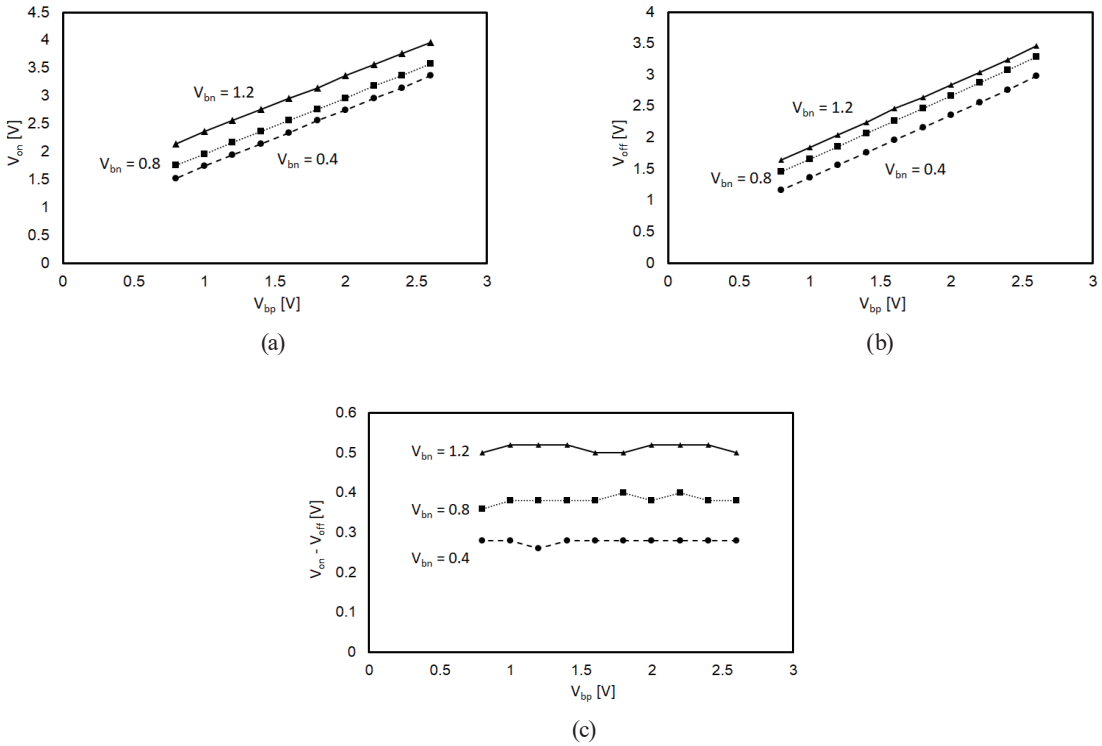


Fig. 6. Threshold voltages (a) V_{on} and (b) V_{off}, and (c) hysteresis V_{on}–V_{off} as functions of V_{on} and V_{bp}.

3. Design Optimization of the Voltage Detector Circuit

3.1 Design issues to be resolved

As presented in the previous section, although the CMOS-controlled optical power receiver platform shown in Fig. 3(a) works as we expected, there are two issues to be improved. The first issue is that the minimum charging current to obtain the expected operation is as large as 2 μA. In a previous work,[15] we used externally configured 0.8 × 0.9 mm^2 Si photodiodes as the PV cells. A photocurrent on the order of μA or even larger is available from the Si PV cell chip, and we can drive an optical ID transmission circuit with the proposed PV optical power transfer scheme. As next-generation optically powered, batteryless microdevices, we plan to use on-chip photodiode structures as integrated PV cells. The photocurrent available from the integrated PV cell is expected to be significantly smaller than that from the above-mentioned Si PV cell. We need to improve the circuit to reduce the minimum operating current.

The other issue is that we cannot adjust the hysteresis V_{on}–V_{off}. Once the circuit is designed, V_{on}–V_{off} scarcely depends on the bias voltages V_{bn} and V_{bp}. In other words, we cannot set V_{on} and V_{off} independently. To apply this platform to various target functions, we need to realize the mutually independent adjustment of V_{on} and V_{off} by changing the bias voltages. In this section, circuit modifications to overcome these two issues are described.

3.2 Introduction of current-limiting MOS transistors and reduction in minimum operating current

In general, a CMOS logic circuit such as a CMOS inverter employed in the current voltage detector does not require a continuous current flow in the steady state. The current flows only in transition of the logic states. Some circuit simulations revealed that the instantaneous current flow during the transition causes incomplete turning-on and the circuit stacks in a metastable state. With a small input current, as long as the CMOS voltage detector is in the off-state and the CMOS switch is opened, the photocurrent can charge the capacitor. This is because all the digital circuits are in the steady state and the total current for the CMOS circuit is very low. However, once V_{CAP} reaches V_{on}, the CMOS voltage detector starts to transit from the off-state to the on-state. The digital circuits in the voltage detector drain all the photocurrent generated in the powering PV cells. Under a low-current condition, the voltage detector circuit cannot complete the transition from the off-state to the on-state and the CMOS switch between the capacitor and the load is still opened. V_{CAP} can neither go up to complete the transition nor drop down to restart the charging, because the current does not flow into the load circuit. This is the reason why the minimum operating current is as large as 2 μA for the circuit shown in Fig. 3(a).

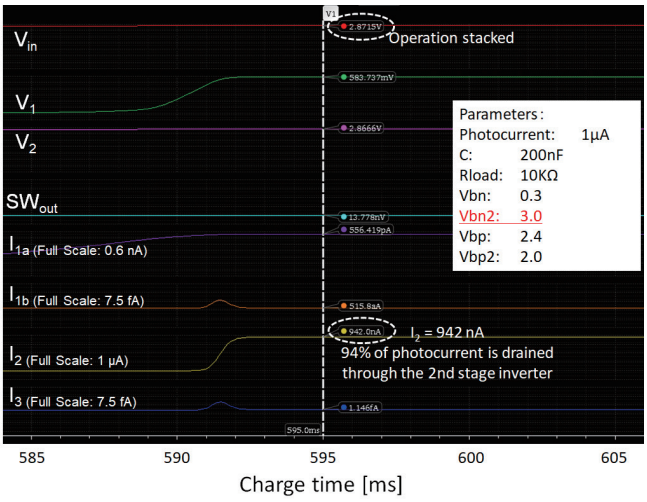
The straightforward solution to overcome this issue is to limit the transition current of the CMOS circuits. In the revised circuit design [Fig. 3(b)], we introduced additional NMOS transistors (current-limiting NMOS transistors) in each of the inverter structures in Fig. 3(a). In the circuit shown in Fig. 3(b), all NMOS transistors were designed as W/L = 1.0 μm/0.5μm, and all PMOS transistors were designed as W/L = 2.0 μm/0.5 μm.

To understand the effects of current limitation, we performed simulations for a slightly modified circuit from Fig. 3(b). We applied a separate bias voltage V_{bn2} to gates of the current-limiting NMOS transistors (M_{n4} and M_{n5}). This means that V_{bn} is applied only to the gate of the M_{n1} transistor. Figure 7 shows the simulated transient traces indicating voltages and currents on the circuit. The traces are plotted around the switching operation. In Fig. 7(a), V_{bn2} is set as 3.0 V, with which current is not limited. Once V_{in} reaches V_{on} (around 2.8 V in this case), the current flow through the second-stage inverter (I_2) increases and most of the photocurrent (1 μA) is drained through the second-stage inverter. This prevents the circuit from the expected turn-on operation and no pulse is generated. On the other hand, with V_{bn2} = 0.3 V, in the switching operation, I_2 only shows a short spike with a peak current of approximately 150 nA, and the circuit correctly generates a pulse. With the gate voltage of 0.3 V, the current-limiting NMOS transistors successfully limit the transition current of the inverter circuits.

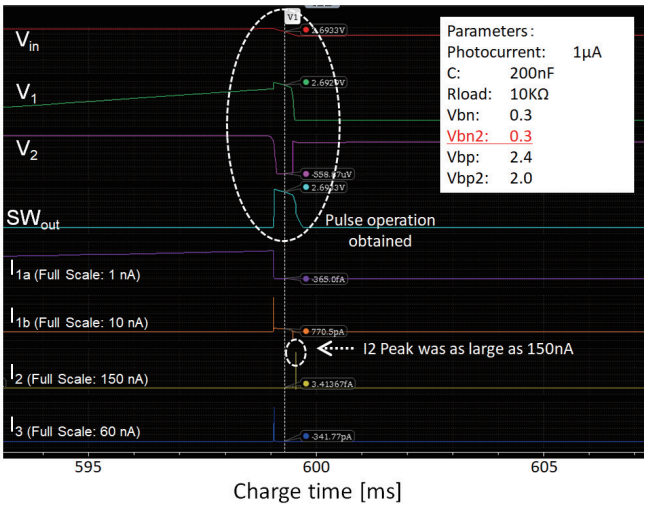
From the viewpoint of voltage availability from the serial-connected PV cells for biasing, a single-PV cell level (~0.4 V) was chosen as the bias voltage V_{bn} for the current-limiting NMOS transistors. Simulations suggest that the circuit works with an operating current of 200 nA from the powering PV cells.

3.3 Introduction of additional bias voltage for independent setting of V_{on} and V_{off}

In the previous design [Fig. 3(a)], the hysteresis of the first-stage switching circuit is realized with the additional current path that is activated only in the on-state. We applied the same bias



(a)



(b)

Fig. 7. (Color online) Simulated circuit operation shown in Fig. 3(b): (a) without and (b) with current-limiting condition.

voltage V_{bp} to both PMOS transistors (M_{p1} and M_{p4}). Simulations suggested that separating the gate voltages of these two PMOS transistors makes it possible to change V_{on} and V_{off} independently. Thus, we introduced the second PMOS bias V_{bp2} only for M_{p4}, as shown in Fig. 3(b).

4. Chip Implementation and Experimental Evaluation

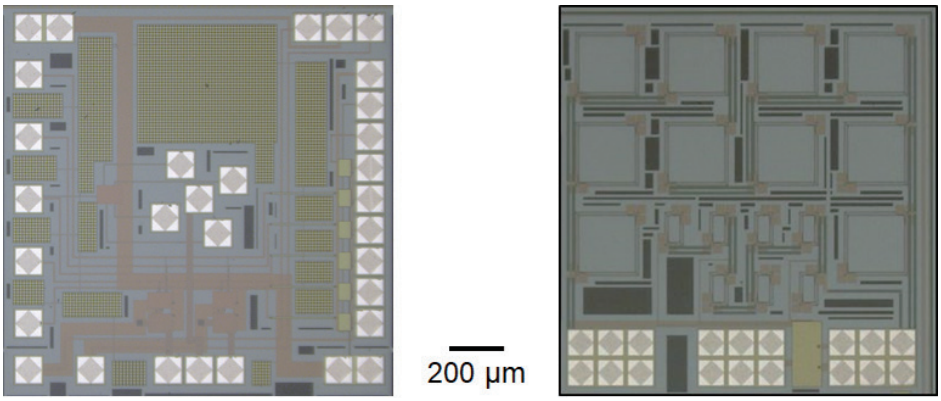
4.1 CMOS chip design

On the basis of the optimization described in the previous section, we designed two CMOS chips for evaluation and demonstration. We used a 0.35 μm 2-poly, 4-metal standard CMOS

process. Figure 8 shows layouts of the CMOS chips. Table 1 shows the specifications of the chips.

Chip-A is a voltage-monitoring circuit [see Fig. 3(b)] for evaluating the reduction in operating current and improving the adjustability of the threshold voltages. Chip-B is the integrated optical power receiver/energy-harvesting chip. We integrated the voltage detector and the CMOS switch with integrated PV cells. We used an N-well/P-sub photodiode structure commonly available in standard CMOS processes as the on-chip PV cell. Two sets of series-connected on-chip PV cells were integrated on chip-B. The first set is composed of 10-series-connected PV cells with a size of 270 × 270 μm^2 for powering. The photocurrent from the anode terminal of the 10th PV cell is accumulated in a capacitor. Since approximately 0.4 V is available from a single PV cell, we expect that more than 4 V will be available from the powering PV cells. The second set is composed of 7-series-connected PV cells with a size of 120 × 170 μm^2. We call such PV cells as the biasing PV cells. We took the bias voltage from the intermediate nodes of the biasing PV cells. We took approximately 0.4 V from the PV × 1 node for V_{bn}, 2.0 V from the PV × 5 node for V_{bp2}, and 2.8 V from the highest (7th) node for V_{bp}. These bias connections were chosen on the basis of simulations and data obtained experimentally with chip-A, which will be described in Sects. 4.2 and 4.3.

The optimized circuit shown in Fig. 3(b) was characterized with Chip-A. All the bias levels (V_{bn}, V_{bp}, and V_{bp2}) were supplied from a DC voltage source. Figure 9 shows setups for evaluation. To evaluate the operating current described in Sect. 4.2, a 1–10 μF capacitor was connected between V_{in} and GND and a resistor load was connected between V_{out} and GND. We used a current source connected between V_{in} (V_{CAP}) and GND to charge the capacitor. On the other hand, to evaluate the threshold voltages (Sect. 4.3), the experiment was performed without the capacitor and resistor load. We simply applied a triangular voltage wave from a function generator to identify the switching threshold voltages V_{on} and V_{off}.



(a) (b)

Fig. 8. (Color online) Layouts of the CMOS chips for (a) Chip-A, evaluation of the improved voltage monitoring circuit and (b) Chip-B, functional demonstration.

Table 1
Specifications of the CMOS chips.

	Chip-A	Chip-B
Layout	Fig. 8(a)	Fig. 8(b)
Process	0.35 μm, 2-poly, 4-metal standard CMOS process	
Standard voltage	3.3 V	
Target operating voltage	2.5–3.5 V	
Purpose	Circuit evaluation	Demonstration (LED drive)
Chip size	1.25 × 1.25 mm^2	1.25 × 1.25 mm^2
Voltage detector circuit	1	1
Integrated on-chip PV cells	0	17
V_{in} and bias voltages	Externally provided	Internally provided

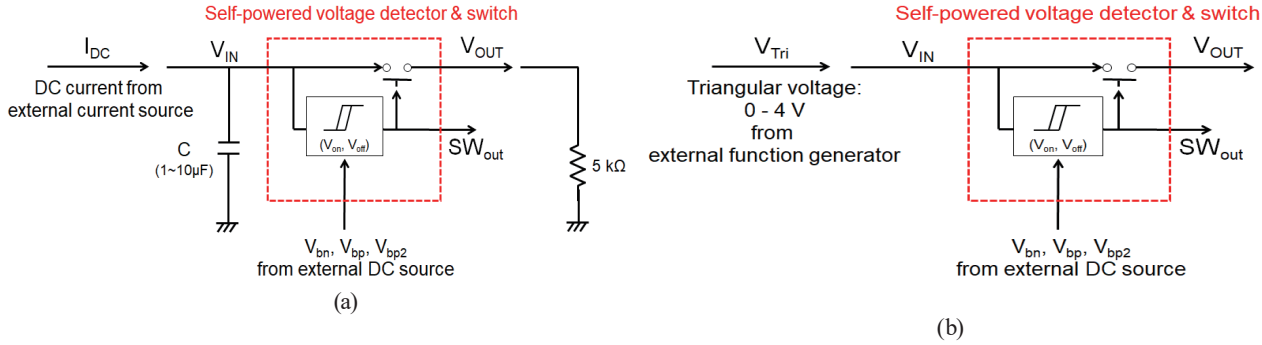


Fig. 9. (Color online) Experimental setups for measurements of (a) minimum operating current and (b) V_{on} and V_{off}.

4.2 Small current operation of the CMOS energy-harvesting switch

With the setup shown in Fig. 9(a), we evaluated the minimum operating current. We set V_{bp} = 2.8 V and V_{bp2} = 2.0 V, and changed V_{bn} from 0 to 1.2 V. We measured the minimum operating current at which automatic switching between V_{on} and V_{off} is available. Figure 10 shows the dependence of the minimum operating current on V_{bn}. The minimum operating current strongly depends on V_{bn}. The smaller the V_{bn}, the larger the current-limiting effect. We obtained an operating current of 370 nA with V_{bn} = 0.4 V. This operating current is approximately one order smaller than 2 μA, which was obtained with the previous circuit design [Fig. 3(b)].[15] This results shows that the introduction of the NMOS for the current-limiting is effective in realizing the low-current operation. The minimum operation current is determined mainly by the current flowing either of the current-limiting NMOS transistors (M_{n4} or M_{n5}). These transistors are in the subthreshold region throughout the operation. We consider that mismatch between the minimum operating current obtained in the simulation (200 nA) and that in the experiments (370 nA) is caused by process fluctuation in the CMOS technology.

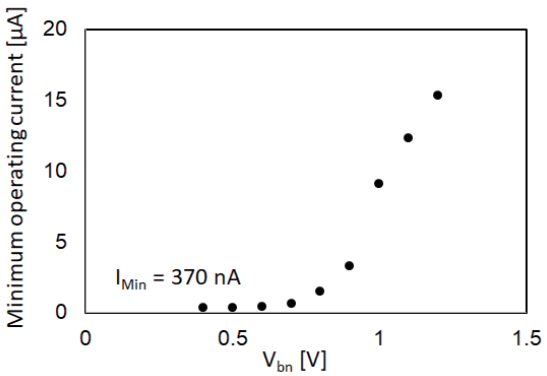


Fig. 10. Minimum operating current as a function of V_{bn}.

4.3 Adjustability of threshold voltages

Figure 11 shows V_{on} and V_{off} as functions of (a) V_{bp} and (b) V_{bp2}. For Fig. 11(a), V_{bp2} was fixed at 2.0 V. For Fig. 11(b), V_{bp} was fixed at 2.8 V. To understand the characteristic of the circuit, we need to add a condition. In a real operation, V_{bp} should be higher than V_{bp2} based on the circuit architecture. With this additional condition, the bias voltage ranges of $V_{bp} > 2.0$ V in Fig. 11(a) and $V_{bp2} < 2.8$ V for Fig. 11(b) should be discussed. In Fig. 11(a), V_{on} linearly increases with V_{bp} in the whole voltage range. On the other hand, when we focus on the voltage range with $V_{bp} > 2.0$ V, V_{off} does not depend on V_{bp}. This means that only V_{on} can be adjusted by changing V_{bp}, and V_{off} is independent of V_{bp}. On the other hand, in Fig. 11(b), V_{on} does not depend on V_{bp2}, and V_{off} linearly increases with V_{bp2}. This result suggests that V_{off} is solely adjustable by changing V_{bp2} and that V_{on} is independent of V_{bp2}. We can conclude that the introduction of V_{bp2} to bias M_{p4} leads to the separated adjustabilities of V_{on} and V_{off}.

A small fluctuation in V_{on} up to approximately 0.2 V in Fig. 11(b) was observed. From a viewpoint of the concept of the system, this level of fluctuation causes no problem. One of the core advantages of the present wireless optical powering architecture is its adaptability to a wide illumination intensity range. The powering pulse is a simple discharging pulse taken from a capacitor and not regulated. Furthermore, as mentioned in Sect. 2, we obtain bias voltages from the second set of PV cells whose voltages slightly depend on illumination. We accept fluctuations in pulse parameters, such as initial (~V_{on}) and final (~V_{off}) voltages, pulse duration, and voltage transient of the powering pulse. V_{on} and V_{off} should be configured within an operating voltage range of the target circuit. At the same time, the target circuit should be sufficiently voltage-tolerant to work with the nonuniform, unstable powering pulse. We design systems with typical voltage ranges larger than 1 V[14,15,18] and the fluctuation of 0.2 V is acceptable for our applications.

4.4 Application demonstration: implantable optogenetic stimulator

After the characterization with the voltage switching circuit, we designed the CMOS power-receiving chip shown in Fig. 8(b).[18] To use chip-B, we need to separate the on-chip PV cells

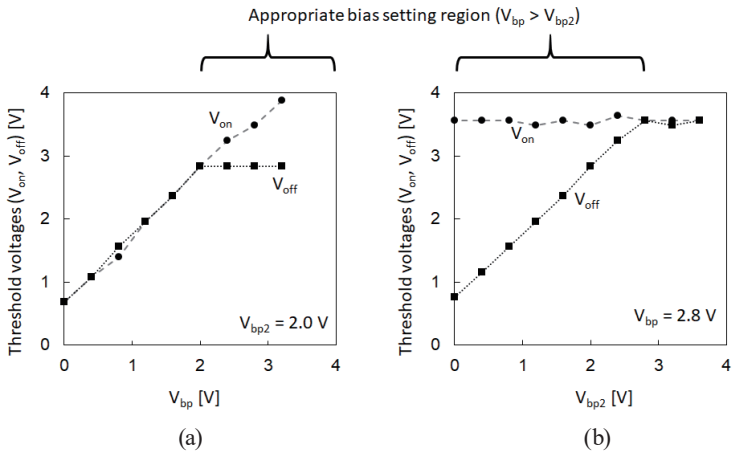


Fig. 11. V_{on} and V_{off} as functions of (a) V_{bp} and (b) V_{bp2}. V_{bp2} was fixed at 2.0 V for (a) and V_{bp} at 2.8 V for (b).

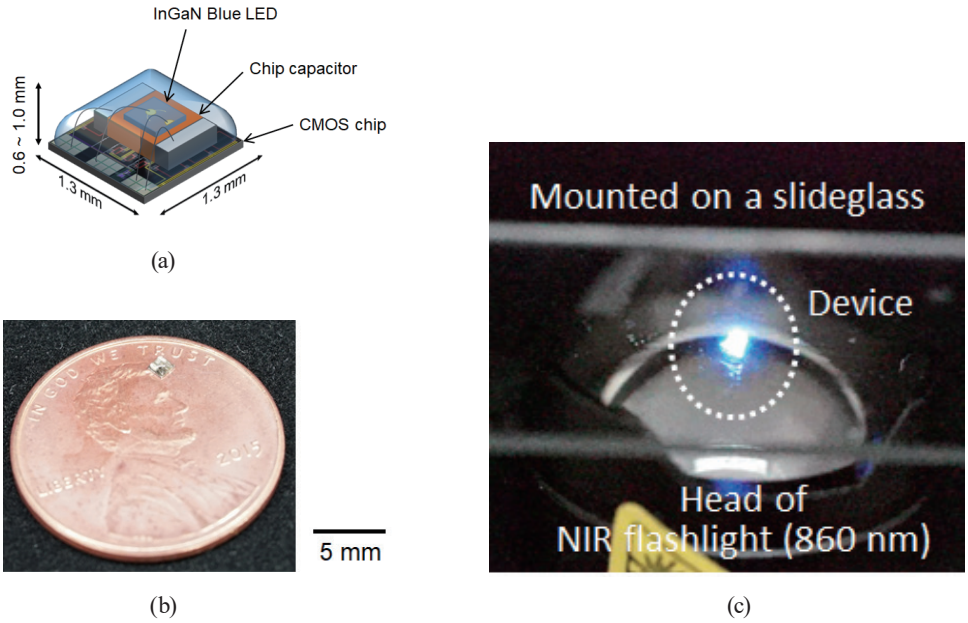


Fig. 12. (Color online) (a) Structure and (b) outlook of a batteryless implantable optogenetic neural stimulator based on the proposed CMOS-based optical power transfer platform. (c) A photograph of the device under operation.[18]

using the Bosch process. We described the process and integration of the chip with a capacitor and an InGaN blue LED in Ref. 18. Figure 12 shows an implantable optogenetic stimulator with the CMOS integrated PV power-receiving chip.[18] The volume of the device is approximately 1 mm^3 and the weight of the device is as small as 2.3 mg. Figure 12(c) shows a photograph of the device under operation. The device was placed on a slide glass and illuminated by a NIR flash light with a peak emission wavelength of 860 nm. As shown in Fig. 12(c), we successfully drove a blue LED. The peak illumination intensity was higher than 10 mW/mm^2 and the pulse

duration is longer than 1 ms. Detailed characteristics are presented in Ref. 18. We expect to apply this device to a research field of optogenetics.

5. Conclusions

In this work, we optimized a CMOS circuit design for an optical power transfer/energy-harvesting platform. The proposed optical power transfer/energy-harvesting platform is designed with a concept of a cyclic operation between the accumulation of PV current in a capacitor and the intermittent operation of the target circuit. The proposed technology is suitable for various types of implantable bioelectronics and IoT micronodes.

On the basis of our previous work, we refined the CMOS circuit to obtain a reduced operating current and flexible adjustability of the switching voltages. We introduced current-limiting NMOS transistors for the reduction in operation current and an additional bias voltage for separate adjustabilities of the turn-on and turn-off voltages of the voltage detector.

We implemented the refined CMOS circuit in a real chip and obtained successful results for the two issues. Finally, we briefly mentioned the implantable optogenetic stimulator, which is realized with the CMOS circuit optimized in this work.

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