Sensors and Materials, Vol. 30, No. 12 (2018) 2905–2917
MYU Tokyo

S & M 1728

Fine Cone-shaped Bumps for Three-dimensional LSI Package— An Optimization of Thermocompression Bonding Process

Shunsuke Nemoto,[1*] Ying Ying Lim,[2] Hiroshi Nakagawa,[2]
Katsuya Kikuchi,[2] and Masahiro Aoyagi[1,2]

[1]Graduate School of Science and Engineering, Saitama University,
255 Shimo-Okubo, Sakura-ku, Saitama-shi, Saitama 338-8570, Japan
[2]Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology,
1-1-1 Umezono, Tsukuba-shi, Ibaraki 305-8560, Japan

(Received May 26, 2018; accepted August 8, 2018)

Keywords: flip-chip bonding, 3D LSI, nanoparticle deposition, cone-shaped bump

Fine cone-shaped bumps (6 μm) were fabricated by a nanoparticle deposition method, where the nanoparticles were deposited onto hole patterns defined in a photoresist. In this work, the goal is to minimize the flip-chip bonding force of LSI chips targeted for three-dimensional (3D) packages while optimizing the bonding strength. In particular, the effects of temperature on the bump compressive stress and shear strength were investigated in detail. From the results, it was found that the crystal grain size of cone-shaped gold bumps increases significantly at ≥150 °C, which in turn affects the mechanical properties of the bump. We also clarified the optimum connection conditions to simultaneously realize a low bonding force and an improved bonding strength by bonding at ≥200 °C.

1. Introduction

Multifunctional LSI chips with small footprints are desirable for consumer applications in the area of mobile, medical, and AI sensors. Three-dimensional (3D) LSI packaging is a promising approach to obtaining smaller footprints and higher densities, where the LSI chips are stacked in the vertical direction. A typical 3D LSI package is composed of stacked chips, which are connected using through silicon vias and microbumps. Work has been ongoing in the development of microbumps using a nanoparticle deposition (NPD) method.[1,2] A key advantage of NPD bumps is their compliance during compression, as the bumps are cone-shaped. Compared with copper pillar bumps, which may be noncoplanar owing to process tolerances, chip-to-chip connection during flip-chip bonding could be improved with NPD bumps. From our previous work,[1] 10 μm NPD bumps were flip-chip-bonded and the signal transmission was demonstrated between LSI chips. In addition, a detailed investigation of the compressive displacement of cone-shaped gold bumps (6 μm diameter) at room temperature was reported.[2] In an extension of the work done previously,[2] the effect of heat on the compressive stress is investigated in this work to understand the effects of heating on the bump strength and

*Corresponding author: e-mail: shun.linux@gmail.com
https://doi.org/10.18494/SAM.2018.2009

ISSN 0914-4935 © MYU K.K.
https://myukk.org/

hardness. The goal of this work is to optimize the bonding force and bonding strength, which affects the reliability of flip-chip connections.

2. Materials and Methods

2.1 NPD process

The NPD equipment used is composed of two chambers, namely a generation chamber (1600 °C, 30–90 kPa) where gold pellets are evaporated in helium gas to produce gold nanoparticles and a deposition chamber with a movable stage in the *X*-, *Y*-, and θ-axes (700 Pa). Owing to the pressure difference between the generation chamber and the deposition chamber, gold nanoparticles are carried from the generation chamber by the helium gas and ejected from the nozzle of the deposition chamber onto the substrate. Figure 1 shows the process of fabricating cone-shaped gold bumps where the nanoparticles are deposited onto hole patterns defined in a photoresist.

Table 1 shows the photolithography conditions for fabricating hole patterns of 6 µm diameter. Cone-shaped bumps are formed onto the hole patterns by this nanoparticle deposition process. A key feature of this deposition method is that nanoparticles are produced and deposited under a vacuum environment, which enables the bump dimensions to be better controlled, making fine bumps possible. After the deposition, excess metals are removed together with the photoresist using the lift-off process. After lift-off, only the cone-shaped bumps remain. A SEM image of a typical cone-shaped gold bump is shown in Fig. 2, which has a bump diameter of 6 µm and a bump height of 6 µm. This yields a bump aspect ratio of around 1.

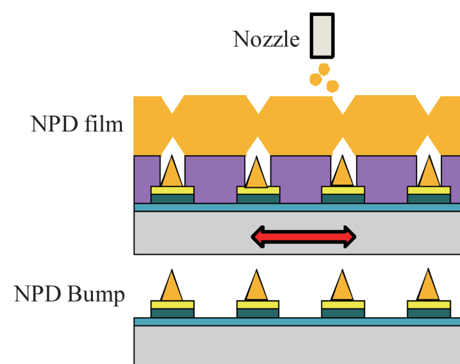

Fig. 1. (Color online) Process of fabricating cone-shaped gold bumps.

Table 1
Photolithography conditions for fabricating hole patterns of 5 µm diameter.

Spin coat	Merck AZP 4620, 3250 rpm
Prebake	110 °C, 5 min
Exposure	G-line stepper, 750 mJ
Development	Merck AZ300MIF 2.38, 3 min 30 s
Rinse	Ultrapure water, 1 min

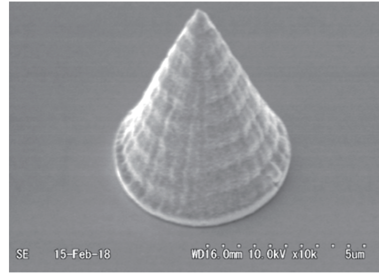

Fig. 2. SEM image of a cone-shaped gold bump.

2.2 Bump compression test

For the compression test of the cone-shaped gold bumps, a microindenter (Fischerscope H100C, Fischer Technology Inc.) was used. Single cone-shaped bumps were compressed using a diamond planar indenter (50 μm^2), and the samples could be heated up to 250 °C. Nemoto *et al.*[2] introduced an equation relating to the compressive load and the compressive displacement of a cone-shaped gold bump, which can be described as

$$\sigma = \frac{F\left(h_0\right)^2}{\pi\left(dr_0\right)^2}. \tag{1}$$

From Eq. (1), σ is expressed as the compressive stress of the bump, where F is the load applied, d the compression displacement, r_0 the radius of the base of the bump, and h_0 the initial bump height. To determine the compression displacement d, the bump height before compression was measured from SEM images, while the bump height after compression was determined using a laser microscope (LEXT OLS4000, Olympus). Owing to the sharp tip of the cone-shaped bump, the bump height before compression could not be accurately captured using a laser microscope. This could be attributed to the laser beam size (minimum, 0.2 μm), which could be in the same order of magnitude as the bump tip size. Similarly, the radius r_0 of the bottom surface of the bump was obtained from SEM images. Table 2 shows the conditions for the bump compression test, where the test temperature was defined as the temperature of the stage onto which the silicon chip was placed.

During the bump compression test, a constant compression rate was applied until the desired load was reached after which the pressure was reduced. Three bumps were measured at each test temperature for a duration of 10 min.

2.3 Resistivity characterization

Figure 3 shows the setup used to characterize the resistivity of a gold film deposited by NPD onto a silicon chip. A four-point probe circuit was used with the metallization induced by Ti/Au deposition (20/500 nm). The width of the NPD film shown in Fig. 3 was 198 μm, with a length

Table 2
Bump compression test conditions.

Subject	Process condition
Test temperature (°C)	25, 50, 100, 150, 200, 250
Pressurization rate (mN/s)	1
Loading condition (mN)	10 (25–150 °C), 7 (200–250 °C)
Retention time (s)	30
Depression rate (mN/s)	−1

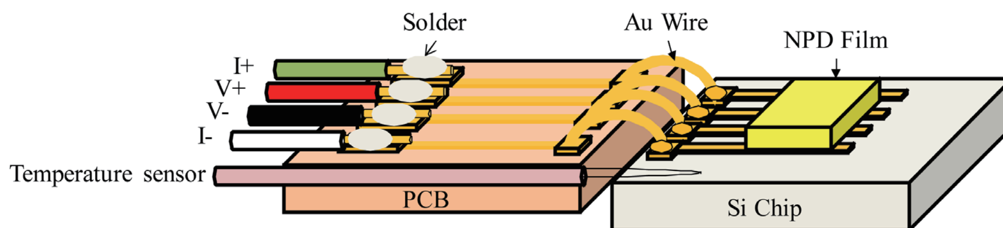

Fig. 3. (Color online) Setup for evaluating temperature dependence of NPD film resistivity.

of 381.0 μm and a thickness of 5.4 μm. The silicon chip was then mounted onto a flexible substrate and a high-temperature solder was used to connect the pads on the flexible substrate to the *I*–*V* terminals of the four-point probe measurement equipment. In addition, another four-point probe circuit was designed on the same silicon chip to evaluate the resistance of Ti/Au metallization (width 10 μm, length 27 mm).

2.4 Shear test

A bond tester (4000Plus Bondtester, Nordson Dage Ltd.) was used to perform the bump shear test of the cone-shaped gold bumps. The gold bumps were designed at a pitch of 150 μm such that single bump testing is possible. Prior to the shear test, the silicon chip was placed onto a hotplate and heated over a temperature range of 100–250 °C, with a duration of 30 s at each temperature point. Subsequently, the chip was placed onto a stainless steel stage (24 °C) for cooling to room temperature. During the shear test, the test height was set at 1 μm, and the test was performed at a speed of 1 μm/s.

2.5 Bump height compression using a flip-chip bonder

To compare the compressed bump height using a microindenter with the bump height obtained after flip-chip bonding, a silicon chip with an area array of 10000 bumps was evaluated. The chip was pressed in a flip-chip bonder (CA300SS, PMT Corporation) at room temperature (27 °C) and 200 °C for a duration of 30 s at each temperature point. After flip-chip bonding, the heights of around 100 bumps were measured. The planarity obtained from the flip-chip bonder is ≤1 μm/10 mm.

2.6 Flip-chip bonding for daisy chain

Flip-chip bonding was performed on a sample containing 40000 cone-shaped bumps to measure the total resistance. A daisy chain structure was designed for measurement using the four-point probe method. The sample is composed of two silicon chips for flip-chip bonding. The top chip with NPD bumps was attached to the ceramic heater of the flip-chip bonder, while the bottom chip designed with daisy chain interconnects was placed onto the stage of the bonder. Prior to bonding, surface treatment was performed for both chips to remove possible contaminations on the chips. The plasma cleaning involved the use of oxygen (20 W, 20 Pa, 200 s) and argon gas (50 W, 1 Pa, 180 s).

Figures 4(a) and 4(b) show the conditions used for the flip-chip bonding. During the flip-chip bonding, the top and bottom chips were first brought into contact, after which the load was then increased to 210 N. As the load was applied, the temperature of the ceramic heater was increased to 300 °C at a rate of 17.5 °C/s [shown in Fig. 4(a)] and kept constant for 30 s. As the heater was attached only on one side of the flip-chip bonder, a temperature difference was observed between the set temperature and the actual bonding temperature. To compensate for the temperature difference, the temperature of the ceramic heater was set to 300 °C to obtain a measured temperature of 200 °C between the top and bottom chips during bonding.

3. Results and Discussion

3.1 Compression test

Figure 5 shows the temperature dependence of compressive stress obtained from the compression test. From the results shown in Fig. 5, the bump shows a compressive stress of ≥1000 MPa over a temperature range from 25 to 150 °C. At temperatures ≥200 °C, the compressive stress decreases to ≤700 MPa. From the results shown in Fig. 5, an increase in temperature during the bump compression test could have affected the crystal grain size in the bump, thus resulting in a decrease in compressive stress. Furthermore, measurements of

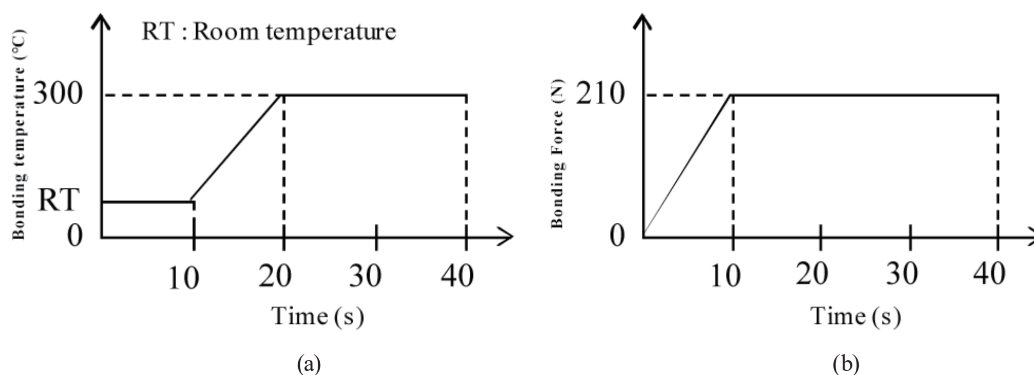

Fig. 4. Conditions for flip-chip bonding. (a) Bonding temperature and (b) bonding force.

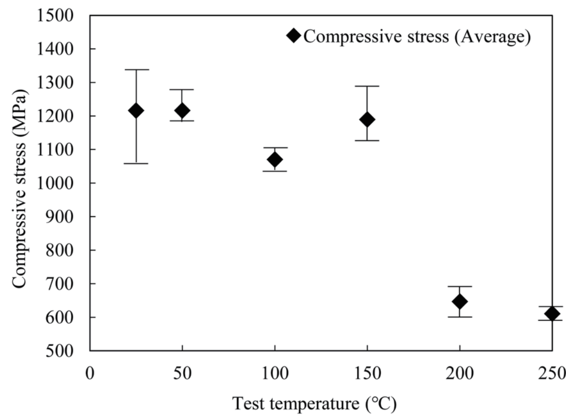

Fig. 5. Temperature dependence of bump compressive stress.

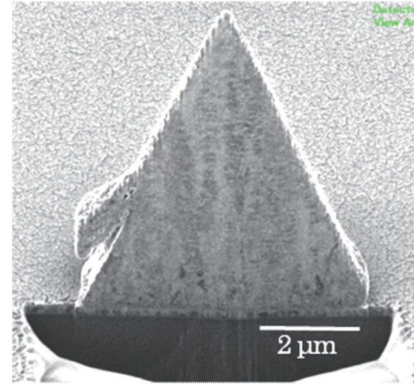

Fig. 6. Cross-sectional SIM image of a cone-shaped gold bump.

Table 3
Bump dimensions before and after heating.

	Bump diameter (μm)	Bump height (μm)
Before heating	5.6	6.3
After heating	5.6	6.1

the bump profile before and after heating (Table 3) indicate that the bump dimensions remain unchanged after heating. This implies that the influence of the bump profile on the variation in compressive stress is minimal.

The crystal grain size has a major influence on the mechanical properties of metals, which can be understood from the Hall–Petch relationship,(3,4) as shown in Eq. (2).

$$\sigma = \sigma_0 + \frac{k}{\sqrt{d}} \tag{2}$$

From Eq. (2), σ is the yield stress, σ_0 the yield stress of the single crystal, k the material constant, and d the average grain diameter of the grain boundary. In addition, Nieh and Wadsworth(5) have reported the dependence of strength and deformation behavior on the particle size where the crystal grain size is classified into the following three categories: macrocrystal (≥1 μm), submicron crystal (~1 μm), and nanocrystal (~10–20 nm).

Figure 6 shows the cross-sectional image of a cone-shaped gold bump prior to heating. The main crystal grain size of the bump was found to be several tens of nanometers, up to a maximum value of around 200 nm. From Fig. 6, nanocrystals and submicron crystals were observed in the cone-shaped gold bumps in the initial state (i.e., before heating).

Recrystallization is a process where grains of a crystal structure form new crystal shapes and the recrystallization of grain boundaries occurs when a constant thermal energy is applied. In

order to understand the effects of heating on the bump strength and hardness, there is a need to determine the temperature at which recrystallization occurs (i.e., recrystallization temperature). This is done by evaluating the resistivity of a thin film. The evaluation of resistivity is based on the assumption that small crystal grain sizes result in a higher degree of grain boundary scattering, which in turn causes an increase in metal resistivity and vice versa. Equation (3) shows the effect of temperature on resistivity.

$$\rho(T) = \rho_0 + \alpha(T - T_0) \tag{3}$$

From Eq. (3), ρ is the resistivity (Ω·m), T is the temperature (°C), T_0 is the reference temperature (°C), ρ_0 is the resistivity (Ω) at T_0, and α is the rate of change in resistance per unit temperature (Ω·°C^{-1}). To determine $\rho(T)$, the resistivity of a NPD film was characterized using the procedure described in Sect. 2.3. The film was heated from room temperature to 200 °C at a rate of 1.2 °C/min.

Figure 7 shows the temperature dependence of the resistivity of the NPD film. From 24 to 138 °C, the resistance increased linearly with the temperature. However, from 138 to 150 °C, the resistance was observed to decrease. In the temperature range from 150 to 200 °C, the resistance was observed to increase with the temperature proportionally. When cooling was performed from 200 to 24 °C, no transition was observed. In the cooling stage, the temperature and resistance were observed to be linearly proportional as shown in Fig. 7. From Eq. (3), α was found to be constant except in the vicinity of the transition and calculated to be $8.6 \times 10^{-9} \pm 0.2$ Ω·cm·°C^{-1}. However, the measured resistivity $\rho(T)$ values of the film at 24 °C before and after heating were 3.0×10^{-6} and 2.6×10^{-6} Ω·cm, respectively. With reference to Eq. (3) the change in $\rho(T)$ implies that the crystal grain size has increased in the transition region (138–150 °C). Although the typical annealing temperature of gold is less than 200 °C,[6] the results obtained indicate that annealing could be induced below 200 °C.

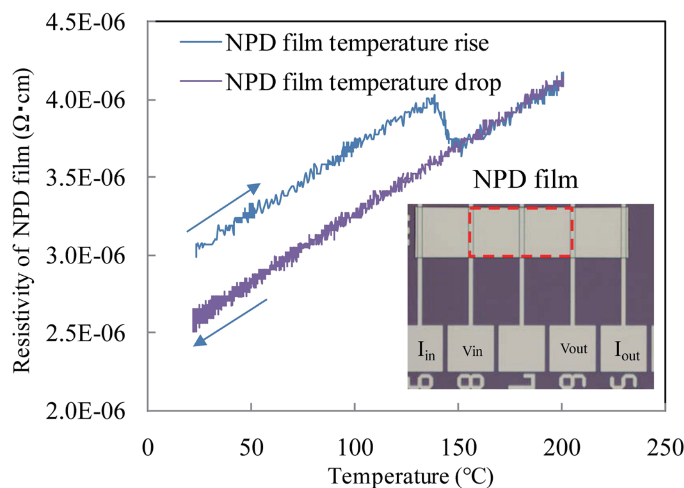

Fig.7. (Color online) Temperature dependence of the resistivity of NPD film.

To evaluate the crystal grain boundary, the cross section of a sample after flip-chip bonding was evaluated. Flip-chip bonding was performed at a temperature of 200 °C for 30 s, with a load of 5.4 mN/bump applied during bonding. The cross section of the bump-pad interface after flip-chip bonding is shown in Fig. 8. From the figure, the particle diameter of the crystal grain boundary along the red line was estimated. Assuming similar crystal grain sizes, the maximum width of the crystal grain size in Fig. 8 would be at the center of the crystal grain boundary and the minimum width would be at the edge of the grain boundary. As such, the average width can be expressed as a normal distribution at 50%, and the grain diameter is $2/\sqrt{3}$ times the average grain size. From the calculations, the average crystal grain size is around 386 nm.

3.2 Shear test

Figure 9 shows the variation in bump shear strength with respect to temperature. For a typical bump at room temperature, the bump shear strength is around 5 mN. Upon heating to 100 °C, the mechanical strength is observed to be lower than that of the nonheated bump. However, as the heating temperature is increased, the bonding strength is observed to improve. At 250 °C, the bump shear strength (5 mN) is similar to that under the initial condition.

From the results obtained, the fracture interfaces across the temperature range were similar, as shown in the photograph in Fig. 9. From SEM results, each interface was observed to be formed at an average height of 156 nm from the bump pad. As the shear test was performed at a height of 1 μm from the bump base at each temperature point, it can be implied that the stress was concentrated at the same place. Thus, the difference in bump shear strength across the temperature range could be due to the recrystallization of the thin NPD film from 138 to 150 °C, as discussed in Sect. 3.1.

Chauvineau *et al.*[7] have reported the occurrence of recrystallization in a thin gold film from 80 to 150 °C. The results in Fig. 10 show a similar trend, where the resistance of a Ti/Au film

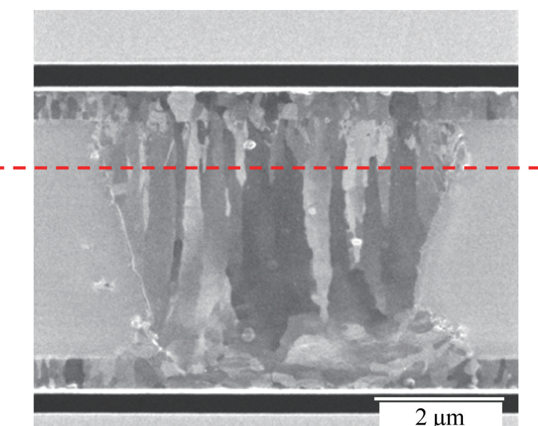

Fig. 8. (Color online) Cross section of the bump-pad interface after flip-chip bonding. The red dashed line indicates the location used for crystal size measurements.

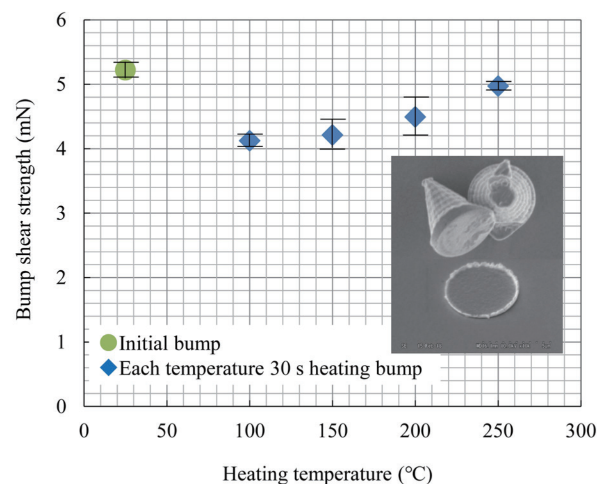

Fig. 9. (Color online) Temperature dependence of bump shear strength.

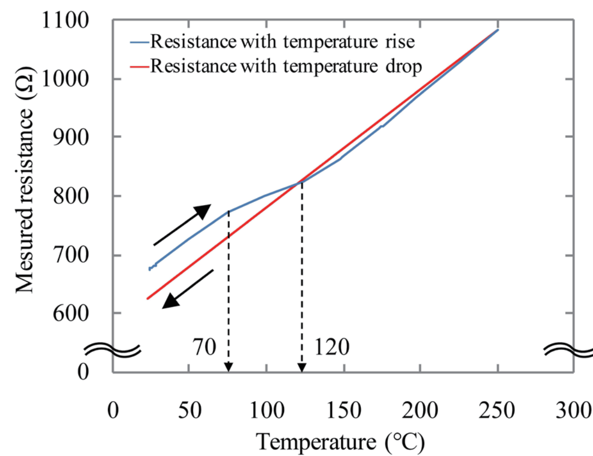

Fig. 10. (Color online) Temperature dependence of gold film resistance.

(described in Sect. 2.3) was characterized from room temperature to 250 °C. The thickness of the Ti/Au film was 20/500 nm. The results in Fig. 10 show a transition in resistance between 70 and 120 °C. With reference to Fig. 9, these results imply the onset of recrystallization at around 100 °C near the bump-pad interface, where the bump shear strength was observed to decrease. As the temperature increased beyond 100 °C, the crystal defect density in the NPD bump possibly decreased owing to the recrystallization effect, which resulted in an improved bump shear strength.

3.3 Load dependence of bump height

Figure 11 shows the load dependence of heights of area array bumps versus those of single bumps, using the procedure described in Sect. 2.5. The dotted lines show the bump heights calculated using the compressive stresses obtained from the microindenter measurements at 25 and 200 °C. From Fig. 11, a good correlation could be observed between the calculated and measured results.

Table 4 shows the calculated and measured bump heights. The measured bump heights were determined from cross-sectional photographs of bumps flip-chip-bonded under the conditions described in Sect. 2.5. From Table 4, the design values were found to agree well with the measured values, with an obtained variation ≤0.6 μm.

3.4 Electrical connection after flip-chip bonding

Flip-chip bonding (200 °C, 30 s, 5.4 mN/bump) was performed on a sample containing 40000 cone-shaped bumps formed in an area array. The test conditions were described in Sect. 2. 6. Figure 12 shows the sample after flip-chip bonding. The bumps were connected in a daisy chain in 5000 × 8 blocks. Each block was measured separately for electrical connection. Finally, the entire block of the 40000 bumps was measured, with an obtained resistance of 3674

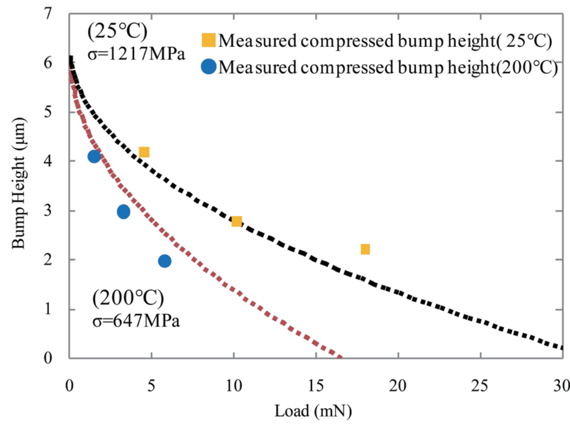

Fig. 11. (Color online) Load dependences of heights of area array bumps vs single bumps.

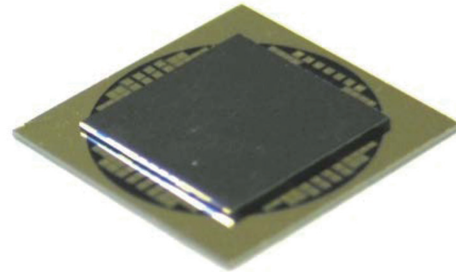

Fig. 12. (Color online) Photograph of the sample after flip-chip bonding.

Table 4
Calculated and measured bump heights.

Force	14.2 N	32.6 N	58.2 N
Design value (Bump press tester)	4.4 μm	3.5 μm	2.6 μm
Design value (Flip-chip bonder)	4.2 μm	3.1 μm	2.1 μm
Measured value	4.1 μm ± 0.1	3.0 μm ± 0.2	2.0 μm ± 0.3

Ω (estimated 92 mΩ/bump). The previous four-point probe characterization of a single bump yielded a resistance of 10 mΩ/bump. This implies that the estimated resistance of 92 mΩ/bump obtained from the daisy chain measurements includes the interconnect resistance and the contact resistance between the bump and the pads.

4. Conclusions

In this work, 6 μm cone-shaped bumps were realized using a NPD process. The effect of temperature on the bump compression process was investigated, with the goal of optimizing the load and bonding strength in flip-chip connections targeted for 3D LSI packages. The important results from this work are summarized below.

1) From the results of the bump compression test and the temperature dependence of the resistivity of the NPD film, the crystal grain size was found to have a significant effect on the compressive stress.
2) In the bump compression test, the bump sample was subjected to heating for 10 min. In contrast, the bumps were annealed for a short period (200 °C for 30 s) in the flip-chip bonding process. After bonding, bump connection was obtained using a low load of 5.4 mN/bump, which implies a low stress for LSI chips. The results suggest that short periods of heating suffice for obtaining bump connection.

3) From the bump shear results, a possible recrystallization near the bump-pad interface was observed at around 100 °C. At temperatures above 100 °C, crystal defects could have decreased owing to the recrystallization phenomenon, which resulted in an improved bump shear strength.
4) A daisy chain structure composed of 40000 bumps was measured using a four-point probe setup. The electrical connection for the structure was demonstrated, with a measured resistance of 92 mΩ/bump. The previous four-point probe characterization of a single bump yielded a resistance of 10 mΩ/bump. This implies that the estimated resistance of 92 mΩ/bump obtained from the daisy chain measurements includes the interconnect resistance and the contact resistance between the bump and the pads.

Acknowledgments

The authors would like to thank Mr. Yoshihiro Gomi from Mixnus Fine Engineering Co., Ltd. for sharing his expertise in the fabrication of nanoparticle bumps. Part of this work was conducted at the AIST Nano-Processing Facility, supported by the "Nanotechnology Platform Program" of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan.

References

1 F. Imura, S. Nemoto, N. Watanabe, F. Kato, K. Kikuchi, H. Nakagawa, M. Aoyagi, T. Morimoto, M. Hagimoto, H. Uchida, N. Hikichi, and Y. Matsumoto: Proc. 2012 JIEP Annual Meeting (JIEP, 2012) 266.
2 S. Nemoto, T. Bui, W. Feng, K. Kikuchi, F. Kato, H. Nakagawa, and M. Aoyagi: IEICE Trans. Electron. (Japanese Edition) **J99-C** (2016) 314.
3 W. Sylwestrowicz and E. O. Hall: Proc. Phys. Soc., London, Sect. B **64** (1951) 747.
4 N. J. Petch: J. Iron Steel Inst. **174** (1953) 25.
5 T. G. Nieh and J. Wadsworth: Scr. Metall. Mater. **25** (1991) 955.
6 G. Qi and S. Zhang: J. Mater. Process. Technol. **68** (1997) 288.
7 J. P. Chauvineau, P. Croce, G. Devant, and M. F. Verhaeghe: J. Vac. Sci. Technol. **6** (1969) 776.

About the Authors

Shunsuke Nemoto received his B.S. and M.S. degrees in Electronic Engineering from Iwaki Meisei University, Japan, in 2004 and 2006 respectively. From 2006 to 2009, he worked as a development engineer at the Alps Business Service Corporation. From 2009 to 2017, he worked in the Nanoelectronics Research Institute (NeRI) at the National Institute of Advanced Industrial Science and Technology (AIST), Japan. Since June 2017, he has been working as an engineer with the Process Engineering Department at Renesas Semiconductor Package & Test Solutions (RSPT) Co., Ltd., Japan. He is also currently a doctoral student at the Graduate School of Saitama University. (shun.linux@gmail.com)

Ying Ying Lim received her B.Eng. (Hons) and M.Eng. degrees in Electrical and Electronic Engineering from Nanyang Technological University, Singapore, and her Ph.D. degree in Mechanical and Manufacturing Engineering from Loughborough University, United Kingdom, in 2015. From 2005 to 2011, she worked as a research engineer at the Institute of Microelectronics (IME), A*STAR, Singapore, where she designed, simulated, and characterized high-frequency embedded passives for packaging. She also has experience in the high-frequency dielectric characterization of substrates and thin films. She is currently a postdoctoral researcher of the Nanoelectronics Research Institute (NeRI) at the National Institute of Advanced Industrial Science and Technology (AIST), Japan. Dr. Lim was the recipient of the Outstanding Student Paper Award at the Electronics Packaging Technology Conference (EPTC 2005) and the Best Interactive Poster Award at the Third International Conference in Advanced Manufacturing for Multifunctional Miniaturised Devices (ICAM3D-2014). Her current research interests lie in the areas of wearable electronics and high-density 3D system integration. (yingying.lim@aist.go.jp)

Hiroshi Nakagawa received his D.E. degree in Electronic Engineering from Tokyo University of Science, Japan, in 1996. He is currently a guest researcher of both the Nanoelectronics Research Institute and the Advanced Power Electronics Research Center at the National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan.
(h.nakagawa@aist.go.jp)

Katsuya Kikuchi received his B.S., M.S., and Ph.D. degrees in Electronic Engineering from Saitama University, Saitama, Japan, in 1996, 1998, and 2001, respectively. He joined the National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan, in 2001, where he has been engaged in the research of 3D integration system technologies. He is currently a group leader of a study on a 3D integration system at the Nanoelectronics Research Institute (NeRI), AIST, Tsukuba, Japan. His current research interests include design and fabrication techniques toward 3D integration systems with particular emphasis on power/signal integrity, testing, and diagnosis. He is a member of the Institute of Electrical and Electronics Engineers, the Japan Institute of Electronics Packaging, the Institute of Electronics Information and Communication Engineers, and the Japan Society of Applied Physics. (k-kikuchi@aist.go.jp)

Masahiro Aoyagi (M'94–SM'10) received his B.E. and D.E. degrees in Electronics Engineering from the Nagoya Institute of Technology, Nagoya, Japan, in 1982 and 1991, respectively. He joined the Electrotechnical Laboratory, Tsukuba, Japan, in 1982, where he has been engaged in the research and development of Nb, NbN superconducting devices, and Josephson integrated circuits. He was involved in a special section on Josephson computer technology from 1982 to 1994. He was a guest researcher of the National Physical Laboratory, Teddington, U.K., from 1994 to 1995. He was a group leader of a study of high-density interconnection at the Nanoelectronics Research Institute (NeRI), National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, from 2000 to 2010. He was also a group leader of the National R&D Projects of High-Density Electronic System Integration from 1999 to 2004 and Functionally Innovative 3D Integrated Circuit (Dream Chip) Technology from 2008 to 2012. He was the 3D integration system group leader of NeRI at AIST from 2011 to 2014. He is currently the Director of the Collaboration Promotion Unit with Tsukuba Innovation Arena (TIA) Central Office, AIST. He is also an affiliated professor of Graduate School of Science and Engineering, Saitama University. His current research interests include high-performance high-density 3D system integration technology. (m-aoyagi@aist.go.jp)