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Impedance-matched Planar-antenna-integrated High-efficiency Push-pull Power Amplifier with Center-tapped Transformer for 5 GHz Wireless Communication

Takeshi Kuboki,^{1*} Tomoki Sadakiyo,¹ Wee Sang Park,² and Haruichi Kanaya¹

¹Graduate School of Information Science and Electrical Engineering, Kyushu University, 744 Motooka, Nishi-ku, Fukuoka 819-0395, Japan

²Department of Electronic and Electrical Engineering, Pohang University of Science and Technology, 77 Cheongam-ro, Jigok-dong, Nam-gu, Pohang, Gyeongsangbuk-do, Republic of Korea

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We present a highly efficient power amplifier (PA) with an impedance-matched planar antenna. An impedance-matching network including inductors and capacitors is a common and essential practice for wireless communication systems; however, efficiency degradation at a matching network is a serious issue. We implement a matching block into a planar antenna and integrate a PA with the impedance-matched planar antenna. The impedance-matched antenna and PA are applied to a wireless transmitter for the 5 GHz band in a 0.18 mm CMOS. The proposed integrated PA has a power-added efficiency (PAE) of 15.7% in linear operation and a maximum PAE of 30.7%.

1. Introduction

Increasing demand for wireless communication systems has promoted intensive development to realize high data rates with quadrature amplitude modulation (QAM) and low-power circuit components. IEEE 802.11 wireless LAN for 5.2 GHz supports 7 Gb/s with 256-QAM.⁽¹⁾ Multilevel QAM requires high linearity of a power amplifier (PA). Therefore, the PA is a major source of power-dissipating components required to realize high linearity. Besides the need for a high data rate, there is also a strong demand for low power dissipation, especially for mobile communication devices. However, a general amplifier has a trade-off between high linearity and low power. We therefore need to design an efficient PA for wireless communication and some techniques are proposed to improve the efficiency of the PA.^(2,3)

The impedance-matching circuit of the PA is one of the elements capable of the highest power dissipation. Usually an impedance-matching circuit is designed to have the input and output impedances of 50 Ω ; however, it exhibits power loss that may reduce the efficiency of the transmitter.

^{*}Corresponding author: e-mail: kuboki@ed.kyushu-u.ac.jp https://doi.org/10.18494/SAM.2018.2025

In this paper, we propose a high-efficiency wireless transmitter with an impedance-matched antenna. Instead of an impedance-matching circuit of the PA, we place a matching block on the antenna with coplanar waveguide (CPW) matching.^(4,5) Unlike the widely used 50 Ω matching circuit of the PA, we can set the characteristic impedance between the PA and the antenna to values other than 50 Ω without the power loss of a matching circuit. We design a matching block of the antenna to maximize the efficiency of the transmitter. We also design a push-pull PA for the 5.2 GHz band with a center-tapped transformer in 0.18 mm CMOS. The transmitter including the proposed PA and antenna has a power-added efficiency (PAE) of 15.7% in linear operation and a maximum PAE of 30.7%.

The remainder of this paper is organized as follows. In Sect. 2, the proposed PA circuit is explained in detail. Section 3 describes the proposed antenna with an impedance-matching block. The simulated and measured results of the proposed transmission are explained in Sect. 4. Finally, in Sect. 5, we conclude the discussion.

2. PA

In this section, we describe the design of the proposed PA, the simulated results, and the results of a comparison with a conventional PA.

2.1 Design of PA

Figure 1 shows the schematic of the proposed PA, which is based on a class-AB doubleended push-pull amplifier. The proposed PA consists of an input-matching circuit, two designed transformers, and an amplifier. The input-matching circuit is composed of a parallel capacitor and a series inductor, and the impedance of an input-matching circuit is tuned to 50 Ω for measurement. The amplifier circuit consists of two identical N-type MOSs (NMOSs) for the I/O transistor with a high voltage tolerance of around 5 V. We adopted a cascode configuration with a common-source NMOS and a common-gate NMOS to improve the gain of the PA. The DC supply of V_{bias} , V_g , and V_{dd} is set to 0.9, 1.8, and 4.5 V, respectively, and the total dissipation power of the PA is 93 mW.



Fig. 1. Schematic of (a) proposed and (b) conventional PAs.

The proposed PA includes two center-tapped transformers, InTrans and OutTrans. InTrans generates differential signals with the same amplitude from the single-ended signal of input, and OutTrans generates output single-ended signals for the antenna from amplified differential signals. We designed the transformer by using a three-dimensional (3D) electromagnetic analyzer to derive the S-parameter of the transformer. Figures 2(a) and 2(b) show the layout of the center-tapped transformer. The PA circuit is fabricated in a 0.18 mm CMOS process with 6-metal layers, and the center-tapped transformer consists of two inductors, a 2-port inductor with the 3rd and 4th metal layers, and a center-tapped 3-port inductor with the 5th metal layer and the 6th metal layer, which is the top metal layer. The drawing line for the bias of the 3-port inductor is laid out with metal layer 4.

Figure 3 shows simulated and measured S-parameter results and the phase gap of the proposed transformer under the condition that each port of the center-tapped transformer is terminated at 50 Ω . The measured *S*21 and *S*31 are respectively -6.7 and -7.4 dB at 5.2 GHz with a phase gap of 180° for the pass band.



Fig. 2. (Color online) (a) Two-dimensional (2D) and (b) 3D layouts of the center-tapped transformer for the proposed PA.



Fig. 3. (Color online) Measured S21 and S31 and phase gap of the center-tapped transformer.

2.2 Proposed PA without output-matching network

The output impedance of the PA is widely matched to 50 Ω using inductors and capacitors (LC impedance-matching network); however, the parasitic resistors in the LC impedance-matching network reduce the performance of the PA, i.e., the gain and PAE. The proposed PA is designed to achieve both high gain and high PAE with a matching network on the antenna even with an impedance of other than 50 Ω .

Figures 4(a) and 4(b) show the simulated output and input power of the proposed and conventional PAs. The input signal frequency is 5.2 GHz, and the power dissipation of both the proposed and conventional PA is 93 mW. The 1 dB compression point (P1dB), which is an index of linearity for an amplifier, of the proposed PA is 11.3 dBm and that of the conventional PA is 10.4 dBm. The linear output powers of the proposed and conventional PAs are 14.9 and 13.5 dB, respectively. The proposed PA achieves a 13.9 dB gain at P1dB, whereas the gain of the conventional PA is 12.5 dB.

Figures 5(a) and 5(b) show the results of the simulated load-pull analyses of the proposed and conventional PA with an LC impedance-matching output. The output impedance of the proposed PA is $70.5 + j55.0 \Omega$ and that of the conventional PA is matched to 50Ω . The red and



Fig. 4. (Color online) Simulated output and input powers of (a) proposed and (b) conventional PAs.



Fig. 5. (Color online) Results of simulated load-pull analyses of (a) proposed and (b) conventional PAs.

blue contours show the PAE and output power, respectively. The input signal frequency is 5.2 GHz, and the input power is -2.6 dBm. The output powers of the proposed and conventional PAs are 11.3 and 10.0 dBm, and the PAEs of the proposed and conventional PAs are 30.9 and 25.2%, respectively.

Figure 6 shows the simulated PAE and input power. The PAE of the proposed PA at P1dB is 15.7%, which is 3.3 points higher than the 12.4% of the conventional PA. Moreover, the proposed PA achieves a maximum PAE of 30.9%, which is 5.7 points higher than the 25.2% maximum PAE of the conventional PA.

2.3 Measured results of the proposed PA

Figure 7 shows a micrograph of the proposed PA, fabricated in 0.18 mm CMOS. We measured the S-parameter of the proposed PA with a vector network analyzer (VNA). Because the output impedance of the proposed PA is not tuned to 50 Ω , the output impedance should be calculated from the measured S-parameter with impedance conversion owing to the 50 Ω input impedance of the measurement instrument. Figures 8(a) and 8(b) show the measured



Fig. 6. (Color online) Simulated PAEs of the proposed and conventional PAs.



Fig. 7. (Color online) Micrograph of the proposed PA in 0.18 μ m CMOS.



Fig. 8. (Color online) Measured and simulated (a) S11 and (b) S21 of the proposed PA.

and simulated results of *S*11 (reflection power) and *S*21 (transmission power) of the proposed PA, respectively. The measured *S*11 and *S*21 are degraded compared with the simulated results owing to the parasitic elements of the fabricated circuit. However, the measured results indicate that the proposed PA works well.

The output impedance of the proposed PA is calculated as $70.5 + j55.0 \Omega$. Therefore, the output impedance of the complex conjugate of the PA that maximizes the efficiency of the transmitter is $70.5 - j55.0 \Omega$.

3. Antenna with Impedance Matching Block

Figure 9 shows the layout of the proposed antenna for the proposed PA. The proposed antenna is based on a slot antenna. The impedance-matching block consists of a CPW, quarterand half-wavelength transmission lines of meandering geometry, and impedance inverting circuits (J inverts).^(6–11) Figure 10 shows the simulated input impedance and gain characteristic of the proposed antenna. The simulated input impedance of the proposed antenna is calculated as $73.6 - j63.2 \Omega$ at 5.2 GHz, which is nearly equal to the target impedance of $70.5 - j55.0 \Omega$. In addition, the proposed antenna has a peak gain at around 5 GHz.



Fig. 9. (Color online) Layout of the proposed antenna with impedance-matching block.



Fig. 10. (a) Simulated impedance and (b) gain of the proposed antenna.

The simulated and measured S11 characteristics of the proposed antenna are shown in Fig. 11. The simulated and measured S-parameters are acquired when the port impedance is $70.5 - j55.0 \Omega$, not 50 Ω . The measured S11 does not completely correspond to the simulated results owing to parasitic elements of the connector for the measurement. However, the measured results show that the proposed antenna achieves S11 of -13.6 dB, which is a satisfactory performance for an antenna. The simulated and measured results closely match the simulated results, and the proposed antenna is a nondirectional antenna with the X–Z plane.

4. Integrated PA with Antenna

The fabricated integrated PA with the proposed antenna, which has an impedance-matching block, is shown in Fig. 13(a). The proposed PA is mounted on the proposed antenna and the routing wires of the signal and ground are Au. An enlargement of the area around the proposed PA is shown in Fig. 13(b).

The measured and simulated S21 values of the integrated PA are shown in Fig. 14. The simulated and measured results are acquired when the port impedance is $70.5 - j55.0 \Omega$, not 50 Ω . The input power is -2.6 dBm. In the measurement, the radiation power from the antenna is received by the horn antenna in an anechoic chamber, and the received power is measured with



Fig. 11. (Color online) Simulated and measured *S*11 values of the proposed antenna.

PA.



Fig. 12. (Color online) Simulated and measured X-Z plane radiation patterns.



(a) (b) Fig. 13. (Color online) (a) Micrograph of the integrated PA with the antenna and (b) enlargement of area around



Fig. 14. (Color online) Measured results of the integrated PA (green) and intrinsic PA (blue, measured; red, simulated).

VNA. The red and blue lines respectively show the simulated results and the measured results of the intrinsic PA, and the green dots show the measured *S*21 of the integrated PA, which is composed of the proposed PA and the proposed antenna. The measured *S*21 of the intrinsic PA is smaller than the simulated value owing to parasitic elements of the routing wire and probe contacts at the power supply and signal lines.

Because of the difficulty in bonding, the gap between the two ground wires are wide. The line length of both wires is 2 mm, which is 7% of the half-wavelength at 5 GHz (30 mm) and causes a slight impedance mismatch. Moreover, the PA chip is attached to the antenna substrate with an insulating adhesive. Therefore, a small impedance mismatch will be generated by the insulating layer on the signal line. Because the impedance mismatch is small, the measured *S*21 of the integrated PA is slightly smaller than that of the intrinsic PA, as shown in Fig. 14.

5. Conclusions

The integrated push-pull PA with the planar slot antenna was demonstrated. The conventional PA whose output impedance is 50 Ω is connected to an antenna with 50 Ω impedance. On the other hand, the proposed integrated PA with the antenna can choose the impedance other than 50 Ω so as to achieve higher PAE for a high-efficiency transmitter. The proposed antenna can tune the impedance, and the impedance tuning technique at the antenna enables to achieve higher PAE of the PA. The proposed PA achieved PAE at PldB of 15.7% and maximum PAE of 30.9%. A slot antenna with an impedance-matching network whose impedance is other than 50 Ω was developed. The proposed antenna enabled impedance matching with the output impedance of the PA while maintaining both high gain and high linearity of the PA. We fabricated the integrated PA with the proposed antenna. The measured and simulated results revealed that the integrated PA achieved the high gain and high efficiency for wireless transmitters. We will try to reduce the discrepancy in gains between the integrated PA with the antenna and the intrinsic PA, by optimizing the gap between the ground wires in the near future.

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About the Authors



Takeshi Kuboki received his B.E., M.E., and Ph.D. degrees in Communications and Computer Engineering from Kyoto University, Japan, in 2006, 2008, and 2015, respectively. From 2013 to 2015, he was engaged in the development of high-speed serial interfaces in Renesas Electronics Corp., Itami, Japan. Since 2015, he has been an assistant professor at Kyushu University. His research interests are in analog and high-speed circuits, wireline and wireless communication systems, and sensing technology with terahertz radiation. (kuboki@ed.kyushu-u.ac.jp)



Tomoki Sadakiyo received his B.E. and M.E. degrees from Kyushu University, Japan, in 2016 and 2018, respectively. His research interests are in wireless communication and the design of antennas.



Wee Sang Park received his B.S. degree in electronic engineering from Seoul National University, Korea, in 1974, and his M.S. and Ph.D. degrees in electrical engineering from the University of Wisconsin-Madison, USA, in 1982 and 1986, respectively. From 1986 to 1988, he taught at Wichita State University. He joined Pohang University of Science and Technology, Korea in 1988, and retired in 2017. He was the director of the Antenna Laboratory at POSTECH, and conducted research on passive microwave devices such as phased-array antennas, small antennas, propagation in metamaterials, frequency-selective surfaces, wireless power transfers, RFID radiators, and LSI radiations. Professor Park was the symposium general chair of the ISMOT2017 conference held in Seoul, and is a member of the IEEE MTT and AP societies.



Haruichi Kanaya received his B.S. degree from Yamaguchi University, Japan, in 1990 and his M.S. and Ph.D. degrees from Kyushu University, Japan, in 1992 and 1994, respectively. In 1994, he became a Research Fellow (PD) of the Japan Society for the Promotion of Science. In 1998, he was a visiting scholar at the Massachusetts Institute of Technology (MIT), USA. He is currently engaged in the study and design of RF CMOS LSI systems, energy harvesting devices, MEMS, and miniature, planar, flexible and array antennas. He is an associate professor at the Department of Electronics, Graduate School of Information Science and Electrical Engineering, as well as the System LSI Research Center, Kyushu University. Dr. Kanaya is a senior member of the Institute of Electronics, Information and Communication Engineers (IEICE) and Institute of Electrical and Electronics Engineers (IEEE). (kanaya@ed.kyushu-u.ac.jp)