Sensors and Materials, Vol. 31, No. 7 (2019) 2213–2223
MYU Tokyo

S & M 1925

Improved One-cycle Control for Realizing AC/DC Power Factor Correction Boost Converter

Ching-Lung Chu,* Ming-Tsung Tsai, and Jheng-Fong Shen

Southern Taiwan University of Science and Technology, No. 1, Nan-Tai Street, Yungkang Dist., Tainan 710, Taiwan

(Received November 16, 2018; accepted February 14, 2019)

Keywords: one-cycle control, boost converter, power factor correction

In this paper, an improved one-cycle control is proposed for an AC/DC boost converter with power factor correction (PFC) using logic and analogy circuits. The proposed improved one-cycle control method realizes features that are similar to those of the conventional one-cycle method without using a sense input voltage and a multiplier. It can also promote the stability of the converter. The adjustable maximum duty cycle limit of the converter is designed to limit the maximum duty cycle by adopting the logic and analogy circuits. According to the analysis of the modified one-cycle control method, the suitable circuit component parameters of the converter can be designed for the one-cycle control AC/DC PFC boost converter. Finally, a modified one-cycle control AC/DC PFC boost converter with input ACs of 90, 110, 220, and 260 V, an output DC of 400 V, and an output power of 500 W was built to verify the accuracy and feasibility of its performance.

1. Introduction

Power factor correction (PFC) techniques used to make the input AC current conform with the input AC voltage have been widely used in AC/DC converter industrial products, for which a boost converter is suitable owing to a continuous input current. Many reports have discussed the control of PFC AC/DC boost converters.[1–15]

A conventional control method uses voltage outer and current inner loops to trace the input voltage, input current, and output DC voltage with the average current control method.[1] However, the control by this method is complex and requires many detection components, which increases the circuit volume, cost, and complexity, and UC3854 is typically used as the control chip. Another control method is one-cycle control,[2–13] which does not need to detect the input voltage and does not use a multiplier, but it only uses a trigger signal control of an integrator and compares a sawtooth wave with the current detesting value. Finally, the control is relatively simple through the set-reset (SR) flip-flop control converter duty cycle and can significantly reduce the circuit size and cost.

Conventional one-cycle control methods can be broadly divided into the following two categories: the first category uses the output DC voltage error to obtain a continuous count-down sawtooth wave to be compared with the measured inductance current and to

*Corresponding author: e-mail: clchu@stust.edu.tw
https://doi.org/10.18494/SAM.2019.2197

ISSN 0914-4935

determine the duty cycle of the converter switch[2–5] with IR1155S typically used as the control chip. The second category uses the output DC voltage error to obtain a continuous count-up sawtooth wave to be compared with the measured inductance current and to determine the duty cycle of the converter switch.[6,7] These two categories of one-cycle control methods enable PFC. In addition, there are other reports that show more complex one-cycle control methods.[8,9]

However, the one-cycle control of the output current waveform is often skewed or deformed;[5,10] this problem can be solved using an output voltage feedback filter.[7] When the input AC voltage is large or the load is light, the input AC operates discontinuously especially as the input AC voltage is close to a zero-cross point; thus, the input current operates continuously and discontinuously in half a cycle, resulting in a poor harmonic distortion.[6,7,12,13] This problem of poor total harmonic distortion can be solved by increasing the filter inductance when the input AC is small; therefore, two filter inductances of different sizes are adopted to compare the input AC waveform and total harmonic distortion in this study.

A one-cycle control circuit uses an SR flip-flop to drive the power switch of an AC/DC converter. However, the SR flip-flop through an S or R pin at the edge of the trigger obtains a different output signal. Thus, the SR flip-flop should be prevented because it triggers the problem in some cases and results in an output signal error that causes the converter to lose control. Therefore, a simple logic circuit is added to prevent the SR flip-flop from triggering such an error and limit the maximum power switch duty cycle to enhance the overall circuit stability in the boost converter. In this paper, by theoretical analysis, we design the parameters of the control circuit components to be suitable for this one-cycle control. The feasibility of the control is verified using two filter inductances of different sizes.

2. Circuit Analysis of One-cycle Control

In this section, a conventional one-cycle control electric circuit and its shortcomings are analyzed and discussed. The shortcomings are overcome by adding a simple logic circuit.

2.1 Conventional one-cycle control electric circuit

The conventional implementation of one-cycle control AC/DC boost converters, as shown in Fig. 1,[7] through an integrator with a reset trigger signal generated a variable output voltage V_m as the peak value of $V_2(t)$, which is a continuous count-down sawtooth wave, and compared it with the detected inductance current $V_1(t)$. When the clock (CLK) signal is triggered, the power switch turns on, the inductance current $V_1(t)$ increases linearly, and $V_2(t)$ starts to decrease linearly from the peak value of V_m. When $V_1(t) > V_2(t)$, the power switch turns off, the signal $V_1(t)$ starts to decrease linearly, $V_2(t)$ is triggered by the reset signal and rapidly returns to the peak value of V_m, and the next CLK signal is expected to be triggered.

This conventional single-cycle control has some limitations. When CLK is triggered, $V_2(t)$ starts to decrease linearly from V_m, and if the next CLK is triggered, the extension line of $V_2(t)$ cannot fall to zero, as shown in Fig. 2; when $V_2(t)$ is at $t = t_2$, t_4, and t_5, $V_2(t)$ is still positive, and when the inductance current approaches zero, the V_R signal gradually approaches the CLK

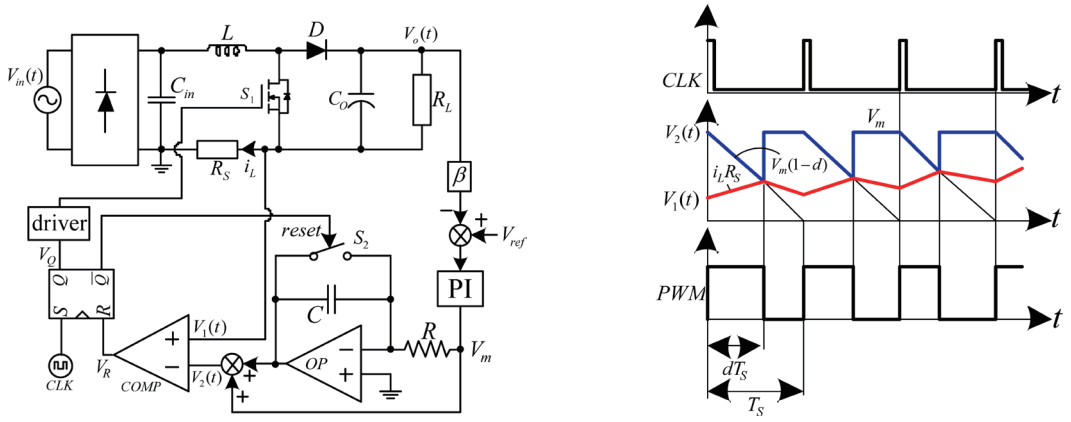

Fig. 1. (Color online) Traditional one-cycle control applied in AC/DC PFC boost converter.[7] (a) Circuit scheme. (b) Operated sequence waveforms.

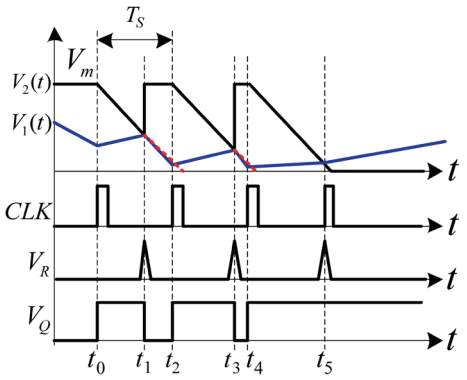

Fig. 2. (Color online) Traditional one-cycle control applied in AC/DC PFC boost converter with error triggered.

signal. At $t = t_5$, the V_R and CLK signals will overlap at $t = t_5$. At this time, the S and R pins of the SR flip-flop will be triggered at the same time, V_Q will continue to maintain the high voltage of the upper state, so that the power switch of the converter will always be turned on, and the sawtooth wave $V_2(t)$ will no longer reset and will always be zero. This will cause the inductance current to continue to increase and finally the converter will lose control. If the extension line $V_2(t)$ reaches zero early, the maximum duty cycle of the converter will become smaller. The converter will no longer deliver enough energy to the heavy load. Therefore, the ideal way is that when $V_2(t)$ ends at the end of a CLK cycle, V_m must be dropped to zero immediately; however, owing to the nonideal characteristics of the components, it is difficult to achieve precise control through V_m.

2.2 Improved one-cycle control circuit

To overcome the shortcomings of conventional one-cycle control, an improved one-cycle control electric circuit is proposed as shown in Fig. 3. Here, our main aim is to improve the following three points:

a. As shown in Fig. 2, beyond $t = t_5$, the logical comparison is wrong owing to the SR. $V_1(t)$ and $V_2(t)$ will never have a crossover point. Therefore, the trigger signal of the continuous count-down sawtooth wave $V_2(t)$ will be changed by CLK_1 to ensure that the integrator can be reset at the beginning of every CLK_1 cycle as shown in Fig. 3; thus, $V_2(t)$ can be regressed to the maximum V_m value.
b. To prevent the inductance current being close to zero, even if $V_2(t)$ in a CLK time period cannot be reduced to zero as shown in Fig. 2, a logic circuit is added between the output of the comparator and the CLK_1 signal as shown in Fig. 3. Moreover, the S and R pins of SR flip-flop signals will not be triggered simultaneously, eliminating SR flip-flop output errors.
c. Since the conventional one-cycle control has no maximum duty cycle limit, the power switch of the converter remains turned on, which will cause the converter to lose control. Therefore, a logic circuit is added between the output of the comparator and the CLK_1 signal as shown in Figs. 3 and 4; the signal CLK_2 is generated by CLK_1 through a limiter, which can generate a maximum adjustable duty cycle limit in the range of $(D_1–1)T_S$.

The improved one-cycle control circuit and sequence proposed in this paper are shown in Figs. 3 and 4, respectively. The continuous countdown sawtooth wave of the variable peak V_m can be provided by a stable CLK_1 signal and the maximum duty cycle limit is determined by the CLK_2 signal. When the current is zero and even if $V_2(t)$ cannot be decreased to zero during the maximum duty cycle, the converter can still be limited to the set maximum duty cycle.

3. Discussion and Design of the Improved One-cycle Control Circuit

In this section, the proposed improved one-cycle control circuit is discussed and the relationship between waveforms in Figs. 3 and 4 is analyzed. The design of the control

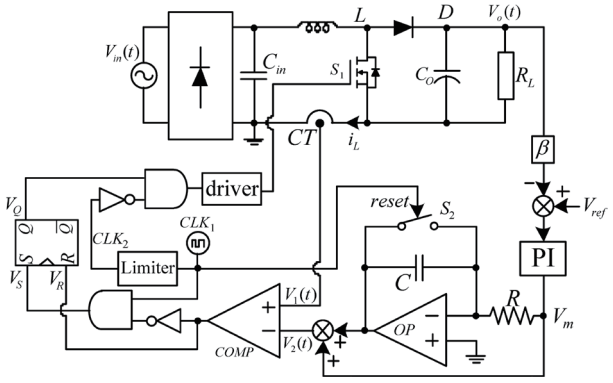

Fig. 3. Improved one-cycle control circuit applied in AC/DC PFC boost converter.

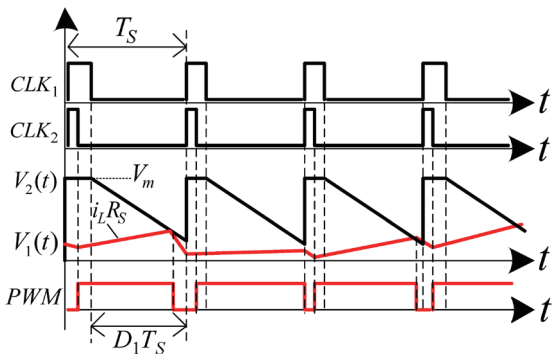

Fig. 4. (Color online) Operated sequence waveforms of the improved one-cycle control.

circuit element parameters is obtained by using the derived formula. Before the analysis, $V_1(t) = i_L(t) \cdot CT$ is defined first in Figs. 3 and 4, where CT is the current conversion voltage ratio and V/A is the conversion unit.

3.1 Analysis of the relationship among maximum duty cycle, $V_1(t)$, and $V_2(t)$

According to Fig. 4, during the maximum duty cycle, if $V_2(t)$ has not yet decreased from V_m to zero and when the inductance current is close to zero at $V_1(t) \cong 0$, $V_1(t)$ will not be greater than $V_2(t)$ and then the converter will remain at the maximum duty cycle limit. If $V_2(t)$ has decreased from V_m to zero during the maximum duty cycle, the maximum duty cycle of the converter can be reduced; however, the converter will no longer provide enough energy for the heavy load. Therefore, a more suitable control method is that, in the maximum working period, $V_2(t)$ should just decrease from V_m to zero, and even if $V_1(t)$ is zero, $V_1(t)$ can still be compared with $V_2(t)$. As shown in Figs. 3 and 4, where $V_2(t)$ must be reduced from V_m to zero during the working period of $D_1 \cdot T_S$, Eq. (1) is obtained as

$$0 = V_m - \frac{1}{RC} V_m (D_1 \cdot T_S), \tag{1}$$

and the integrator parameter can be determined from Eq. (1) as

$$R \cdot C = D_1 \cdot T_S. \tag{2}$$

3.2 Analysis of the slope relationship between $V_1(t)$ and $V_2(t)$

As shown in Fig. 5, the timing of $V_2(t)$ and the inductance current detection value $V_1(t)$, where the slope of $V_2(t)$ goes from point A to zero voltage, can be expressed as

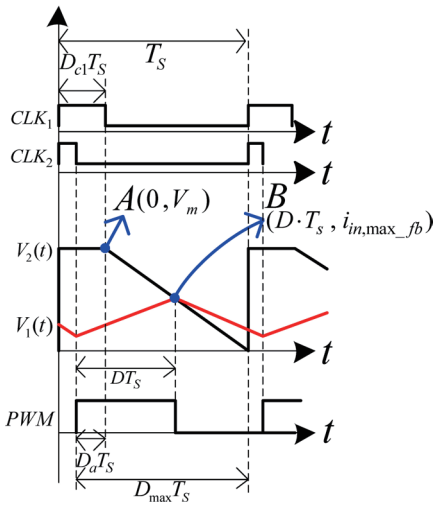

Fig. 5. (Color online) Relationship between $V_1(t)$ and $V_2(t)$ in the improved one-cycle control.

$$M = \frac{-V_m}{T_s - D_{c1}T_s} \ . \tag{3}$$

The curve of $V_2(t)$ from V_m to zero is written as the linear equation

$$V_2(t) - V_m = M \cdot t. \tag{4}$$

When the input voltage is $v_{in,peak,min}$, the duty cycle of the boost converter can be expressed as

$$D = \frac{V_o - v_{in,peak,min}}{V_o}. \tag{5}$$

The maximum peak value of the inductance current of the boost converter can be expressed as

$$i_{L,peak} = \frac{\sqrt{2} \cdot P_{rate}}{v_{in,rms,min}} + \frac{v_{in,peak,min}}{2L} D \cdot T_s. \tag{6}$$

Finally, the peak value of the maximum inductance current through the current sensor can be expressed as

$$i_{L,peak\_fb} = \left(\frac{\sqrt{2} \cdot P_{rate}}{v_{in,rms,min}} + \frac{v_{in,peak,min}}{2L} D \cdot T_s \right) \cdot CT_{max}. \tag{7}$$

From Fig. 5, it can be seen that time is very short and can be ignored; thus, $D{\cdot}T_s - D_a{\cdot}T_s \cong D{\cdot}T_s$. By substituting $D{\cdot}T_s$ in the coordinate of point B in Fig. 5 and Eq. (7) into Eq. (4), followed by Eq. (3) into Eq. (4), we obtain

$$\left(\frac{\sqrt{2} \cdot P_{rate}}{v_{in,rms,min}} + \frac{v_{in,peak,min}}{2L} DT_s \right) \cdot CT_{max} = \frac{-V_m}{T_s - D_{c1}T_s} \cdot D \cdot T_s + V_m \ . \tag{8}$$

Finally, the ratio CT_{max} of the maximum current limit can be expressed as

$$CT_{max} = \frac{2L \cdot v_{in,rms,min} \cdot V_m}{2\sqrt{2} \cdot L \cdot P_{rate} + v_{in,rms,min} \cdot v_{in,peak,min} \cdot D \cdot T_s} \left(1 - \frac{D}{1 - D_{c1}} \right). \tag{9}$$

4. Experimental Results

In this study, we implement a set of P_o = 500 W, v_{in} = 85–264 V_{rms}, V_o = 400 V_{dc}, f_s = 80 kHz, and AC/DC boost converters, which use the improved one-cycle control to achieve PFC. The filter inductance is 1 mH, and the output filter capacitance is C_o = 820 pF. When the input voltage v_{in} = 220 and 260 V_{rms}, the input current difference is compared with the filter inductances of 1 and 5 mH.

First, D_{c1} = 0.1 and $0 < D_a \leq 0.1$ are set, so that the maximum working period of the converter can be adjusted to $0 < D < 1$, then the integrator capacitance C is designed to be 0.0047 μF, and the integrator resistance R is calculated using Eq. (2), because the power supply of the operational amplifier (OP) uses ±12 V. The actual output is about V_m = 10 V. When the input voltage is $v_{in,peak,min}$, the duty cycle is calculated as D = 0.68 using Eq. (5). The slope $M = \frac{-V_m}{T_s - D_{c1}T_s} = -888.9k$ is calculated using Eq. (3), and the peak inductance current of $i_{L,peak}$ = 8.4 A is calculated using Eq. (6). Finally, CT_{max} = 0.2886 is calculated using Eq. (9). In this paper, CT = 0.2 is selected.

Figure 6 shows the inductance current feedback $i_{L\_fb} > 0$ waveform of the improved one-cycle control. Figure 7 shows the inductance current feedback $i_{L\_fb} \cong 0$ waveform of the improved one-cycle control. The V_{gs} signal can still be maintained at the maximum duty cycle, and V_m and i_{L_fb} still have intersections. Figures 8–19 respectively show that the waveforms of the input AC voltages are 90, 110, 220, and 260 V_{rms}, when the inductance L is 1 mH. Figures 20–23 respectively show that the waveforms of the input AC voltages are 220 and 260 V_{rms}, when the inductance L is 5 mH.

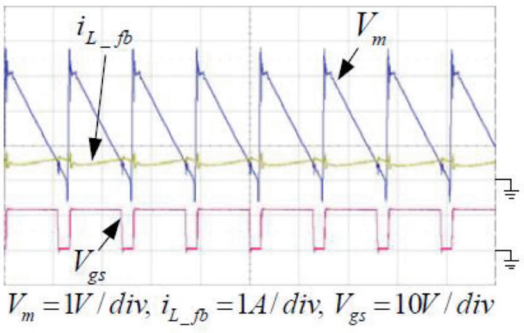

Fig. 6. (Color online) Waveforms of V_m, i_{L_fb}, and V_{gs} with $i_{L\_fb} > 0$.

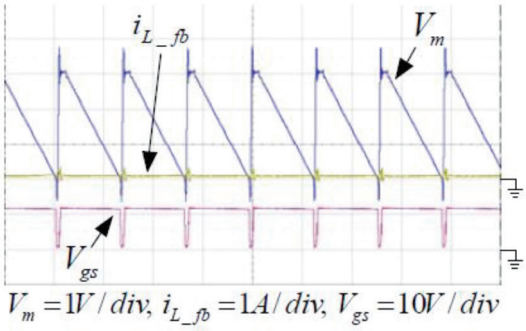

Fig. 7. (Color online) Waveforms of V_m, i_{L_fb}, and V_{gs} with $i_{L\_fb} \cong 0$.

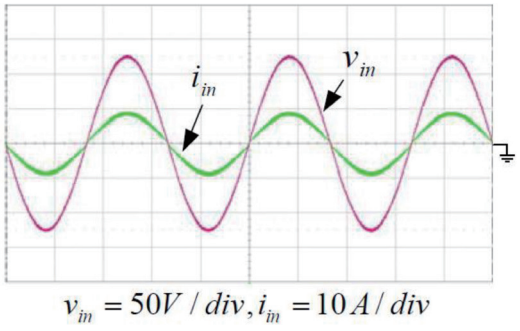

Fig. 8. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 90 V_{rms} and P_o = 500 W.

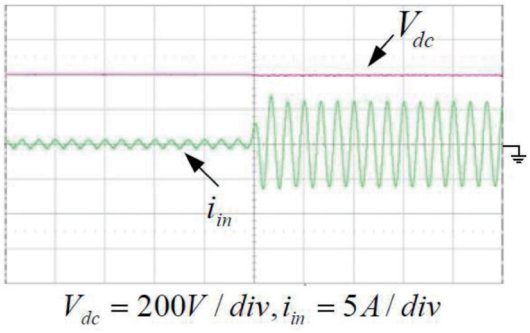

Fig. 9. (Color online) Waveforms of V_{dc} and i_{in} with v_{in} = 90 V_{rms} and P_o from 100 to 500 W.

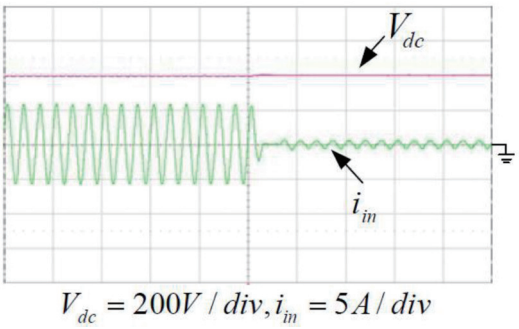

Fig. 10. (Color online) Waveforms of V_{dc} and i_{in} with v_{in} = 90 V_{rms} and P_o from 500 to 100 W.

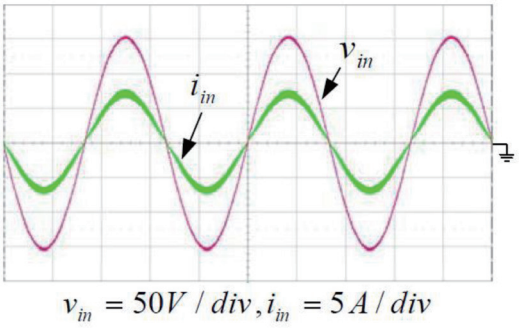

Fig. 11. (Color online) Waveforms of v_{in} and i_{in} with v_{in} =110 V_{rms} and P_o = 500 W.

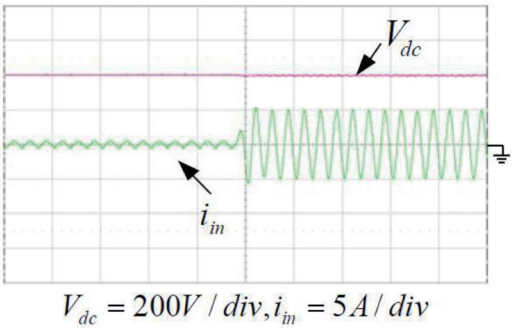

Fig. 12. (Color online) Waveforms of V_{dc} and i_{in} with v_{in} = 110 V_{rms} and P_o from 100 to 500 W.

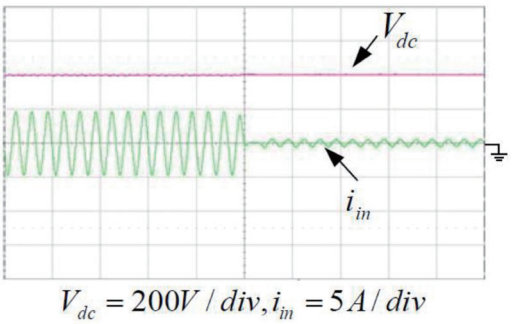

Fig. 13. (Color online) Waveforms of V_{dc} and i_{in} with v_{in} = 110 V_{rms} and P_o from 500 to 100 W.

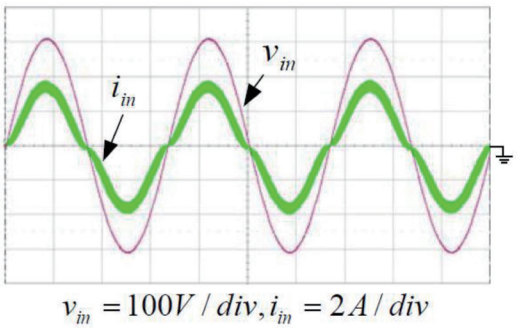

Fig. 14. (Color online) Waveforms of V_{dc} and i_{in} with v_{in} = 220 V_{rms} and P_o = 500 W.

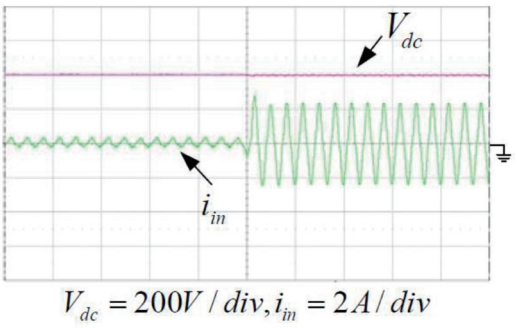

Fig. 15. (Color online) Waveforms of V_{dc} and i_{in} with v_{in} = 220 V_{rms} and P_o from 100 to 500 W.

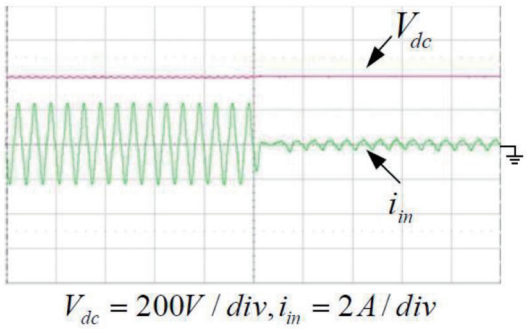

Fig. 16. (Color online) Waveforms of V_{dc} and i_{in} with v_{in} = 220 V_{rms} and P_o from 500 to 100 W.

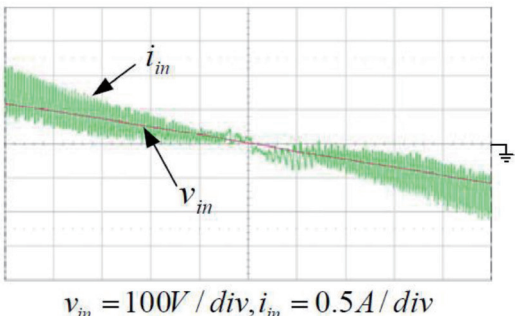

Fig. 17. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 220 V_{rms}, P_o = 500 W, and L = 1 mH.

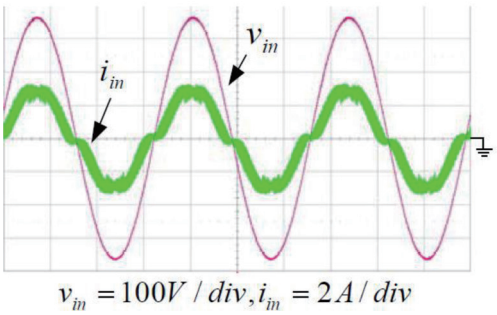

Fig. 18. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 260 V_{rms}, P_o = 500 W, and L = 1 mH.

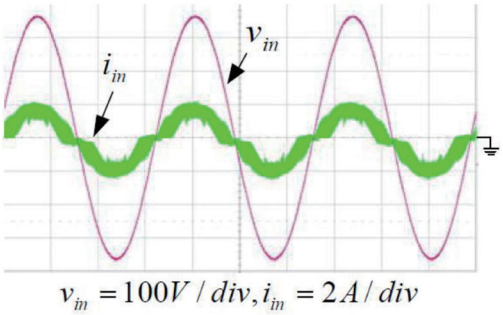

Fig. 19. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 260 V_{rms}, P_o = 300 W, and L = 1 mH.

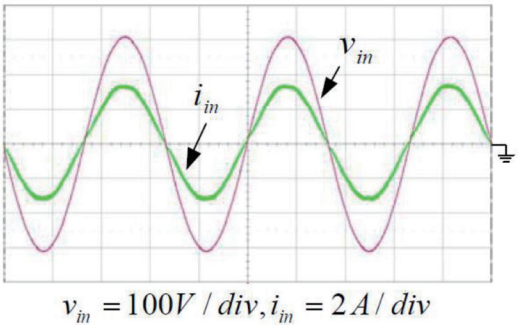

Fig. 20. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 220 V_{rms}, P_o = 500 W, and L = 5 mH.

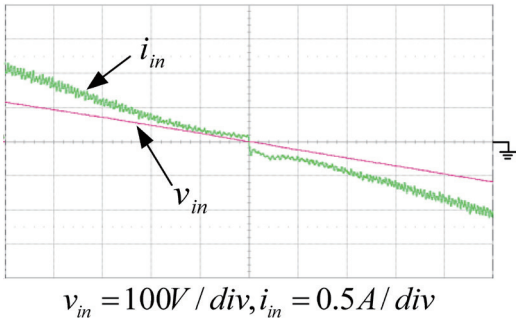

Fig. 21. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 220 V_{rms}, P_o = 500 W, and L = 5 mH.

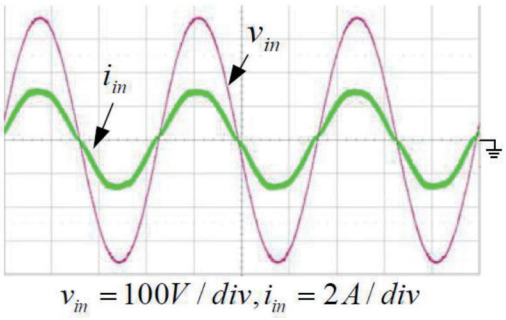

Fig. 22. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 260 V_{rms}, P_o = 500 W, and L = 5 mH.

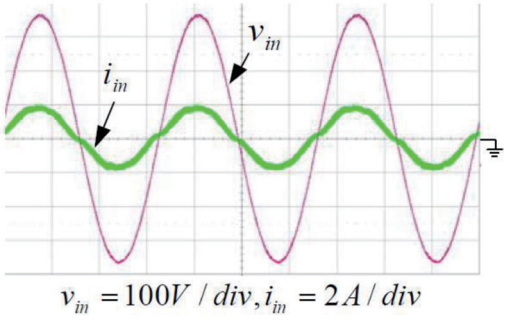

Fig. 23. (Color online) Waveforms of v_{in} and i_{in} with v_{in} = 260 V_{rms}, P_o = 300 W, and L = 5 mH.

As v_{in} = 220 V_{rms} and L = 1 mH, it can be seen from Fig. 14 that when the input voltage is higher, the input current is smaller. If the inductance is smaller, the inductance current ripple is larger, reducing the input current to zero, and the waveform has a larger ripple. When the inductance is increased to 5 mH, as shown in Fig. 20, because the inductance current ripple is smaller, the waveform has a smaller ripple as the input current is zero. Figures 17 and 21 show a comparison of input currents close to zero. Figure 24 shows the efficiency curves of the AC/DC PFC converter under various input voltages; the efficiency can reach more than 80% from 200

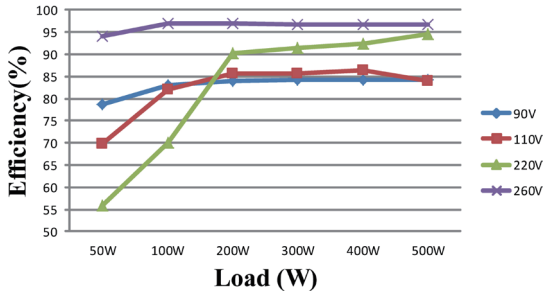

Fig. 24. (Color online) Efficiency measured under various input voltages.

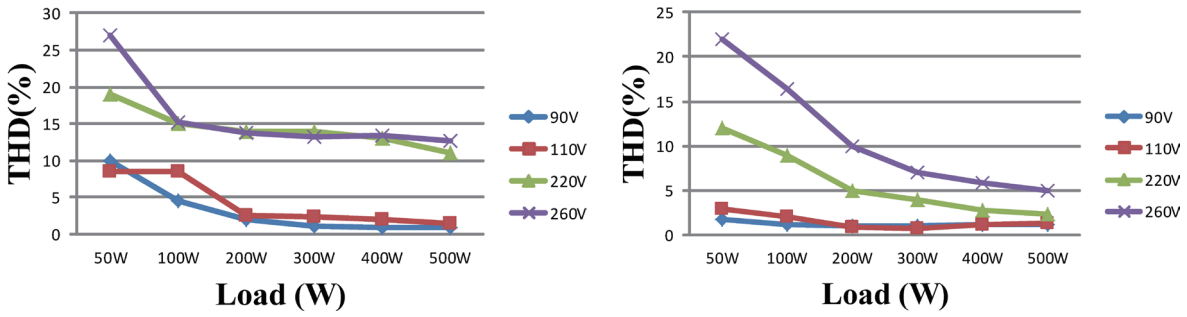

Fig. 25. (Color online) Total current harmonic distortion under various input voltages. (a) L = 1 mH and (b) L = 5 mH.

to 500 W. Figure 25 shows the total current harmonic distortion for L = 1 and 5 mH; the total current harmonic distortion for v_{in} = 220 V_{rms} and L = 5 mH is much lower than that for v_{in} = 220 V_{rms} and L = 1 mH.

5. Conclusions

In this study, an improved one-cycle control technique is applied in an AC/DC PFC boost converter. The proposed improved one-cycle control method realizes features that are similar to those of the conventional one-cycle method without using a sense input voltage and a multiplier. It can also promote the stability of the converter. The adjustable maximum duty cycle limit of the converter is designed to limit the maximum duty cycle by adopting logic and analogy circuits. By analyzing the modified one-cycle control method, we can design the suitable circuit component parameters of the converter for one-cycle control AC/DC PFC boost converters. Finally, a modified one-cycle control AC/DC PFC boost converter with input ACs of 90, 110, and 220 V, an output DC of 400 V, an output power of 500 W, v_{in} = 220 V, and filter inductance analyzed by the comparison between 1 and 5 mH was implemented to verify the accuracy and feasibility of its performance.

Acknowledgments

The authors thank the Ministry of Science and Technology, Taiwan, R.O.C. for the financial support through Grant MOST 106-2221-E-218-024-MY3.

References

1 E. Figueres, J. M. Benavent, and G. Garcera: IEEE Trans. Ind. Electron. **54** (2007) 1272.
2 A. Lollio: Transportation Electrification Conf. Expo (2014) 1.
3 T. K. Jappe and S. A. Mussa: IEEE Int. Telecommunications Energy Conf. (2011) 1.
4 T. K. Jappe and S. A. Mussa: IEEE Int. Symp. Industrial Electronics (2011) 1555.
5 R. Brown and M. SoIdano: IEEE Applied Power Electronics Conf. Exposition **2** (2005) 825.
6 Y. Wang and J. Li: 32nd Annu. Conf. IEEE Industrial Electronics (2006) 1763.
7 H. Chao, L. Wei-ming, and G. Xiao-jun: IEEE Power Electronics and Motion Control Conf. **3** (2012) 1621.
8 A. A. M. Bento and E. R. C. da Silva: IEEE Industry Applications Conf. (2007) 2333.
9 Y. Li, Y. Yang, Z. Zhu, and W. Qiang: IEEE Int. Conf. Asic (2011) 661.
10 R. Etz, T. Patarau, and D. Petreus: IEEE Design and Technology in Electronic Packaging (2012) 211.
11 E. Santi and S. Cuk: IEEE Telecommunications Energy Conf. (1992) 131.
12 Z. Lai and K. M. Smedley: IEEE Applied Power Electronics Conf. Exposition **1** (1997) 66.
13 K. C. Chang, K. H. Chen, T. J. Liang, and B. D. Liu: IEEE Int. Symp. Circuits and Systems (2009) 3078.
14 N. Vamannan and V. Hohn: IEEE Trans. Ind. Appl. **52** (2016) 3267.
15 H. Cheng, Y. Ma, and C. Wang: IEEE Int. Power Electronics and Application Conf. Exposition (2018) 1.