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Impact of Active Surface Area on Performance and Reliability of Tri-gate FinFET

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In this work, a contact etch stop layer (CESL) was found to cause tensile stress above the gate of FinFET devices, and the top tensile stress introduced compressive stress in the channel. With increasing active surface area (SA), a higher compressive stress was observed. The effect of compressive stress became more evident, resulting in a lower current but a higher reliability for nFinFET devices.

1. Introduction

FinFETs are considered a promising candidate for device scaling that surpasses the framework of traditional planar transistors and has a better gate controlling capability, repressing short-channel effects (SCEs) and hot carrier effects (HCEs), and improving the subthreshold swing (SS).[(1–5)] Even though fin-based structures may be superior electrically, they are less robust than planar structures mechanically, which may give rise to some unexpected failure mechanisms.[(6)] Prior studies indicate that mechanical stress shows a great impact on the electrical behavior. In traditional planar MOSFETs, thermal annealing is considered to expand the filler in shallow trenches and squeeze it; thus, the channel region is subjected to a compressive stress.[(7)] A typical fin bending may lead to electrical or physical failure. Its leaning angle forms an asymmetric depletion area and makes the leakage current larger than expected.[(8)] On the other hand, tensile and compressive stresses, which are two components of mechanical stress, will respectively improve electron and hole mobilities.[(9,10)] Stresses are intentionally introduced into the device channel by means of a silicon-carbon (SiC) source and drain (S/D), a strained cap layer, shallow trench insulation (STI), and so forth during the transistor fabrication process. In addition, lattice-mismatched SiC regions also induce stress in the Si channel along the width (transverse) and vertical directions.[(11)] In fact, with the

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continuous shrinking of the feature size, the STI stress effect becomes significant.[12] However, this behavior is much different from those of FinFETs and MOSFETs. In this work, the electrical and reliability analyses of tri-gate FinFETs affected by different active surface areas (SAs) were studied.

2. Experimental Methods

Figure 1 shows a TEM image of the tri-gate FinFET used in this study. The channel length, fin width, and fin height of the device were 16, 10, and 42 nm, respectively. The surface orientation of the fin sidewall is (110), while the channel direction is <110>. After FinFET device fabrication, SiN was covered as a contact etch stop layer (CESL). The CESL obtained by thermal CVD has tensile stress due to the manufacturing process. SA was defined as the distance from the gate to the edge of shallow trench isolation (STI), as shown in Fig. 2, and different SAs of 0.098, 0.386, and 3.842 μm were utilized.

In this work, the electrical properties of FinFET devices were measured using a semiconductor parameter analyzer (Agilent-B1500A) at room temperature. During hot carrier injection (HCI) stress measurement, the drain and gate voltages were set as $V_D = V_G = 1.6$ V with the grounded source and body. *I*–*V* curves were measured at certain stress time intervals.

3. Results and Discussion

Figure 3 shows I_D–V_G curves with different SAs. The extracted values of V_{TH} and SS are respectively shown in Figs. 4(a) and 4(b). It was observed that V_{TH} increases with SA, while SS is similar to the variation in SA. However, a reduction in drain current was observed with increasing SA. All samples are fabricated under the same conditions except for SA. As a result, the increase in V_{TH} and the reduction in I_D might be due to the influence of SA. On the other hand, similar SS values also indicate that different SAs did not affect the interface quality of devices.

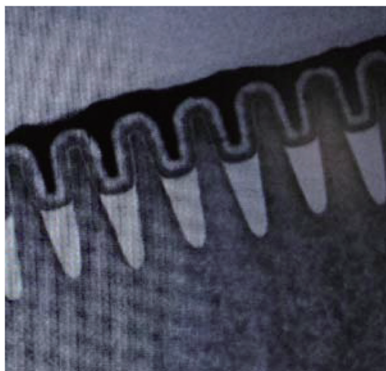

Fig. 1. (Color online) TEM image of the tri-gate FinFET.

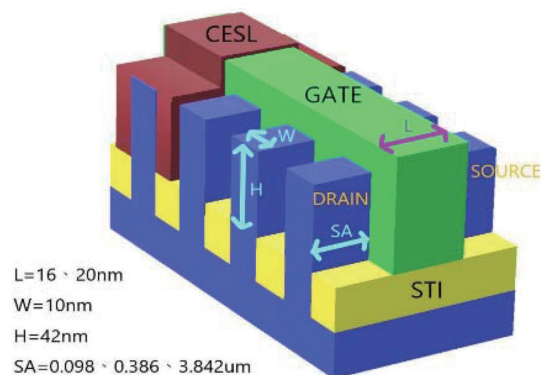

Fig. 2. (Color online) Structure and definition of SAs specifications for FinFET.

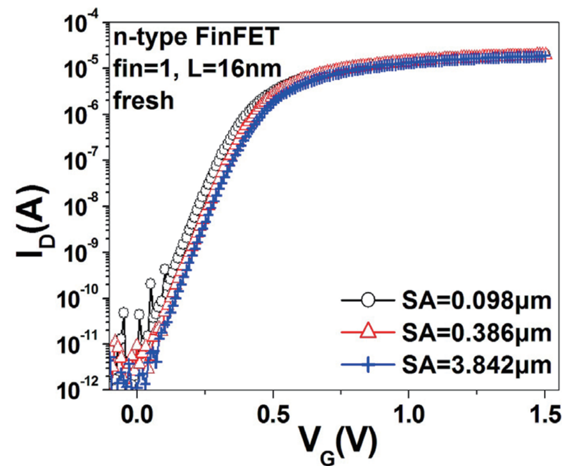

Fig. 3. (Color online) I_D–V_G curves of different SA specifications.

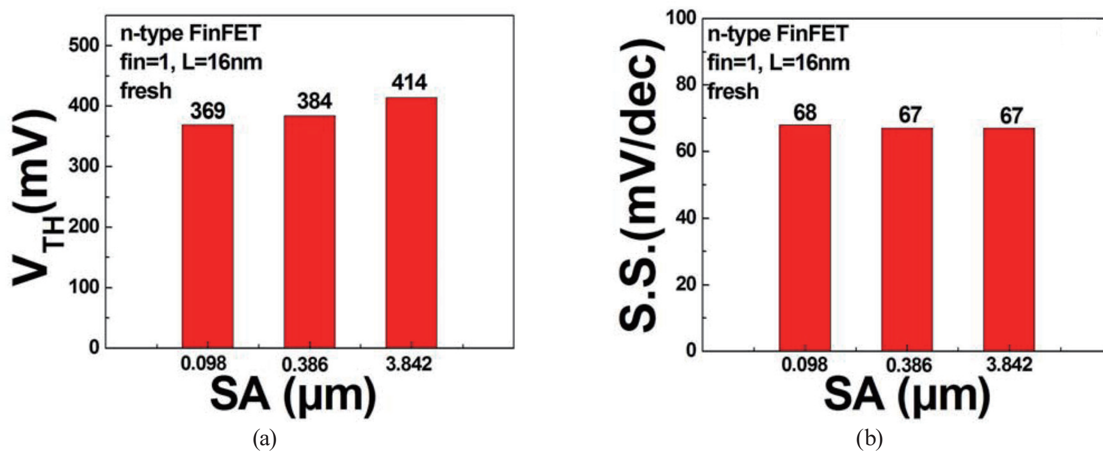

Fig. 4. (Color online) Extracted values of (a) V_{TH} and (b) SS with different SA specifications.

HCI was then utilized to investigate the reliability of FinFET devices with different SAs. The I_D–V_G curves obtained before and after 6000s HCI are plotted in Fig. 5. The positive V_{TH} shift during HCI stress indicates that the injected electrons were trapped in the gate dielectric layer. On the other hand, SS degradation reveals that impact ionization, which induces the generation of the interface state, occurs in FinFET devices during HCI stress.(2) It was observed that the FinFET device with a smaller SA shows a more severe degradation of V_{TH} and the subthreshold slope. The V_{TH} shift and SS variation versus stress time were extracted and are shown in Figs. 6(a) and 6(b), respectively. A V_{TH} shift of 441 mV was found in the device with SA = 0.098 μm, while a V_{TH} shift of 327 mV was observed in the device with SA = 3.842 μm. On the other hand, the increase in SS variation was determined to be 69 mV for the device with SA = 0.098 μm and 42 mV for the device with SA = 3.842 μm. It was observed that the FinFET device with a larger SA shows a higher reliability.

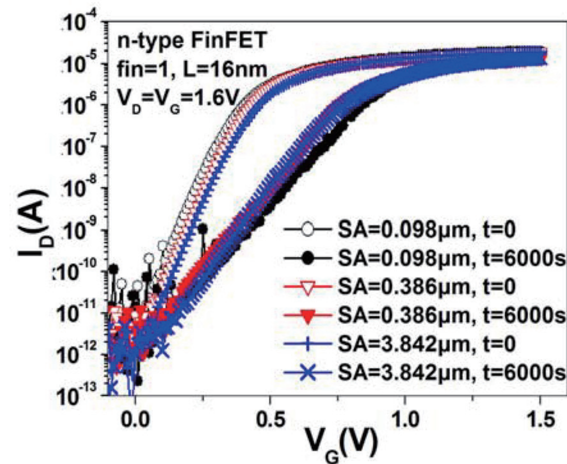

Fig. 5. (Color online) I_D–V_G curves with different SAs after HCI stress for 6000 s.

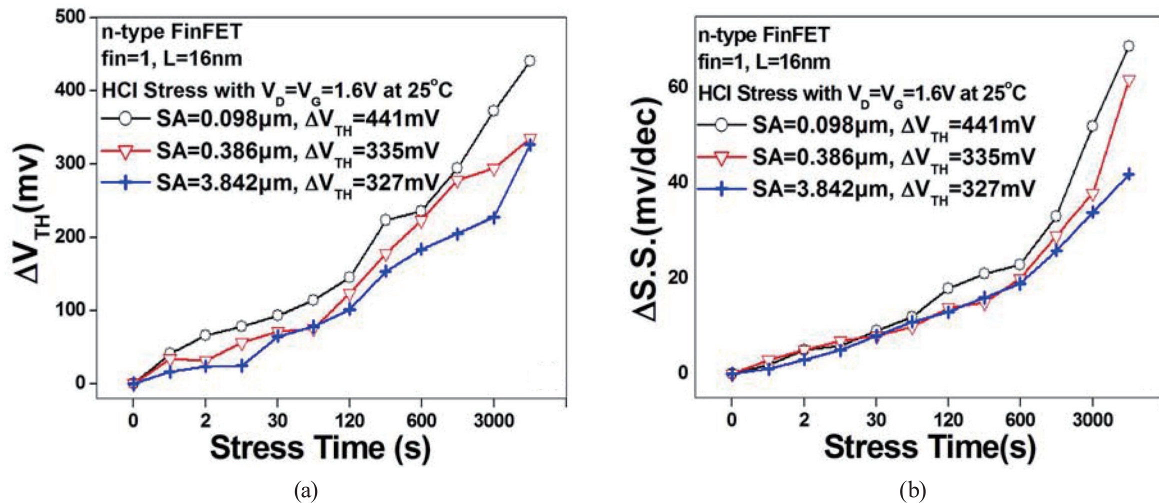

Fig. 6. (Color online) Extracted values of (a) V_{TH} shift and (b) subthreshold slope variation versus stress time with different SA specifications.

To examine the effect of different SA specifications, the schematic diagram of SA-induced channel stress components is shown in Fig. 7. The FinFET device used in this work was covered with SiN deposited in a furnace, thus resulting in tensile stress above the gate, which is expressed as T in Fig. 7. The tensile stress above the gate and S/D is expected to introduce a compressive stress to the channel, which is expressed as C in the diagram. As a result, a compressive stress to the channel is expected as the influence of SA. With increasing SA, the larger area covered by the CESL is expected to cause a higher tensile stress above the gate. The larger bending above the gate would lead to a higher compressive stress to the channel.

The reliability improvement of FinFET devices with the increase in SA can be explained as follows. With the increase in SA, the higher compressive stress reduces the electron mobility in the channel of nFinFETs. The reduced electron channel mobility results in a weaker

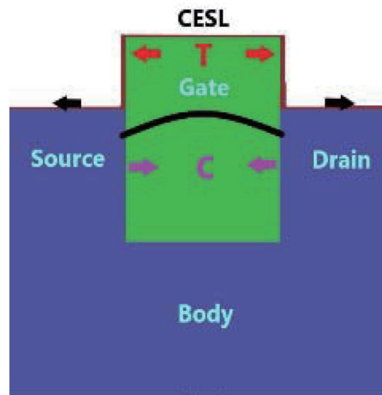

Fig. 7. (Color online) SA-induced channel stress and bending mechanism for FinFET devices.

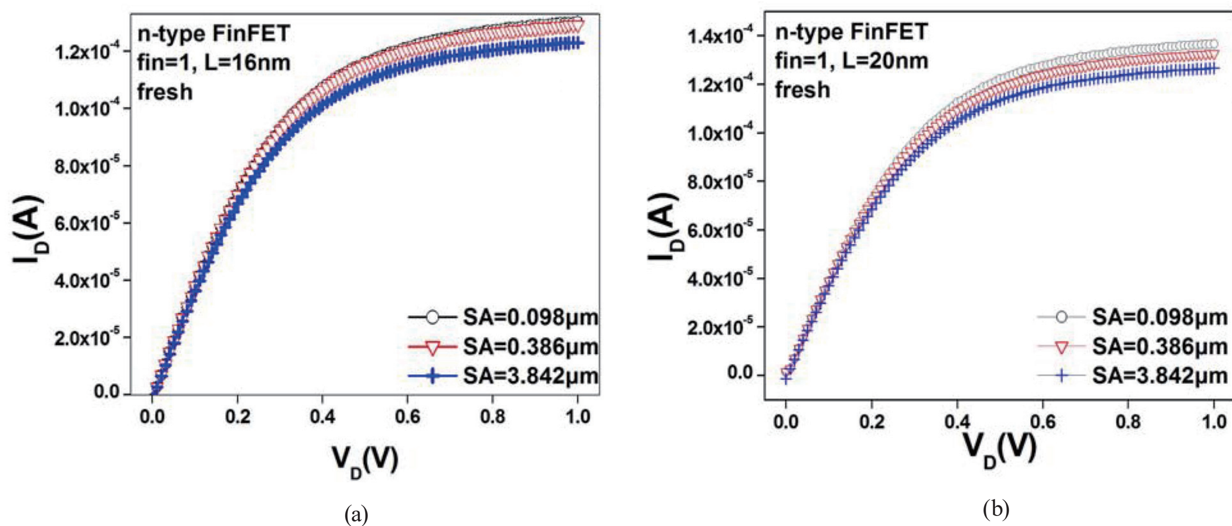

Fig. 8. (Color online) I_D–V_D curves of FinFETs with different SAs at (a) L = 16 and (b) 20 nm.

ionization impact during HCI stress, which inhibits the generation of the interface state and thus suppresses subthreshold slope degradation. On the other hand, fewer electrons are injected and trapped into the gate dielectric layer owing to the slower channel electrons, decreasing the positive shift of V_{TH} under HCI stress.

To verify the effect of compressive stress under different SA specifications, FinFET devices with different channel lengths were studied in this work, and the I_D–V_D curves obtained at L = 16 and 20 nm are respectively shown in Figs. 8(a) and 8(b). A reduced drain current was observed in the device with SA = 3.842 μm as compared with that obtained with SA = 0.098 μm, and the degradation rates were determined to be 5.0 and 7.8% for FinFET devices with L = 16 and 20 nm, respectively. These results could be explained by SA-induced compressive stress. For the longer channel device, the tensile stress provided by the CESL is enhanced by the larger area above the channel. The larger tensile stress above the gate introduces a higher compressive stress in the channel. A more severe drain current degradation is expected in the longer channel

device owing to the higher compressive stress, and the higher compressive stress reduces the electron mobility more effectively. As a result, a more severe I_D degradation for the longer channel with increasing SA could be explained.

4. Conclusions

N-type FinFET devices with different SAs were studied in this work. Compressive stress was found in the channel after CESL deposition. A large SA is considered to introduce a high compressive stress to the channel, thus reducing the channel electron mobility. As a result, a reduced device performance but an improved reliability is expected for FinFET devices with larger SAs.

Acknowledgments

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