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Analysis of Off-state Leakage Currents in Poly-Si FinTFTs with Wide Drain by Microwave Annealing

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In this study, polycrystalline silicon fin-like thin-film transistors (poly-Si FinTFTs) with a wide drain structure are fabricated. The off leakage current of poly-Si FinTFTs with various extended wide drain lengths (L_{EX}) is investigated. As L_{EX} increases, the longitudinal electric field at the intrinsic drift/N+ drain junction decreases and improves the off leakage current derived from longitudinal band-to-band tunneling (L-BTBT). The off leakage current of poly-Si FinTFTs at different temperatures is also analyzed to investigate the leakage mechanisms. For poly-Si FinTFTs with a small L_{EX} (= 0 and 0.8 mm), the weak dependence of leakage current on temperature indicates that the band-to-band tunneling (BTBT) is dominant. For poly-Si FinTFTs with a large L_{EX} of 1.6 mm, the strong dependence of leakage current on temperature and the weak dependence of leakage current on drain voltage indicate that trap-assisted tunneling (TAT) is the dominant leakage mechanism. These results indicate that it is gate-induced drain leakage (GIDL), resulting from L-BTBT, that is effectively suppressed by increasing L_{EX}.

1. Introduction

Gate-induced drain leakage (GIDL) is the major component of the off-state leakage current in fin-like field-effect transistors (FinFETs) and increases standby power dissipation.[1,2] In a three-dimensional (3D) structure such as a FinFET, although the transverse band-to-band (T-BTBT) tunneling in the gate-to-drain overlap region can be suppressed by reducing the transverse electric field, the band overlap between the valence band of the body and the conduction band of the drain region enables substantial longitudinal band-to-band tunneling (L-BTBT) in the OFF state.[3] Therefore, 3D transistors for low-power applications are severely limited by L-BTBT. Over the past few years, some attempts have been made to reduce L-BTBT.[4–8]

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In our previous work, polycrystalline silicon fin-like thin-film transistors ((poly-Si FinTFTs) with a wide drain structures were simulated.[9] Extending the wide drain can effectively suppress the longitudinal electric field near the drain and improve L-BTBT. Because of their electron mobility being higher than that of amorphous silicon (a-Si), poly-Si TFTs exhibit a high carrier mobility and therefore a fast transient response and a high current-driving capability, which are suitable for system-on-panel (SoP) or system-on-glass (SoG) applications. The suppression of the GIDL current in poly-Si TFTs has become an important issue. Channel length scaling can improve the carrier mobility of the poly-Si TFTs owing to the reduced numbers of grain boundaries in the channel.[10] As the channel length decreases, however, the short-channel effect (SCE) becomes more pronounced. Three-dimensional multigate structures,[11–13] such as double-gate, tri-gate, and gate-all-around (GAA) structures, as well as the low-temperature microwave annealing (MWA) method[14,15] are known as to improve gate controllability and restrict dopant diffusion, respectively, and effectively suppress the SCE. In this study, tri-gate FinTFTs with various extended wide drain lengths (L_{EX}) are fabricated and the off leakage current for the different structures is investigated. The devices at different temperatures are also analyzed.

2. Materials and Methods

All the poly-Si FinTFTs discussed in this study are fabricated on a 6” silicon wafer with a 1-μm-thick wet oxide layer as the substrate. A 100-nm-thick undoped a-Si layer is deposited on the substrate by low-pressure chemical vapor deposition (LPCVD) as the active layer. After the solid phase crystallization (SPC) of the a-Si layer at 600 ℃ for 24 h in nitrogen ambient, the polycrystalline silicon layer is defined. The active region is then patterned by electron-beam lithography and transferred by reactive ion etching to form multiple nanowires (NWs). Thereafter, a 50-nm-thick tetraethyl orthosilicate (TEOS) layer is deposited by LPCVD as a gate insulator and a 100-nm-thick *in situ* n+ poly-Si layer is deposited and patterned to form the gate electrode. Subsequently, the drift region and the self-aligned source and drain are implanted with BF_2^{49+} at 20 keV at doses of 5×10^{14} and 5×10^{15} cm^{-2}, respectively. Dopants are activated by low-temperature MWA at 2400 W for 300 s below 550 °C. Finally, a 300-nm-thick TEOS oxide passivation layer is deposited followed by Ti/TiN/AlSiCu/TiN contact metallization. The electrical characterization is carried out by on-wafer measurements using an Agilent 4155C semiconductor parameter analyzer and Agilent EasyEXPERT software.

3. Results and Discussion

3.1 Poly-Si FinTFT structures

Figure 1 shows schematic top views of the poly-Si FinTFTs with L_{EX} = 0, 0.8, and 1.6 mm. The channel length (L) is 0.7 mm. The metal field plate is connected to the gate electrode as a gate field plate (GFP) and the drift region is undoped, which helps to improve the breakdown voltage by spreading the depletion region at the surface and lowering the electric field. Figure 2

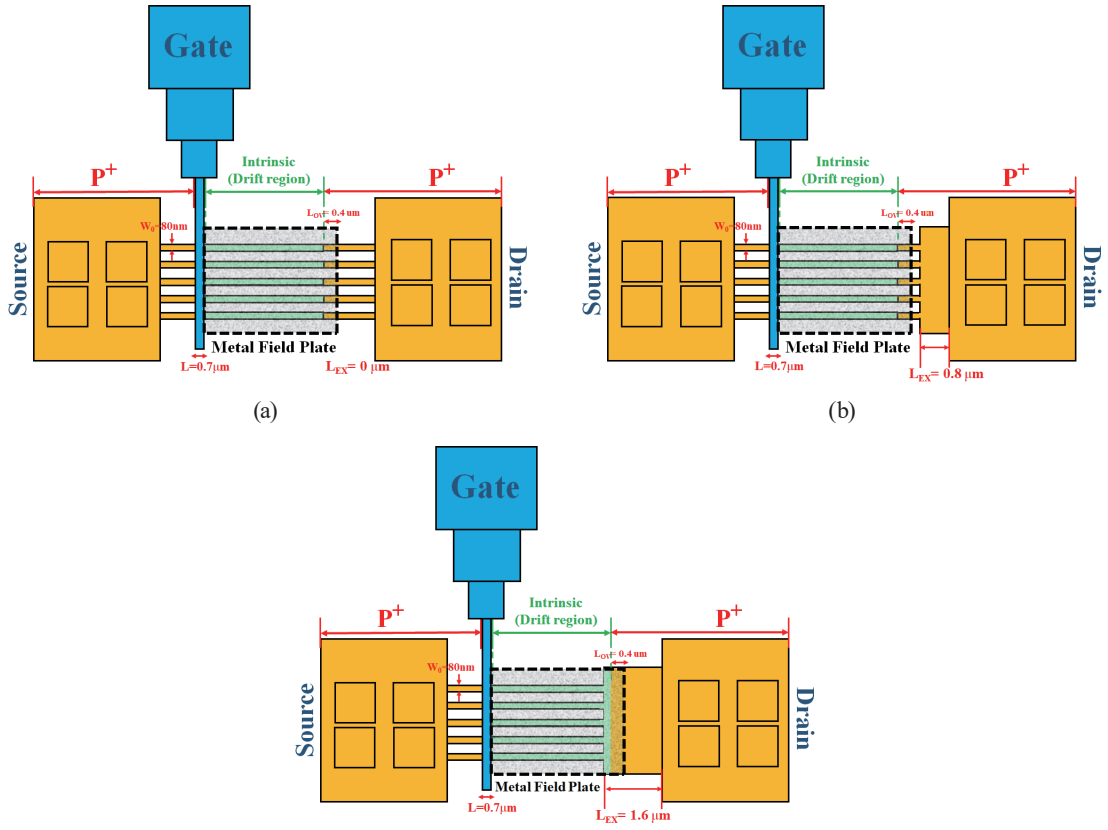

Fig. 1. (Color online) Schematic top view of poly-Si TFTs with (a) L_{EX} = 0 μm, (b) L_{EX} = 0.8 μm, and (c) L_{EX} = 1.6 μm.

Fig. 2. TEM image of a single NW.

shows a cross-sectional transmission electron microscopy (TEM) image of a single NW. The bottom side of each channel wire (W_0) is about 80 nm. The measured width of each channel wire (W_{nw}) is approximately 280 nm and the number of fins is five. Therefore, the effective channel width W_{eff} is 14 mm. All the poly-Si FinTFTs measured in this work have the same W_{eff}.

3.2 Leakage current of the poly-Si FinTFTs with various L_{EX}

Figure 3(a) shows the transfer characteristic curves of the poly-Si FinTFTs with various L_{EX}. The leakage currents of the poly-Si FinTFTs are clearly different for each sample and, as such, are governed by different leakage mechanisms. The leakage mechanisms for poly-Si FinTFTs are primarily derived from band-to-band tunneling (BTBT) and trap-assisted tunneling (TAT). In Fig. 3(a), the leakage current becomes larger as L_{EX} increases from 0 to 0.8 mm and has a strong dependence on the gate voltage. As L_{EX} increases, the increase in ion implantation area causes the generation of more traps and leads to a higher leakage current. In addition, increasing L_{EX} can reduce the longitudinal electric field at the intrinsic drift /N+ junction and improve the leakage current derived from L-BTBT.[9] Therefore, the leakage current of the poly-Si FinTFTs with L_{EX} = 0.8 mm being higher than those with L_{EX} = 0 mm is mainly due to the larger number of traps resulting from ion implantation. When L_{EX} increases to 1.6 mm, the leakage current is higher at a low gate voltage than for the other values of L_{EX} and shows a weak dependence on the gate voltage. The results indicate that TAT rather than BTBT dominates the leakage current of the poly-Si FinTFTs with L_{EX} = 1.6 mm. To improve the electrical characteristics of the poly-Si TFTs, MWA at 1.2 kW for 100 s in N_2 ambient instead of forming gas annealing is carried out as a post-metallization annealing (PMA) process [shown in Fig. 3(b)]. After PMA, in contrast, the leakage current decreases as L_{EX} increases from 0 to 0.8 mm, which is attributed to the reduction in interface trap density. Therefore, the leakage current of the poly-Si FinTFTs with L_{EX} = 0.8 mm being lower than that of the FinFETs with L_{EX} = 0 mm is mainly due to the longitudinal electric field at the intrinsic drift /N+ junction.

3.3 Leakage current of the poly-Si FinTFTs at different temperatures

To investigate the leakage mechanisms of poly-Si FinTFTs with various L_{EX}, transfer characteristic curves obtained at various temperatures are compared. Figure 4 shows the poly-Si FinTFTs with L_{EX} = 0.8 mm at 25, 50, 75, and 100 °C under drain voltages of −1 and −3 V.

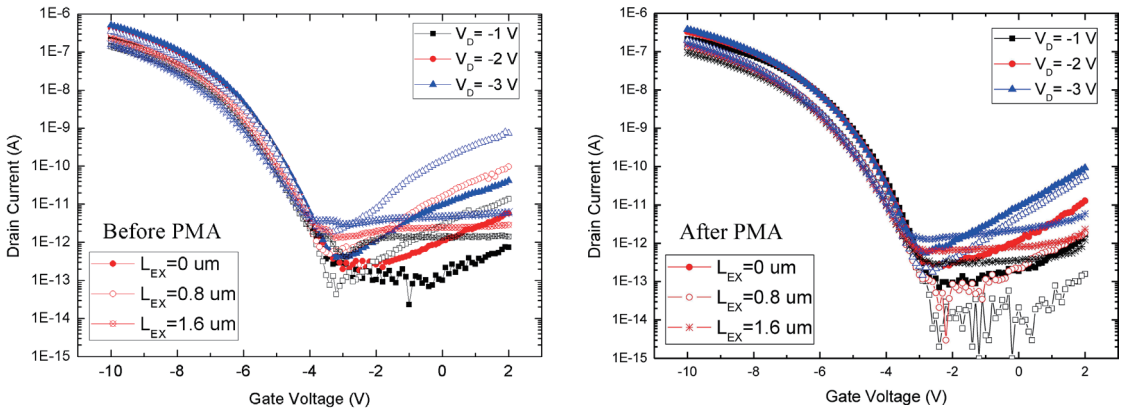

Fig. 3. (Color online) Measured transfer characteristic curves of the poly-Si FinTFTs with various L_{EX} (a) before and (b) after PMA.

The dependence of leakage current on temperature becomes less sensitive with increasing drain voltage. The bandgap change is small and decreases with increasing temperature. When the temperature is increased, there is a small bandgap change, resulting in a small increase in BTBT current. Therefore, the BTBT becomes dominant as the drain voltage increases.

Figure 5 shows the poly-Si FinTFTs with L_{EX} = 0 and 1.6 mm at a drain voltage of −3 V at various temperatures. When the drain voltage is fixed at −3 V, the temperature dependence of the leakage current is stronger for the poly-Si FinTFTs with L_{EX} = 1.6 mm than for those with L_{EX} = 0 and 0.8 mm (as shown in Figs. 4 and 5). However, the drain voltage dependence of the leakage current is weaker for the poly-Si FinTFTs with L_{EX} = 1.6 mm than for the others. These results confirm that TAT rather than BTBT dominates the leakage current of the poly-Si FinTFTs with L_{EX} = 1.6 mm. In addition, the temperature dependence of the leakage current becomes weak when the poly-Si FinTFTs undergo the PMA treatment. This result demonstrates that the trap density for the poly-Si FinTFTs is reduced by the PMA treatment.

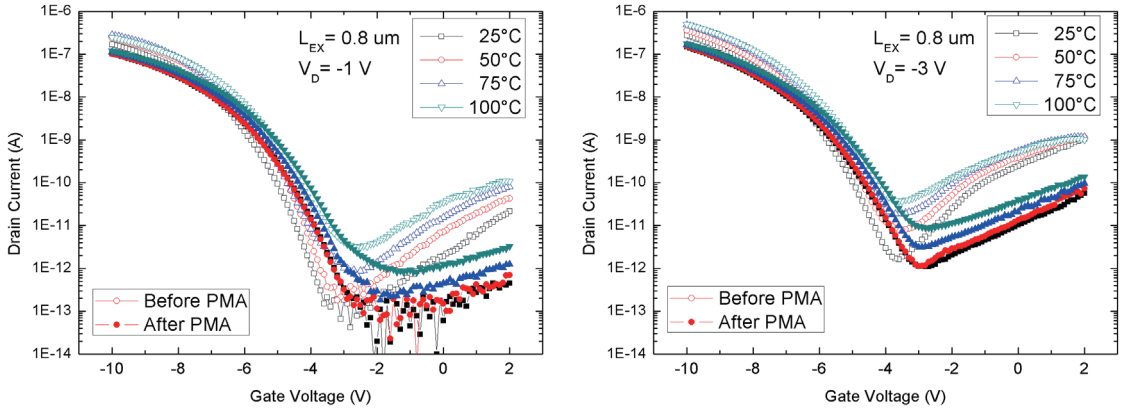

Fig. 4. (Color online) Measured transfer characteristic curves of poly-Si FinTFTs with L_{EX} = 0.8 μm at various temperatures at (a) V_D = −1 V and (b) V_D = −3 V.

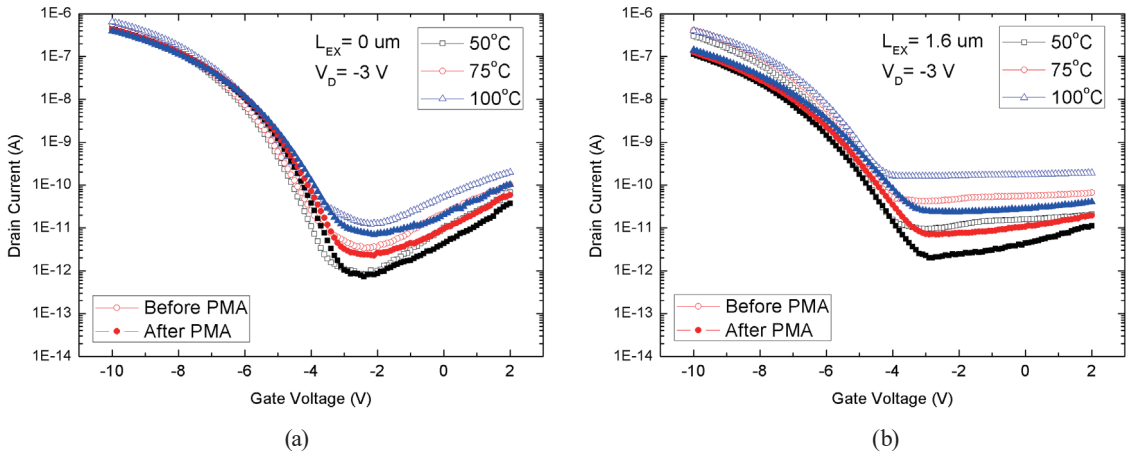

Fig. 5. (Color online) Measured transfer characteristic curves of poly-Si FinTFTs at V_D = −3 V at various temperatures with (a) L_{EX} = 0 μm and (b) L_{EX} =1.6 μm.

4. Conclusions

The off leakage current of poly-Si FinTFTs with different L_{EX} has been investigated. After PMA, the leakage current decreases as L_{EX} increases, especially at a high gate voltage and a high drain voltage. For a small L_{EX} (= 0 and 0.8 mm), the dependence of leakage current on temperature is less sensitive, which indicates that the BTBT is dominant. The BTBT is primarily dependent on drain voltage rather than on temperature. As L_{EX} increases to 1.6 mm, the weak dependence of leakage current on drain voltage and the strong dependence of leakage current on temperature indicate that TAT is the dominant leakage mechanism, where an increase in L_{EX} can reduce the longitudinal electric field and L-BTBT. These results provide an effective method of suppressing the GIDL current of FinFETs in which L-BTBT instead of T-BTBT is the primary source for 3D transistors such as FinFETs.

Acknowledgments

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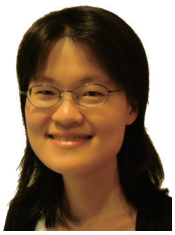

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