A Drive Control Method for Silicon Micro-gyroscopes

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The tracking ability of a silicon micro-gyroscope in a highly dynamic environment is a key factor for MEMS and inertial technology. To improve the tracking ability in a highly dynamic environment, a new drive control method for silicon micro-gyroscopes is proposed. First, a double closed-loop system with a phase-locked loop (PLL) and an automatic gain control (AGC) is designed to track the resonant frequency and stabilize the output amplitude. Second, the framework and corresponding algorithm of a second-order frequency-locked loop (FLL)-assisted third-order PLL were designed. Thereafter, the tracking performance characteristics of a third-order PLL and the proposed second-order-FLL-assisted third-order PLL at different frequency differences were simulated in Matlab Simulink. Simulation results show that the second-order-FLL-assisted third-order PLL can track the resonant frequency in a shorter time with a higher precision than the third-order PLL, and that the proposed method can still lock the resonant frequency of 11570 Hz when the frequency difference increases to 400 Hz, demonstrating its applicability in highly dynamic environments. Finally, the digital application specific integrated circuit (ASIC) test platform further validates the effectiveness of our proposed drive control method.

1. Introduction

Compared with traditional gyroscopes, silicon micro-gyroscopes have small size, light weight, high reliability, digitization, and intelligence, and are widely used in military, aerospace, and civil fields. Silicon micro-gyroscopes have become a research hotspot in the field of MEMS and inertial technology in recent decades.[1,2] The accuracy of silicon micro-gyroscope has always been a key issue in the study of micro-machined gyroscopes.[3,4] Maintaining the stability of the drive mode is the key to improving accuracy.[5] In addition, the printed circuit board (PCB) of the analog circuit is susceptible to interference from external environmental factors, such as package, temperature, and humidity, which affect the measurement accuracy. On the other hand, using electronic technology to achieve drive control can reduce external environment interference and improve measurement accuracy.[6]

The drive control mode affects the accuracy of silicon micro-gyroscopes, and the phase-locked loop (PLL) directly determines the precision of the drive control of silicon micro-gyroscopes. In Ref. 7, the drive control method of combining the PLL and automatic gain control (AGC) is proposed for silicon micro-gyroscopes to improve accuracy. The PLL is utilized to realize the synchronization of the driving and resonant frequencies, and the AGC stabilizes the amplitude of the resonant signal. In Ref. 8, the PLL is combined with self-oscillation, and the gyroscope used can achieve a frequency error of less than 0.01% in 0.3 s. In Ref. 9, the digital PLL is combined with the AGC as a drive control method. The reported results show that the start-up time of the gyroscope driver is about 0.6 s, but the tracking accuracy of the digital PLL was not mentioned. A previous research work[10] makes the AGC and software PLL (SPLL) work in parallel to ensure that the drive loop is self-excited and phase-locked, in which the SPLL is based on the Coordinated Rotation Digital Computer (CORDIC) algorithm.

The above-mentioned methods mainly use a PLL to track the resonant frequency. Our proposed method is different from the above methods. In our work, the PLL and frequency-locked loop (FLL) are combined to optimize the PLL to achieve a better driving frequency control for silicon micro-gyroscopes. By combining the PLL with the FLL, the frequency of the drive signal is first tracked by the FLL, and then the PLL compensates for the output phase of the FLL to achieve a more accurate tracking of the resonant frequency. The method overcomes the shortcoming of a third-order PLL, which is easy to lose lock in a highly dynamic environment, and maintains the high-precision characteristics of the third-order PLL. The simulation results obtained using the MATLAB Simulink software and experimental results on the digital Application Specific Integrated Circuit (ASIC) verify the effectiveness of the proposed method.

2. Design of Drive Control System

To maintain the output frequency of a silicon micro-gyroscope equal to the resonant frequency and to keep the output amplitude stable, a double closed-loop control system with an improved PLL and an AGC loop is proposed in our method.

As shown in Fig. 1, the drive mode of the silicon micro-gyroscope adopts the double closed-loop control, in which the PLL is used for phase control and the AGC is used for amplitude control. PLL and AGC loop control processes are both executed on the FPGA board. On the forward channel of the double closed-loop control system, DAC is digital-to-analog conversion, C/V is capacitance-to-voltage conversion, and ADC is analog-to-digital conversion. A butterfly-shaped single-mass gyroscope chip was adopted in our work, and its output is passed through a C/V circuit, and then the derived voltage is converted into a digital signal by an ADC circuit. The quality factor Q_x of the gyroscope used is 23134, the resonant frequency ω_x is $2\pi \times 11570$ rad/s, and the drive equivalent mass m_x is 7e−6 kg.

The feedback channel of the PLL is composed of a phase detector (PD), an IIR loop filter (LF), and a voltage-controlled oscillator (VCO). This loop obtains the frequency error by comparing the resonant frequency with the VCO frequency, and then outputs the error voltage. The IIR LF
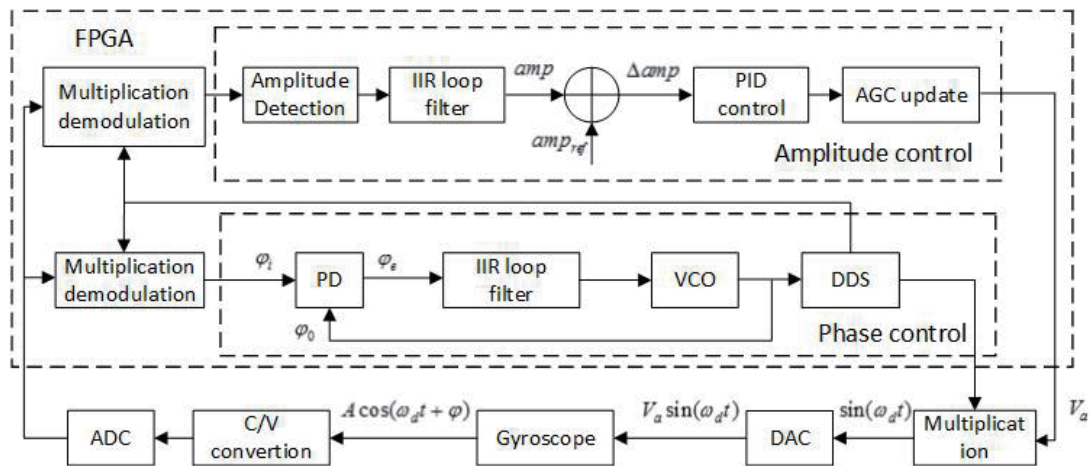
Fig. 1.   Framework of double closed-loop drive system of silicon micro-gyroscope.

is used to obtain the low-frequency component of its input signal. The VCO is then controlled such that the output frequency is consistent with the resonant frequency. The feedback channel of the AGC is composed of an amplitude demodulator, an IIR LF, a proportional-integral-differential (PID) control algorithm module, and an AGC update module. The amplitude demodulator extracts the amplitude of the system output through multiplication demodulation and amplitude detection. The DC voltage obtained through the IIR LF is compared with the reference amplitude to derive the amplitude error. This error is input to the PID control algorithm module, and the AGC update module generates gain feedback to the silicon micro-gyroscope.

3.   Design of Third-order PLL

The block diagram of the mathematical model of the third-order PLL is shown in Fig. 2. The PD is used to identify the phase error of two input signals, which are the output ϕ_i of the silicon micro-gyroscope and the VCO output ϕ_o. The LF is used to filter out the high-frequency portion of the phase error to obtain low-frequency components. The output voltage of the LF controls the phase of the VCO and changes the output frequency by phase.

3.1   Mathematical model of third-order PLL

One of the two inputs of the PD is the output of the silicon micro-gyroscope, denoted as

$$v_i(t) = V_{im}\sin(\omega_i t + \phi_1),\tag{1}$$

and the other is the VCO output, denoted as
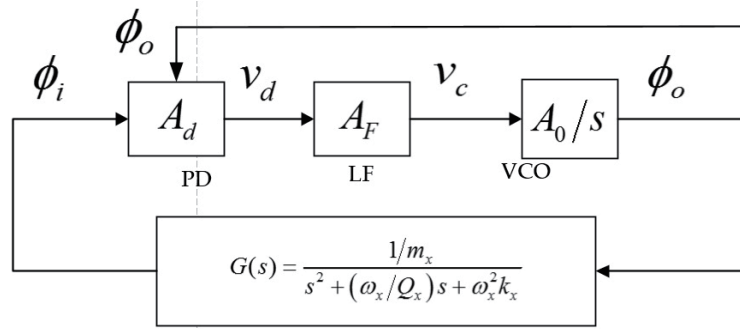
$$v_o(t) = V_{om}\cos(\omega_o t + \phi_2),\tag{2}$$

Fig. 2.   Block diagram of the mathematical model of the third-order PLL.

where ω_i is the output frequency of the gyroscope and ω_o is the output angular frequency when the VCO is controlled by the control voltage in the closed loop. Assuming the initial phase as 0, then

$$\phi_e\left(t\right)=\phi_i\left(t\right)-\phi_o\left(t\right)=\left(\omega_i-\omega_o\right)t. \tag{3}$$

The mathematical model of the PD is

$$v_d\left(t\right)=A_d\sin\phi_e\left(t\right)=A_d\sin(\omega_i-\omega_o)t, \tag{4}$$

where A_d is the maximum output voltage of the PD. The output of the PD is a sinusoidal function of the frequency error. This is a nonlinear function that can be approximated as a linear function if ϕ_e is between −90 and 90°.

The output voltage of the PD is filtered and de-noised by an LF to output DC components. Here, a second-order LF is adopted, and the mathematical model of the LF is

$$v_c\left(t\right)=A_F v_d\left(t\right), \tag{5}$$

where A_F is the transfer function of the second-order filter, which will be further introduced in Sect. 3.2.

The phase-controlled model of the VCO is

$$\int_0^t\omega_0\left(\tau\right)d\tau=\omega_r t+A_0\int_0^t v_c\left(\tau\right)d\tau, \tag{6}$$

where $\omega_r t$ is the instantaneous reference phase. The following formula is obtained by the integral operation of Eq. (6)

$$\phi_0\left(t\right)=A_0\int_0^t v_c\left(\tau\right)d\tau=\frac{A_0}{s}v_c\left(t\right). \tag{7}$$

The mathematical equation of the overall phase relationship is

$$\phi_e = \phi_i - \phi_0 = \phi_i - \frac{A_0}{s} A_F A_d \sin \phi_e .$$

(8)

3.2　Analysis and implementation of LF

A second-order digital filter of the IIR type is adopted in the third-order PLL, and the transfer function of an ideal second-order filter is $A_F = (1 + \tau_2 s)^2 / \tau_1^2 s^2$, where τ_1 and τ_2 are time constants of the transfer function. Thus, the open-loop transfer function of the third-order PLL is expressed as

$$G(s) = A_d \cdot A_F \cdot \frac{A_0}{s} = \frac{A_d A_0 (1 + \tau_2 s)^2}{\tau_1^2 s^3},$$

(9)

and the closed-loop transfer function of the third-order PLL is

$$\Phi(s) = \frac{K(1 + \tau_2 s)^2}{\tau_1^2 s^3 + K(1 + \tau_2 s)^2},$$

(10)

where $K = A_d A_0$. The stability analysis of the closed-loop transfer function is performed according to Bode's law. The critical frequency is then computed as

$$\omega_T = K \left(\frac{\tau_2}{\tau_1} \right)^2 .$$

(11)

To ensure the stability of the loop, the phase angle condition $\phi(\omega) = 2\arctan \omega_T \tau_2 - 270° + 180° > 0$ must be satisfied. Thus, we have the following inequality:

$$\omega_T \tau_2 > 1 \text{ or } \omega_T > \frac{1}{\tau_2} .$$

(12)

Combining Eqs. (11) and (12), we obtain

$$K > \frac{\tau_1^2}{\tau_2^3} .$$

(13)

Then, we make $r = \omega_T \tau_2 = K \frac{\tau_1^2}{\tau_2^3}$ and compute the bandwidth according to the integral theorem as

$$B_L = \frac{r}{4\tau_2} \frac{2r+3}{2r-1}. \tag{14}$$

At the same time, the phase margin can be obtained as

$$\phi(\omega_T) = 2\arctan r - 90^\circ. \tag{15}$$

After the bandwidth and phase margin are known, we obtain $\tau_1 = \sqrt{\dfrac{K\tau_2{}^3}{r}}$ and $\tau_2 = \dfrac{r}{4B_L} \dfrac{2r+3}{2r-1}$.

When the phase margin $\phi(\omega_T) = 50^\circ$ and the filter bandwidth $\omega_T = 100$ Hz, we have $\tau_1 = 0.0032$ and $\tau_2 = 0.0616$. Thus, the transfer function of the second-order filter is known. $s = \dfrac{2}{T} \dfrac{1-z^{-1}}{1+z^{-1}}$ will be brought into the open-loop transfer function and the coefficients G_1, G_2, and G_3 of the digital filter of the IIR type are derived when compared with the standard formula of the IIR-type filter. The second-order digital filter structure is shown in Fig. 3.

4.   Method of Second-order-FLL-assisted Third-order PLL

It is difficult to meet system performance in a highly dynamic process because the bandwidth will become smaller when the PLL achieves a higher tracking accuracy. To solve this problem, we use the FLL to quickly capture the tracking frequency and obtain the frequency error, and then perform phase compensation by utilizing the PLL to improve the tracking accuracy. Such a design combines the advantages of both the FLL and the PLL to track the frequency with a high precision within a reasonable time in a highly dynamic environment. Figure 4 shows a block diagram of the second-order-FLL-assisted third-order PLL.

4.1   Model of discriminator

The discriminator used in our methods includes a frequency detector and a PD. The model of the discriminator has two inputs, one from the output of the resonator and the other from the VCO output. After the resonator and feedback signals are computed by integration, two signals of I and Q are obtained. Then, the I and Q signals enter the frequency detector and
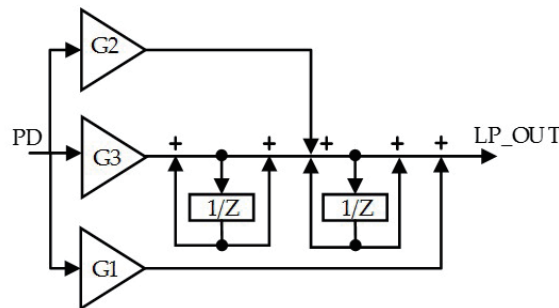

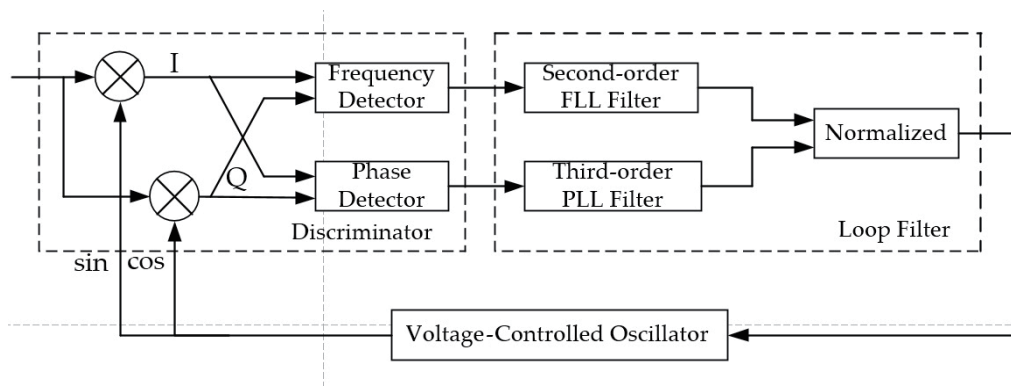Fig. 3.   Second-order filter structure.

Fig. 4.   Structure of the second-order-FLL-assisted third-order PLL.

PD simultaneously. The frequency detector and PD perform specific calculations on *I* and *Q*. Then, the outputs from the frequency detector enter the second-order FLL filter and the outputs from the phase detector enter the third-order PLL filter. The related calculation operations on the frequency and phase detectors are described as

$$cross = I(n-1) \times Q(n) - I(n) \times Q(n-1), \tag{16}$$

$$dot = I(n) \times I(n-1) + Q(n) \times Q(n-1). \tag{17}$$

The output of the frequency detector is denoted as *FD*, computed by

$$FD = a\tan 2(cross, dot)/(t_2 - t_1), \tag{18}$$

which can be further expressed as the frequency error $\dfrac{(\phi_2 - \phi_1)}{(t_2 - t_1)}$.

The output of the phase detector is denoted as *PD*, computed by

$$PD = a\tan 2(Q(n), I(n)), \tag{19}$$

which can also be expressed as the phase error $\phi_2 - \phi_1$.

The characteristic diagram of the function ATAN2 is shown in Fig. 5. As shown in Fig. 5, when the frequency error is in the range of [−180°, 180°], the linearity of the function ATAN2 is good. Thus, the frequency and phase errors can be accurately estimated.

4.2   Second-order-FLL-filter-assisted third-order PLL filter

As shown in Fig.4, the second-order FLL filter filters and de-noises the frequency error of the frequency detector to obtain a DC component, and the third-order PLL filter filters and de-noises the phase error of the phase detector to obtain a DC component. Then, the outputs of the second-order FLL and third-order PLL filters are normalized, and the normalized result
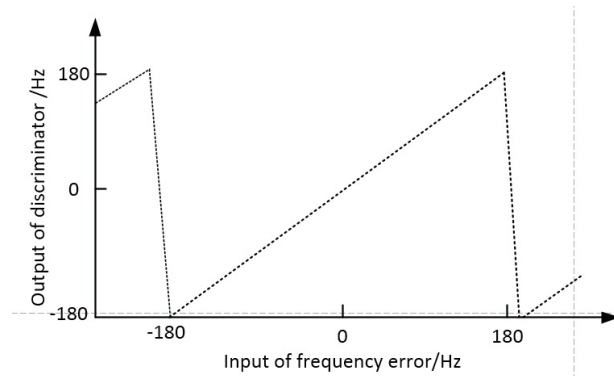
Fig. 5. Characteristic diagram of function ATAN2.

controls the VCO to generate instantaneous frequency and phase, and both frequency and phase are fed back to superpose the frequency and phase of the input signal. Through such a working mechanism, the output signal maintains the same frequency and phase as the input signal.

Figure 6 shows the block diagram of the second-order-FLL-filter-assisted third-order PLL filter. The second-order FLL filter uses a first-order filter, and the third-order PLL filter uses a second-order filter. Assume the bandwidth of the FLL filter, $B_{LF} = 30$ Hz, and the bandwidth of the PLL filter, $B_{LP} = 60$ Hz. According to the filter characteristics, we can obtain the parameters of the second-order FLL and third-order PLL filters as $cf_1 = 80.0378$, $cf_2 = 3204$, $cp_1 = 183.5564$, $cp_2 = 6434.5$, and $cp_3 = 447380$.

As shown in Fig. 6, FD is the output of the frequency detector and serves as the input to the second-order FLL filter, and PD is the output of the phase detector and serves as the input to the third-order PLL filter. T is the sampling time. The output of the second-order FLL filter is

$$FD_{out} = cf_1 \cdot T \cdot \frac{1}{2} \cdot \frac{1+z^{-1}}{1-z^{-1}} + cf_2 \cdot T^2 \cdot \frac{1}{4} \cdot \frac{\left(1+z^{-1}\right)\left(1+z^{-1}\right)}{\left(1-z^{-1}\right)\left(1-z^{-1}\right)}$$
$$= \frac{\left(cf_1 \cdot T \cdot \frac{1}{2} + cf_2 \cdot T^2 \cdot \frac{1}{4}\right) + \left(cf_2 \cdot T^2 \cdot \frac{1}{2}\right)z^{-1} + \left(-cf_1 \cdot T \cdot \frac{1}{2} + cf_2 \cdot T^2 \cdot \frac{1}{4}\right)z^{-2}}{1-2z^{-1}+z^{-2}} \tag{20}$$

The output of the third-order PLL filter is

$$PD_{out} = cp_1 + cp_2 \cdot T \cdot \frac{1}{2} \cdot \frac{1+z^{-1}}{1-z^{-1}} + cp_3 \cdot T^2 \cdot \frac{1}{4} \cdot \frac{\left(1+z^{-1}\right)\left(1+z^{-1}\right)}{\left(1-z^{-1}\right)\left(1-z^{-1}\right)}$$
$$= \frac{\left(cp_1 + cp_2 \cdot T \cdot \frac{1}{2} + cp_3 \cdot T^2 \cdot \frac{1}{4}\right) + \left(-2 \cdot cp_2 + cp_3 \cdot T^2 \cdot \frac{1}{2}\right)z^{-1} + \left(cp_1 - cp_2 \cdot T \cdot \frac{1}{2} + cp_3 \cdot T^2 \cdot \frac{1}{4}\right)z^{-2}}{1-2z^{-1}+z^{-2}} \tag{21}$$
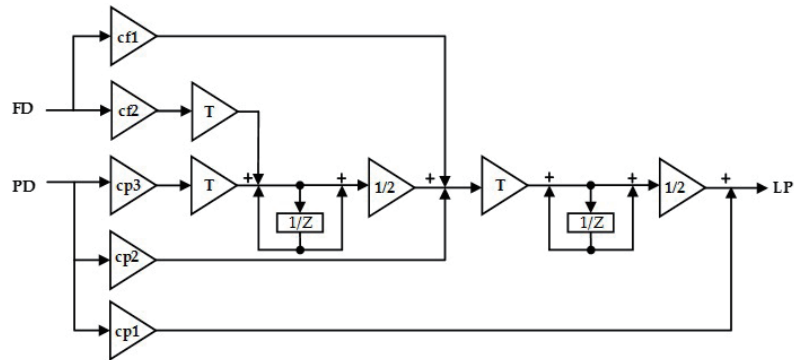
We make

Fig. 6.   Block diagram of the second-order-FLL-filter-assisted third-order PLL filter.

$$cf(1) = cf_1 \cdot T \cdot \frac{1}{2} + cf_2 \cdot T^2 \cdot \frac{1}{4}, \tag{22}$$

$$cf(2) = cf_2 \cdot T^2 \cdot \frac{1}{2}, \tag{23}$$

$$cf(3) = -cf_1 \cdot T \cdot \frac{1}{2} + cf_2 \cdot T^2 \cdot \frac{1}{4}, \tag{24}$$

$$cp(1) = cp_1 + cp_2 \cdot T \cdot \frac{1}{2} + cp_3 \cdot T^2 \cdot \frac{1}{4}, \tag{25}$$

$$cp(2) = -2 \cdot cp_2 + cp_3 \cdot T^2 \cdot \frac{1}{2}, \tag{26}$$

$$cp(3) = cp_1 - cp_2 \cdot T \cdot \frac{1}{2} + cp_3 \cdot T^2 \cdot \frac{1}{4}. \tag{27}$$

The final output of the filter (denoted as *LP*) is the sum of the output of the second-order FLL and third-order PLL filters. Thus, the total output can be expressed as

$$LP(n) = \frac{\left(cf(1)FD(n) + cp(1)PD(n)\right) + \left(cf(2)FD(n-1) + cp(2)PD(n-1)\right)z^{-1} + \left(cf(3)FD(n-2) + cp(3)PD(n-2)\right)z^{-2}}{1 - 2z^{-1} + z^{-2}}. \tag{28}$$

According to Eq. (28), we can obtain the following iteration equation:

$$LP(n) = 2 \cdot LP(n-1) - LP(n-2) + cf \cdot FD' + cp \cdot PD', \tag{29}$$

where *FD′* is the transposition of the input signal *FD* and *PD′* is the transposition of the input signal *PD*.

5. Experimental Results

5.1 Comparison and analysis of simulation results

To compare the performance characteristics of the third-order and the second-order-FLL-assisted third-order PLLs, both were implemented under the same conditions and the simulation results were analyzed. In the simulation, the sampling frequency was set to 512000 Hz and the resonant frequency to 11570 Hz. Figure 7 shows the simulation results of the third-order and second-order-FLL-assisted third-order PLLs at different frequency differences. The results in Fig. 7(a) show that the third-order PLL can accurately track the resonant frequency of the silicon micro-gyroscope when the frequency difference is smaller than 20 Hz. When the frequency
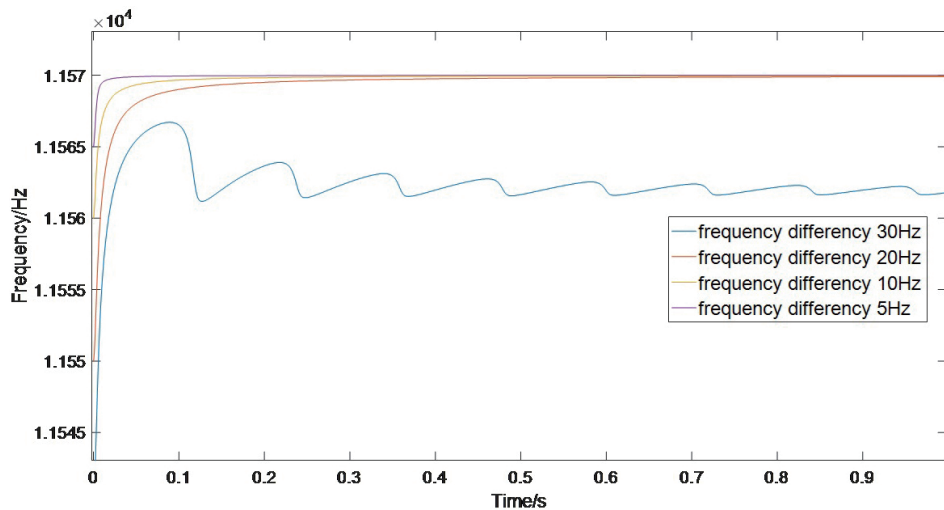
(a)
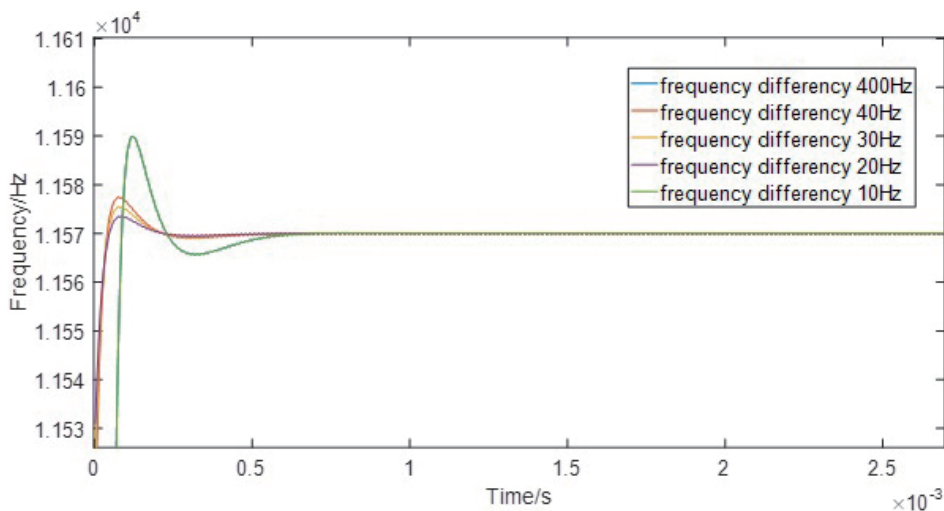
(b)

Fig. 7. (Color online) Simulation results at different frequency differences. (a) Simulation results of third-order PLL. (b) Simulation results of second-order-FLL-assisted third-order PLL.

difference increases to 30 Hz, the third-order PLL loses lock and the resonant frequency will not be accurately tracked. The results in Fig. 7(b) show that the second-order-FLL-assisted third-order PLL can lock the resonant frequency in 4.944×10^{-4} s when the frequency difference increases to 40 Hz. When the frequency difference continues to increase to 400 Hz, we found that the second-order-FLL-assisted third-order PLL can still lock the resonant frequency in 6.757×10^{-4} s. As the frequency difference increases, the locking time becomes longer, but the locking time required by our method is still relatively short, which is better than the responding value of other methods.[8,9]

A comparison of the two methods at the same frequency difference of 10 Hz is shown in Fig. 8. The simulation results show that the lock time of the third-order PLL is 0.057 s and the
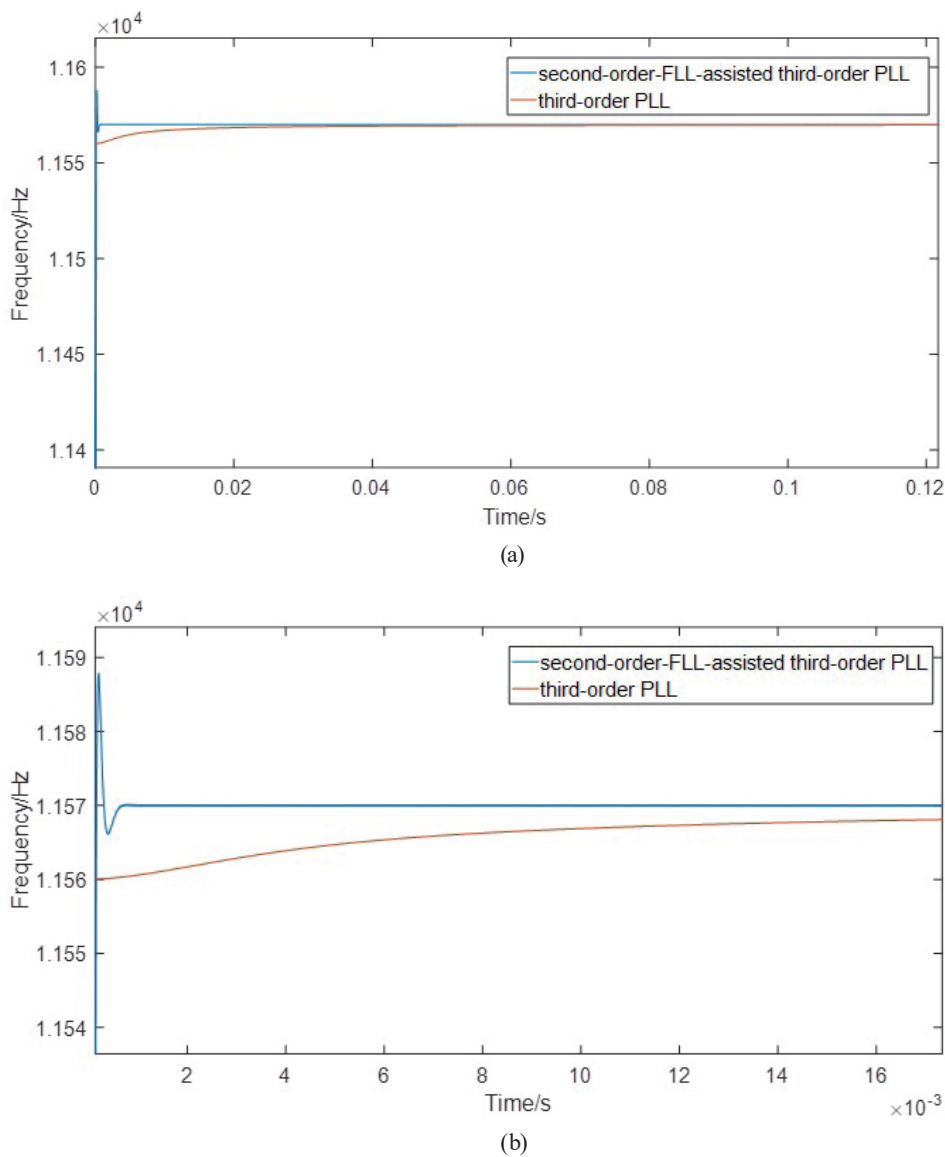

Fig. 8. (Color online) Simulation comparison of two different methods at the same frequency difference. (a) Simulation comparison of two methods at the frequency difference of 10 Hz. (b) Partial enlargement.

stabilization error is 4×10^{-5} Hz. On the other hand, the second-order-FLL-assisted third-order PLL locks the resonant frequency in 4.588×10^{-4} s with an error of 4×10^{-6} Hz.

From the above simulation results, we can conclude that the dynamic performance of the second-order-FLL-assisted third-order PLL is better than that of the third-order PLL, and the tracking accuracy remains high even at relatively large frequency differences. Therefore, the second-order-FLL-assisted third-order PLL is more suitable for the drive control of the high-precision silicon micro-gyroscope in highly dynamic environments.

5.2 Results on digital ASIC platform

As shown in Fig. 9, the circuit test board is mainly composed of three layers. The bottom layer is a gyroscope chip and C/V conversion board, the middle layer is A/D and D/A conversion board, and the top layer is a field-programmable gate array (FPGA) chip board. A self-developed butterfly-shaped single-mass gyroscope is used for the silicon micro-gyroscope chip and a Xilinx KINTEX-7 series FPGA development board is used in the experiments. There are two sets of power modules. The power supply of the analog circuit provides ±5 V and the power supply of the digital circuit provides +12 V.

In addition, the experimental devices used are as follows.
1. Single-axis high-speed temperature-controlled turntable of type SLT-01VI-100C
2. Agilent DSO7034B oscilloscope
3. ROHDE&SCHWARZ signal analyzer
4. GWINSTEK GPR-1820HD DC power supply
5. GWINSTEK APS-7000 AC power supply
6. Data processing computer

The experiments were executed in a temperature-controlled turntable, and the temperature in the turntable was controlled to 25° C, the same as room temperature. At the beginning of the experiment, the frequency of the silicon micro-gyroscope's drive mode was measured as 11570 Hz by the sweep frequency method; the drive quality factor is 23134, and the drive equivalent mass is 7e−6 kg.
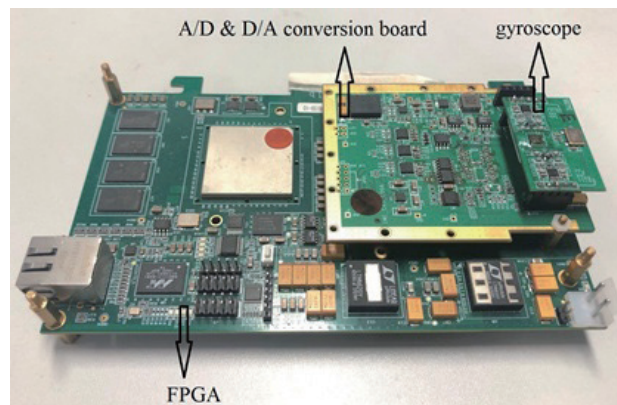

Fig. 9.   (Color online) Circuit test board.

 The FFT results of the gyroscope output after digital signal processing are shown in Fig. 10, indicating that the frequency before adding the second-order-FLL-assisted third-order PLL module is 11566.4 Hz and the amplitude is 1149.01. The frequency after adding the second-order-FLL-assisted third-order PLL module is 11570.3 Hz, which is closer to the resonant frequency of 11570 Hz, and the amplitude is 3201.38. It is clear that the output amplitude increases and the output frequency is closer to the resonant frequency, as determined by using our proposed method.
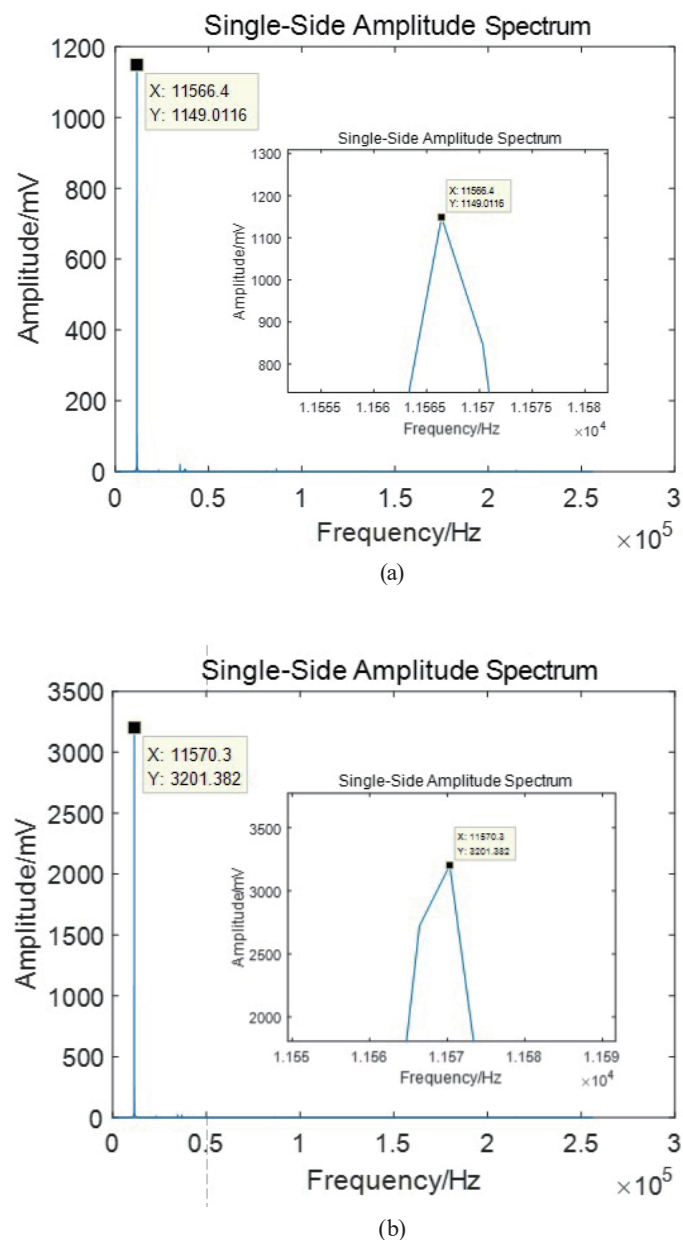

Fig. 10. (Color online) Spectrum analysis of drive output. (a) Spectrum analysis of drive output before locking. (b) Spectrum analysis of drive output after locking.

Table 1
Results of the comparison of our proposed method with other similar methods.

Method	Resonant frequency	Stabilization error
Quadrature phase-locked loop (QPLL)[11]	2872.13 × 2π rad/s	200 Hz
PLL+AGC [12]	357.9 kHz	±15 Hz
Controllor [13]	73412 Hz	15 Hz
Our proposed method	11570 Hz	0.3 Hz

Results of the comparison of our proposed method with other similar methods[11–13] are shown in Table 1. We have listed the reported values of the corresponding methods in those papers.[11–13] It can be seen from Table 1 that our proposed drive control method has advantages over other methods in terms of stabilization precision.

6. Conclusion

To stabilize the frequency and amplitude of drive output, we designed a double closed-loop control loop, in which a PLL is used to stabilize the frequency of the drive output and an AGC is used to stabilize the amplitude of the drive output. The drive control method for a second-order-FLL-assisted third-order PLL is further proposed to improve the tracking frequency. Simulation results show that the tracking speed and stability accuracy of the proposed second-order-FLL-assisted third-order PLL are higher than those of a third-order PLL. Finally, the performance of the proposed method was tested on a digital ASIC platform. Experimental results show the advantages of our designed drive control system in terms of spectrum analysis. Moreover, our proposed method performed better than some other published methods in terms of stabilization precision.

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