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Characteristics of Tunnel Field-effect Transistors under Power-on Electrostatic Discharge and Electrical Overstress Conditions

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The power-on electrostatic discharge (ESD) and electrical overstress (EOS) events are causing an increasing number of failures in modern integrated circuits (ICs). Tunnel field-effect transistors (TFETs) are considered as a better choice than shallow trench isolation diodes in whole-chip ESD protection networks. We have investigated the characteristics of TFETs under power-on ESD and EOS conditions by numerical simulation. The impact of an elevated ambient temperature, variations in current rise time and discharge duration, and the device structure on the triggering voltage and failure current are evaluated. The obtained results are discussed with detailed physical insights.

1. Introduction

Low power is a key requirement of future integrated circuits (ICs) and requires energy-efficient devices. Although conventional MOSFETs continue to be improved by adopting three-dimensional (3D) structures, alternative materials, and short dimensions, devices with different physical mechanisms are essential for further improvement.[1–4] Tunnel field-effect transistors (TFETs) based on the band-to-band tunneling (BTBT) mechanism can achieve small subthreshold swings.[5–7] One of the advantages of TEFTs is that they are compatible with CMOS technology; thus, the concept of mixed MOSFET–TFET circuits was proposed and some new applications such as electrostatic discharge (ESD) protection with a TFET have been investigated.[8–14] It was found that a TFET can be a better choice than a shallow trench isolation (STI) diode in a whole-chip ESD protection network.[10]

Recently, an increasing number of IC failures have been observed under power-on ESD and electrical overstress (EOS) conditions. Two features of power-on conditions are an elevated ambient temperature and different current rise times and discharge durations. In this study, the characteristics of TFETs under power-on conditions are investigated by technology computer-aided design (TCAD) simulation. The impact of key parameters and materials engineering on the power-on ESD and EOS characteristics of TEFTs is also discussed in this paper. Results are explained by analyzing the device triggering mechanism and heat dissipation.

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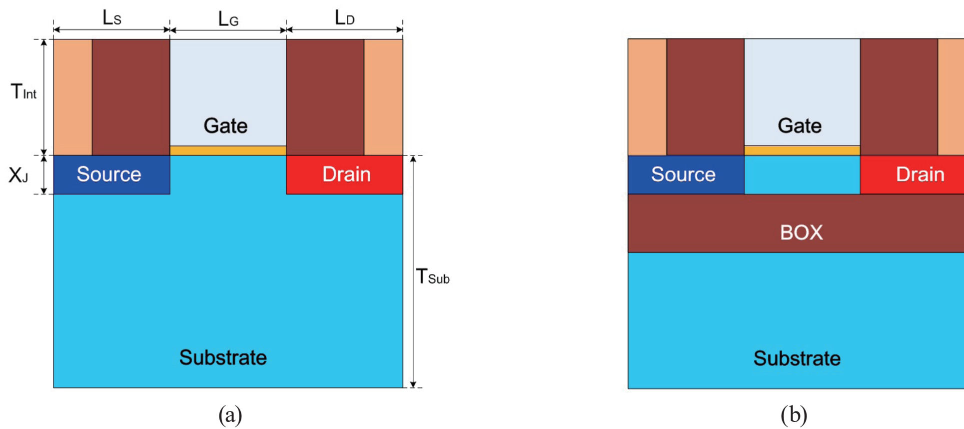
2. Devices and TCAD Methodology

2.1 ESD protection TFET and network

The devices studied in this work are point-tunneling TFETs in bulk and fully depleted-silicon-on-insulator (FDSOI) configurations as shown in Fig. 1. The default parameters are as follows: the thickness of gate oxide: T_{ox} = 4 nm, the height of interconnects: T_{Int} = 0.3 µm, the depth of the source and drain regions: X_j = 10 nm, and the lengths of the gate, source, and drain regions: $L_G = L_S = L_D$ = 100 nm. The doping concentrations of the source (p-type), drain (n-type), and substrate (p-type) regions are 1×10^{20}, 1×10^{20}, and 1×10^{17} cm^{-3}, respectively. The materials of the gate oxide, spacers, and interconnects are HfO_2, SiO_2, and copper, respectively. The thermal boundary conditions are very important in ESD simulation, and unsuitable conditions may produce incorrect results. Since the thermal diffusion length of silicon devices for 100 ns ESD simulation is approximately 3 µm, the substrate thickness T_{Sub} is chosen to be 3 µm.[15] All the four terminals, namely, the substrate, source, drain, and gate, are used as a heat sink. The surrounding temperature of the device is set as 300 K.

The basic concept of an ESD protection network using both TFETs and MOSFETs has been proposed.[10] As shown in Fig. 2, traditional STI diodes were replaced by TFETs with the gate



(a) (b)

Fig. 1. (Color online) (a) Bulk and (b) FDSOI TFETs examined in this study (not to scale).

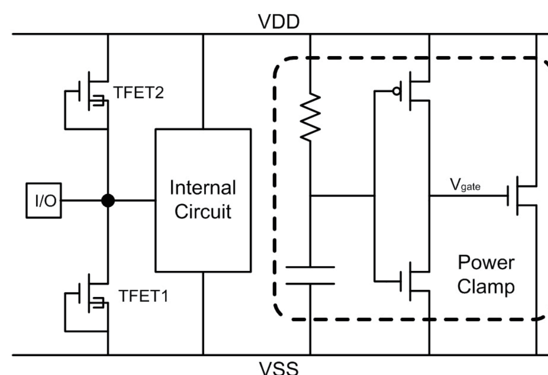


Fig. 2. ESD protection network with mixed MOSFET-TFET design.

connected to the source. A TFET is essentially a p-i-n diode in terms of its structure. Under a negative ESD stress, it works in the forward diode mode and has a high ESD robustness. However, under a positive ESD stress, it conducts the ESD current in the avalanche breakdown mode and has a relatively low ESD robustness. For an ESD current flowing from I/O to VSS, the primary path is from TFET2 (forward diode mode) to the VDD line and through the power clamp to VSS. The secondary path is from TFET1 (avalanche breakdown mode) to VSS.

2.2 TCAD methodology

The simulations in this study are carried out in a Synopsys TCAD simulator. The main carrier generation mechanisms are BTBT, avalanche generation, and thermal carrier generation. A dynamic nonlocal BTBT model is used to capture the tunneling current in the device. The van Overstraeten model is used to mimic the avalanche generation process. A thermodynamic model is used to calculate the lattice temperature. The Shockley–Read–Hall recombination model is also used. Since the devices are exposed to high stresses in ESD events, a high-field saturation mobility model is adopted. A band-gap narrowing model is also used since the source and drain regions are highly doped.

The transmission line pulsing (TLP) test method is used to simulate the quasi-static *I–V* characteristics of the TFETs. Under positive ESD events, currents flow from the drain into the device, while under the positive ESD events, they flow from the source into the device. For the TLP test, the rise time and pulse width are set at 10 and 100 ns, respectively, while for the very fast TLP (vfTLP), the two values are 0.1 and 5 ns, respectively.

3. Results and Discussion

3.1 Ambient temperature

Different from power-off ESD events, power-on ESD and EOS events may occur at a high ambient temperature.[16] The typical operating temperature requirement for ICs can reach 400 K; for some applications such as automotive electronics, this temperature may be even higher. The TLP *I–V* curves of the TFET at room temperature (300 K) and a high temperature (400 K) under positive ESD stresses are shown in Fig. 3(a). It can be seen that the failure current is reduced from 0.9 to 0.7 mA/μm when the ambient temperature is increased from 300 to 400 K. This is because the device fails when the lattice temperature reaches the critical value, and the elevated ambient temperature makes the failure occur earlier.

It is observed from Fig. 3(a) that the triggering voltage hardly changes when the ambient temperature is increased from 300 to 400 K. The impact ionization coefficient has a negative temperature dependence; at a higher temperature, a higher electric field is required for avalanche breakdown.[17] However, the TFET has a BTBT-assisted triggering mechanism in an ESD event, the BTBT current has a positive temperature dependence, and at elevated temperatures, more carriers can be provided for avalanche generation. Because of this combination of phenomena, the increase in triggering voltage can be neglected.

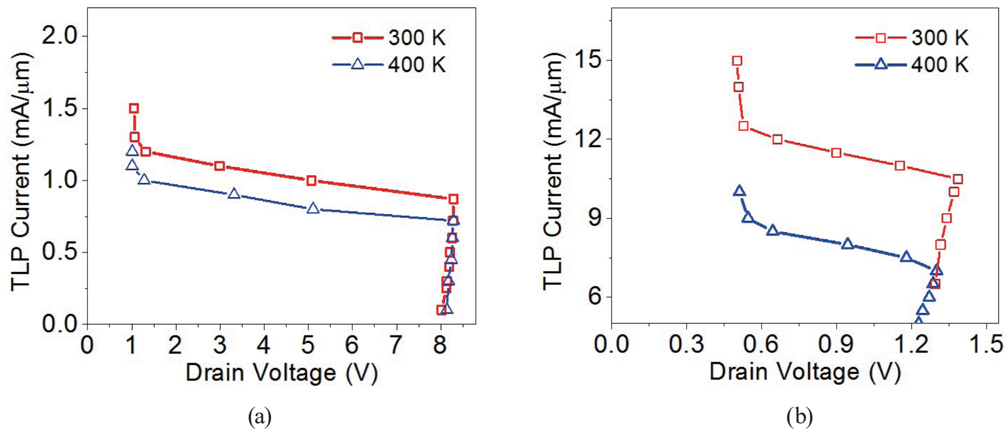


Fig. 3. (Color online) TLP I–V curves of TFET under (a) positive and (b) negative stresses at different ambient temperatures.

In the negative TLP simulation, the devices work in the diode mode, the trigger voltage is low, and the failure current is high. The failure current is reduced from 11 to 7 mA/μm when the temperature is increased from 300 to 400 K.

Drain doping concentration is a key parameter affecting the device characteristics because both the BTBT and the avalanche generation initially occur at the drain/channel junction. Both the impact ionization coefficient and the BTBT rate have a positive dependence on the doping concentration; with the decrease in drain doping concentration, the turn-on voltage increases, more heat is generated, and the failure current decreases. Simulation results are shown in Fig. 4. At 300 and 400 K, the failure current decreases by 24 and 33% when the doping concentration is reduced from 10^{20} to 10^{19} cm^{-3}, respectively.

3.2 VFTLP characteristics

A system-level ESD event is a typical power-on ESD event with a shorter rise time, a shorter discharge duration, and a higher current than its power-off counterpart.[18] As such, at the initial time, the voltage across the device rapidly increases to a peak, which is regarded as the overshoot phenomenon and may cause dielectric breakdown. However, the failure current in the vfTLP test will be higher than that in the TLP test owing to the lower energy contained in each pulse. The vfTLP pulses used in the simulations have a 0.1 ns rise time and a 5 ns pulse width. Simulation results are shown in Fig. 5; it can be seen that the failure current is 3 mA/μm.

The drain voltages of TFETs in vfTLP simulations with different physical models are shown in Fig. 6. It is observed that the overshoot phenomenon is not significant when the BTBT model is employed. This can be attributed to the BTBT-assisted triggering mechanism of the TFET; the BTBT provides the initial carriers for avalanche breakdown, making the device more easily triggered. It can also be observed from Fig. 6 that the overshoot voltage becomes much higher without the BTBT model. Another reason for this is that the device used in the simulation is small, resulting in a high electric field near the p–n junction under ESD stress. Generally, the

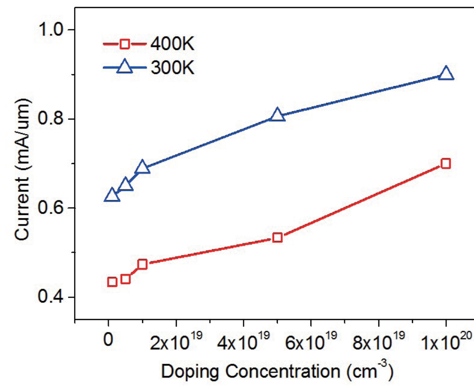


Fig. 4. (Color online) Failure currents of TFETs with various drain doping concentrations under positive stress at different ambient temperatures.

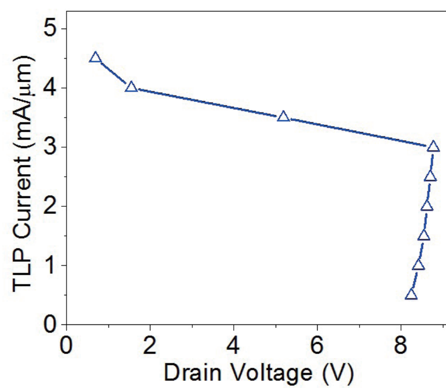


Fig. 5. (Color online) VfTLP *I*–*V* curve of TFET under positive stress.

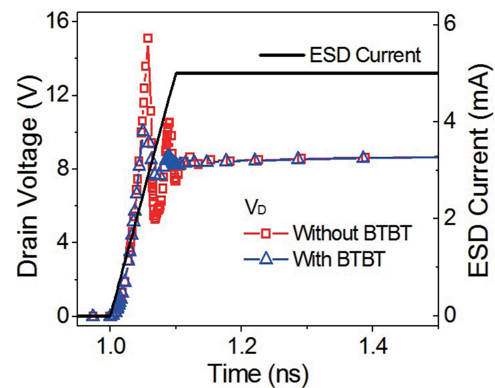


Fig. 6. (Color online) Drain voltages of TFETs in positive vfTLP simulations (current: 0.5 mA/μm).

voltage overshoot phenomenon is significant when the device is large or the p–n junction where avalanche generation first occurs is lightly doped.

During system-level ESD events, the heat cannot efficiently spread to the substrate region, resulting in the significant nonuniformity of the lattice temperature distribution and a reduction in failure current. This is because each system-level ESD event has a high current amplitude and a short discharge duration, meaning that a large amount of Joule heat will be generated in a short time. In addition, the thermal time constants of nanoscale devices are usually on the order of 10 ns, whereas most of the current should be discharged during the first 10 ns.(19) Figure 7 shows contour plots of the lattice temperature in TLP and vfTLP simulations. It can be seen that with a short but high-level current pulse (vfTLP), the temperature in the channel and drain regions is significantly higher than that in other regions. In most of the substrate region, the temperature hardly increases, indicating that the heat cannot be efficiently dissipated through this region. In this comparison, the current amplitude used for vfTLP simulation is higher than that used for TLP simulation. This is because system-level ESD events, which are mimicked in the vfTLP simulation, usually have much higher current than power-off ESD events.

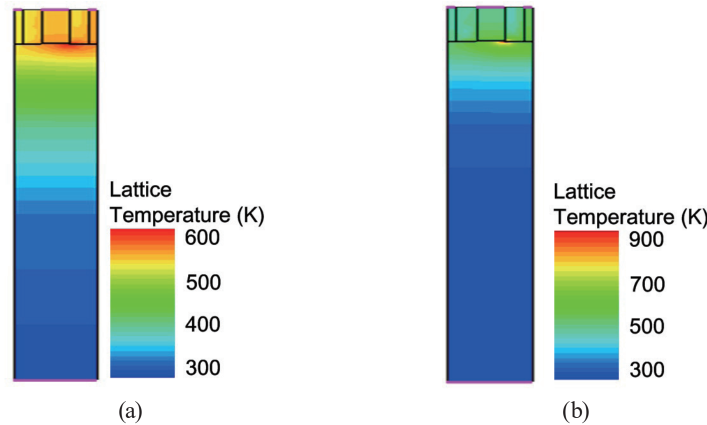


Fig. 7. (Color online) Lattice temperature distributions of TFET in (a) positive TLP simulation at 60 ns (current: 0.3 mA/μm) and (b) positive vfTLP simulations at 3 ns (current: 1 mA/μm) (not to scale).

3.3 Power surge

A power surge is a typical EOS event that has more charges and a longer discharge duration (generally over μs) order than an ESD event.[17] As mentioned above, the turn-on voltage of a TFET under positive stress is high and a large amount of Joule heat will be generated. Since an EOS event is much longer than an ESD event, the heat will accumulate in the device and the lattice temperature will easily reach the critical value, causing device failure. Thus, the robustness of a TFET under a positive EOS is very low.

In this work, we use TLP-like current pulses of 0.1 μs rise time and 1 μs pulse width to roughly evaluate the power surge robustness of a TFET. From Fig. 8, it can be seen that the failure current is 6 mA/μm, which is lower than that in an ESD event (11 mA/μm). However, the reduction in failure current is not proportional to the increase in pulse width. This is because an EOS event is much longer, allowing the heat to spread throughout the device, resulting in a more uniform temperature distribution as shown in Fig. 9. In contrast, in an ESD event, a hot spot exists in the channel region, resulting in earlier failure.

3.4 FDSOI configuration

FDSOI technology has some advantages such as a low power and a relatively low cost, but the low heat dissipation capability of the buried oxide (BOX) degrades the intrinsic ESD robustness. From Fig. 10, it can be seen that the triggering voltage of an FDSOI TFET is lower than that of a bulk TFET owing to better electrostatic control of the back gate. However, the failure current is 42% less than that of the bulk TFET owing to the existence of the BOX.

Generally, to increase the dissipation of heat through the substrate, the thickness of the BOX should be reduced. In addition, materials with better thermal properties, such as Al_2O_3 and SiC, may be used as the BOX and substrate materials to improve the heat dissipation.[20] The

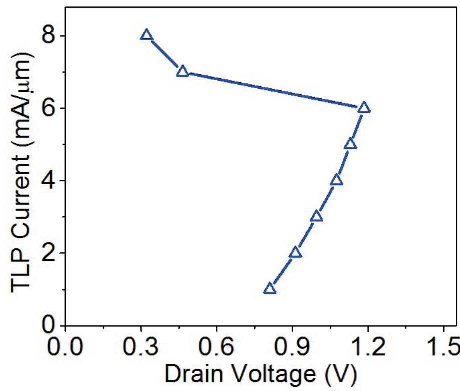


Fig. 8. (Color online) TLP-like I–V characteristics of TFET under negative EOS event.

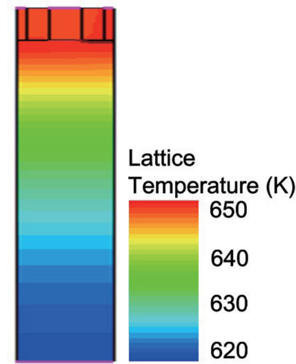


Fig. 9. (Color online) Lattice temperature distribution of TFET in negative EOS simulation at 0.6 μs (current: 4 mA/μm, not to scale).

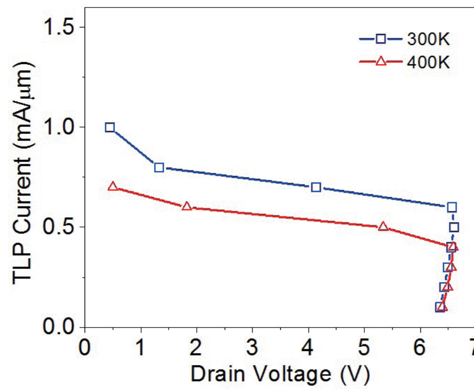


Fig. 10. (Color online) Positive TLP I–V curves of FDSOI TFET at different temperatures.

Table 1
Thermal properties used in simulations.

	SiO_2	Al_2O_3	Si (10 nm channel)	Si (substrate)	SiC
Thermal conductivity [W/(m·K)]	1.4	35	13	148	490
Heat capacity [J/(cm^3·K)]	1.61	2.89	1.63	1.63	2.22

thermal properties of these two materials and the traditional materials, which are used in the simulations, are listed in Table 1. It can be seen that both the thermal conductivity and heat capacity of Al_2O_3 and SiC are higher than those of the traditional counterparts. Figure 11 shows the temperature contour plots of TFETs with different materials in positive TLP simulations. It can be seen that more heat can spread to the substrate region when materials with superior thermal properties are used.

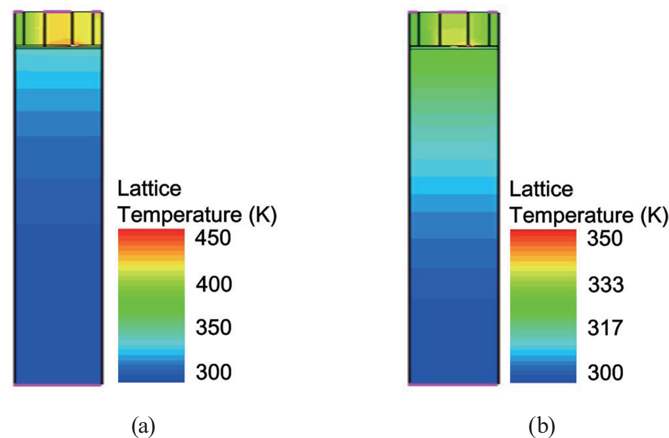


Fig. 11. (Color online) Lattice temperature distributions of TFETs with (a) SiO_2 BOX and silicon substrate, and (b) Al_2O_3 BOX and SiC substrate in positive TLP simulations at 60 ns (current: 0.5 mA/μm, not to scale).

4. Conclusions

In this work, the characteristics of TFETs under power-on ESD and EOS conditions were investigated. From the results of TCAD simulations, the following conclusions were drawn. Increasing the ambient temperature severely degrades the robustness of TFETs since the failure temperature is easily reached. The overshoot phenomenon is not significant in TFETs, mainly owing to the BTBT-assisted triggering mechanism. Because of the longer discharge duration and the greater amount of heat accumulation, the failure current under an EOS event is lower than that under an ESD event.

Acknowledgments

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