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Bridgeless Single-stage Step-down Power Factor Corrector under Synchronous Switching Control Scheme

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In this paper, a novel bridgeless power factor corrector (PFC) is proposed. The PFC can shape the waveform of the input current to be sinusoidal and in phase with the AC input voltage simply by sensing of the AC voltage, input current, and output voltage. That is, it is able to achieve a unity power factor. As compared with conventional PFCs, the proposed PFC possesses the particular features of high step-down voltage ratio, being bridgeless, galvanic isolation, and leakage energy recycling. All the active switches in the proposed PFC can be operated under an identical control signal. In addition, the output voltage can be regulated only by single-loop control, instead of dual- or multiloop control. Therefore, the control scheme for the PFC is simple and much easier to carry out. The operation principle, theoretical analysis, and hardware validation to verify the proposed PFC are described.

1. Introduction

Power-electronics-based devices have been applied in various fields from household appliances to industry equipment, and the total number of relevant products is increasing dramatically. Among them, converters to convert AC power to DC are widely required, especially for a low DC output voltage, such as for battery chargers, LED drivers, and computer power supplies.

AC-to-DC converters conventionally include a bridge rectifier and a huge filter capacitor. Similarly to the power-stage structure shown in Ref. 1, this configuration is simple, cheap, and without the need of an extra control circuit. Nonetheless, it may lead to serious harmonic distortion and results in a low power factor. Adding a current-shaping circuit at the input can not only improve the power factor but also reduce harmonic distortion. Nevertheless, power factor correctors (PFCs) are generally still based on a bridge configuration.[2–7] The efficiency is therefore rather low. Furthermore, if a PFC is a boost type, the output DC voltage will be higher than the input, even with the obvious advantage of a continuous input current. To deal with a low-voltage load, buck-type PFCs are options,[8–13] but the input current will be discontinuous and an active switch has to be driven on the high-voltage side. Therefore, a cascaded filter on the AC input side is necessary for achieving a better power factor.

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To obtain a continuous input current and lower the output voltage simultaneously, a two-stage PFC has been considered.[14–20] However, the requirement of more components and the associated lower efficiency are both its main drawbacks. This paper proposed a bridgeless single-stage step-down PFC (BSSPFC) with the feature of galvanic isolation to overcome the aforementioned problems. A high-frequency transformer is incorporated to feature galvanic isolation, the core material of which is Mn–Zn ferrite. All the active switches in the BSSPFC can be controlled simply by synchronous driving, which simplifies the control mechanism. In addition, the BSSPFC is capable of stepping down the input voltage significantly and improving the converter efficiency effectively. The volume of the AC input filter can also be reduced while operating in continuous conduction mode (CCM).

2. Main Structure and Steady-state Analysis

The structure of the proposed BSSPFC is shown in Fig. 1, which is derived from the integration of a single-ended primary-inductor converter (SEPIC) and a flyback converter. The frond-end of the BSSPFC can be regarded as a modified bridgeless SEPIC in charge of performing power factor correction, and the downstream is a flyback-based configuration for achieving a higher step-down voltage ratio and galvanic isolation. The output power of the BSSPFC can be raised when the current of the input inductor L_{in} is in CCM. In CCM, the current stress of active switches can be alleviated and the size of the EMC/EMI filter is also reduced. In this section, the operation principle and voltage gain will be discussed, where the following assumptions are made.

1) All capacitors are large enough to guarantee that the voltages across C_1, C_2, and C_o can be regarded as constant.
2) Semiconductor devices such as diodes and switches are ideal.
3) The turn ratio n is equal to N_2/N_1.
4) The duty ratio of the converter is D.
5) The switching period is defined as T.

2.1 Operation principle

The operation of the BSSPFC can mainly be divided into three modes over one switching cycle. Figure 2 depicts the conceptual key waveforms, which are the control signal and current

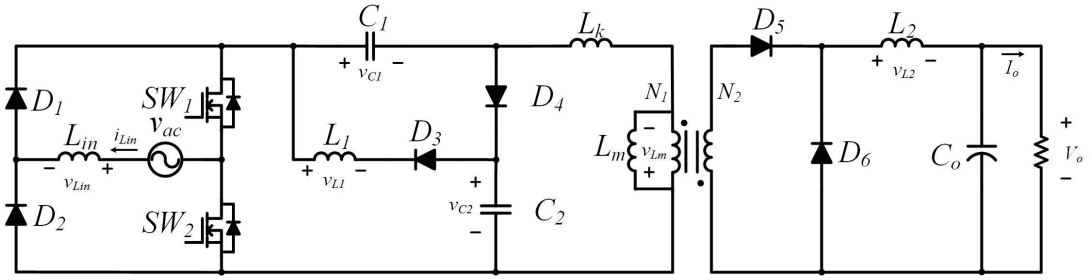


Fig. 1. Power stage of the proposed BSSPFC.

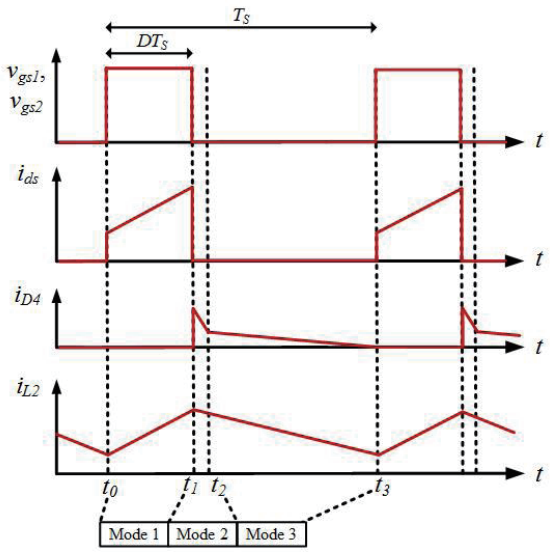


Fig. 2. (Color online) Conceptual key waveforms of the proposed converter.

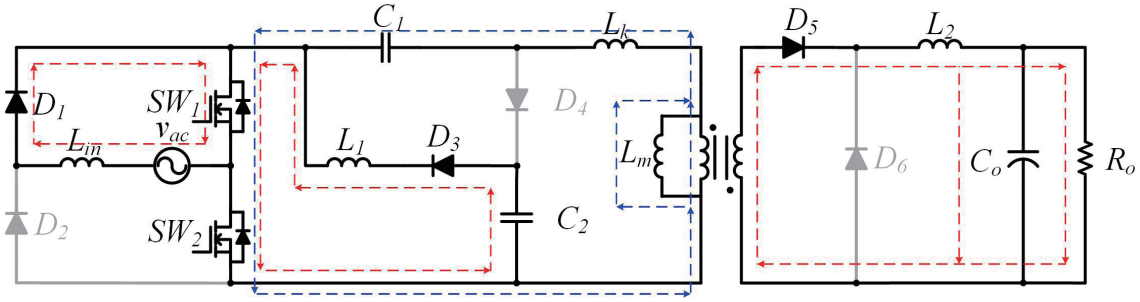


Fig. 3. (Color online) Equivalent circuit of the proposed BSSPFC in Mode 1.

of switch SW_1, the current of diode D_4, and the current of inductor L_2. This figure has been included to aid understanding of the converter operation. The converter operation is discussed mode by mode in the following.

Mode 1 [t_0–t_1] (Fig. 3): At the beginning of Mode 1, switches SW_1 and SW_2 are turned on simultaneously and diodes D_3 and D_5 are in the ON-state. Inductor L_{in} is magnetized by v_{ac} and inductor L_1 is charged by capacitor C_2. Capacitor C_1 transmits its stored energy to inductor L_2 through the transformer. Meanwhile, L_m and L_k absorb energy from capacitor C_1.

Mode 2 [t_1–t_2] (Fig. 4): In mode 2, switches SW_1 and SW_2 are both in the OFF-state and therefore diodes D_3, D_4, and D_6 are forward biased. Inductor L_{in} releases energy to capacitors C_1 and C_2. At the same time, capacitor C_2 also draws energy from L_m and L_k. Mode 2 ends when the two currents flowing through inductors L_m and L_k drop to zero.

Mode 3 [t_2–t_3] (Fig. 5): After L_m and L_k fully discharge their stored energy, the operation mode of the BSSPFC enters Mode 3. During this mode, the circuit condition is the same as that in Mode 2 except for inductors L_m and L_k. Mode 3 continues until the active switches are turned on again and then the converter operation over one switching cycle is completed.

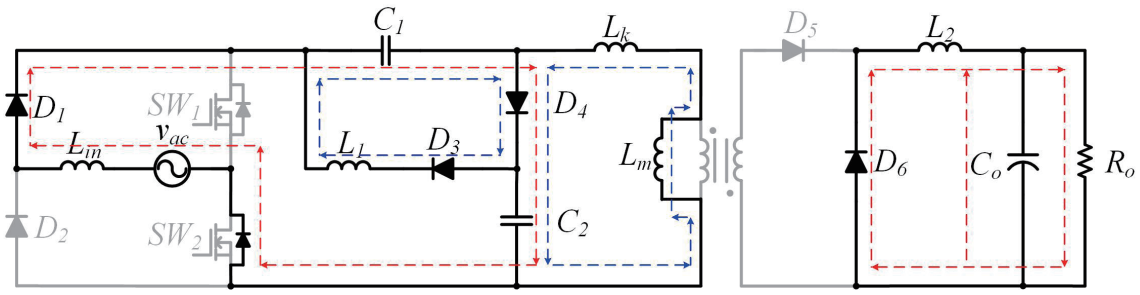


Fig. 4. (Color online) Equivalent circuit of the proposed BSSPFC in Mode 2.

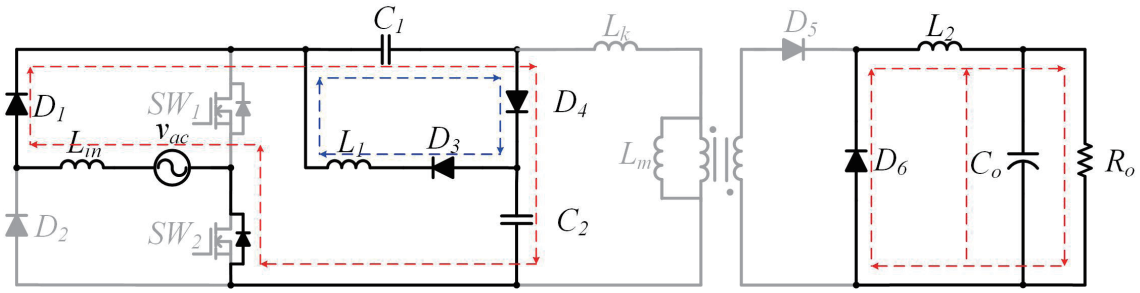


Fig. 5. (Color online) Equivalent circuit of the proposed BSSPFC in Mode 3.

2.2 Voltage gain derivation

The following is the voltage gain derivation of the proposed BSSPFC. Voltage polarity and current direction definitions are shown in Fig. 1. Applying the volt-second balance criterion to inductors L_{in}, L_1, and L_2 and finding the voltage across the capacitor C_1 are the key points of this theoretical derivation.

1) Volt-second balance on L_{in}

When SW_1 is closed ($0 \le t \le DT$), the voltage across input inductor L_{in} is equal to the input source, that is,

$$v_{Lin} = v_{ac}. \tag{1}$$

According to Eq. (1), the variation of the inductor current $(\Delta i_{Lin})_{on}$ during the ON-state interval is

$$\left(\Delta i_{Lin}\right)_{on} = v_{ac} DT. \tag{2}$$

When SW_1 is OFF ($DT \le t \le T$), input inductor L_{in} will charge capacitors C_1 and C_2. Therefore,

$$v_{Lin} = v_{ac} - v_{C1} - v_{C2}\,. \tag{3}$$

From Eq. (3), the variation of the inductor current $(\Delta i_{Lin})_{off}$ over the OFF-time interval can be estimated as

$$\left(\Delta i_{Lin}\right)_{off} = (v_{ac} - v_{C1} - v_{C2})(1-D)T. \tag{4}$$

Under a steady-state condition, the current increment and decrease on inductor L_{in}, $(\Delta i_{Lin})_{on}$ and $(\Delta i_{Lin})_{off}$, respectively, will be identical. Therefore,

$$\left(\Delta i_{Lin}\right)_{on} + \left(\Delta i_{Lin}\right)_{off} = v_{ac}DT + (v_{ac} - v_{C1} - v_{C2})(1-D)T = 0. \tag{5}$$

Solving Eq. (5) yields

$$v_{ac} = (v_{C1} + v_{C2})(1-D). \tag{6}$$

2) Volt-second balance on L_1

When SW_1 is conducted ($0 \le t \le DT$), capacitor C_2 will be in parallel with inductor L_1. That is,

$$v_{L1} = -v_{C2}. \tag{7}$$

According to Eq. (7), the current increment on the inductor, $(\Delta i_{L1})_{on}$, during this time period is

$$\left(\Delta i_{L1}\right)_{on} = -v_{C2}DT. \tag{8}$$

When switch SW_1 is open during the time period $DT \le t \le (1 - D)T$, inductor L_1 provides energy to C_1 and thus,

$$v_{L1} = v_{C1}. \tag{9}$$

From Eq. (9), the inductor current drop, $(\Delta i_{L1})_{off}$, during this time period can be calculated as

$$\left(\Delta i_{L1}\right)_{off} = v_{C1}(1-D)T. \tag{10}$$

Based on the volt-second balance, the net change of the inductor current has to be zero. Accordingly,

$$\left(\Delta i_{L1}\right)_{on} + \left(\Delta i_{L1}\right)_{off} = -v_{C2}DT + v_{C1}(1-D)T = 0. \tag{11}$$

After solving Eq. (11), the relationship between v_{C1} and v_{C2} can be expressed as

$$v_{C1} = \frac{D}{1-D} v_{C2}. \tag{12}$$

3) Volt-second balance on L_2

When SW_1 is ON, the voltage across inductor L_2 will be

$$v_{L2} = nv_{C1} - V_o. \tag{13}$$

According to Eq. (13), the variation of the inductor current $(\Delta i_{L2})_{on}$ during this ON-state period can be expressed as

$$\left(\Delta i_{L2}\right)_{on} = (nv_{C1} - V_o)DT. \tag{14}$$

When the switch is open, inductor L_2 will provide energy to C_o and the voltage of L_2 is equal to V_o.

$$v_{L2} = V_o \tag{15}$$

Thus, the current drop on the inductor current, $(\Delta i_{L2})_{off}$, is computed as

$$\left(\Delta i_{L2}\right)_{off} = -V_o(1-D)T. \tag{16}$$

In steady-state operation, the magnitudes of $(\Delta i_{L2})_{on}$ and $(\Delta i_{L2})_{off}$ will be identical and the following relationship holds:

$$\left(\Delta i_{L2}\right)_{on} + \left(\Delta i_{L2}\right)_{off} = n(v_{C1} - V_o)DT - V_o(1-D)T = 0. \tag{17}$$

Solving Eq. (17), one can obtain

$$V_o = nDv_{C1}. \tag{18}$$

4) Capacitor voltage and converter gain

Substituting Eq. (18) into Eq. (6) gives the voltage across capacitor C_1:

$$v_{C1} = v_{ac}. \tag{19}$$

Likewise, the voltage across capacitor C_2 can be obtained by substituting Eq. (12) into Eq. (18). Accordingly,

$$v_{C2} = \frac{D}{1-D} v_{ac}. \tag{20}$$

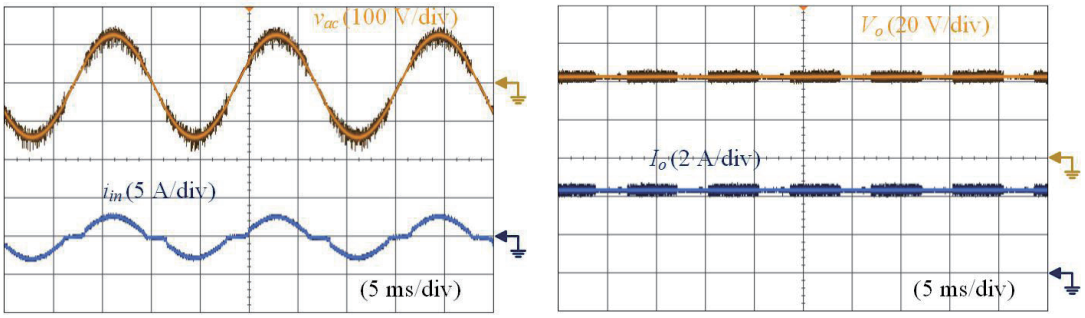
Capacitor C_2 is irrelevant to the voltage gain and only performs energy recycling for leakage inductance and magnetizing inductance. According to Eqs. (18) and (19), the voltage gain of the BSSPFC is determined as

$$V_o = nDv_{ac}. \tag{21}$$

In addition, there are two active switches in the proposed circuit. The voltage stresses of the two switches are identical and are the series voltages across capacitors C_1 and C_2. That is, SW_{stress} equals $v_{C1} + v_{C2}$.

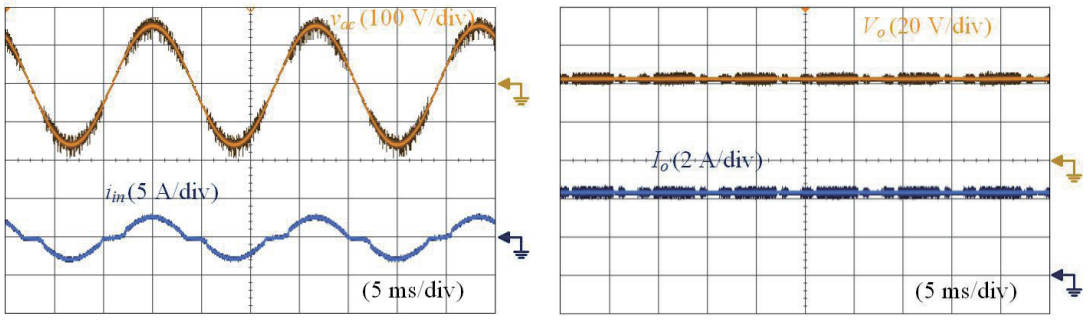
3. Experimental Results and Discussion

To verify the feasibility of the proposed structure, a 200 W prototype dealing with a universal-line input is built, tested, and measured. Figure 6 shows the waveforms of input voltage v_{ac} and current i_{Lin}, when the AC mains is 90 V_{rms}. As shown in Fig. 6(a), the input current is purely sinusoidal and in phase with the AC mains voltage. Figure 6(b) shows the measured output voltage and current, which indicate that a near ripple-free feature can be achieved at the DC output. Figures 7(a) and 7(b) show the voltages and currents of the input



(a) (b)

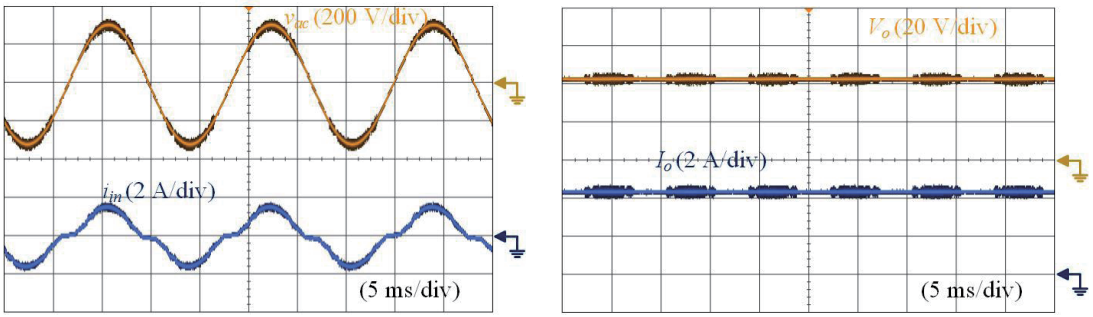
Fig. 6. (Color online) Measured waveforms when AC mains is 90 V_{rms}. (a) Input voltage v_{ac} and input current i_{Lin}. (b) Output voltage V_o and output current I_o.



(a) (b)

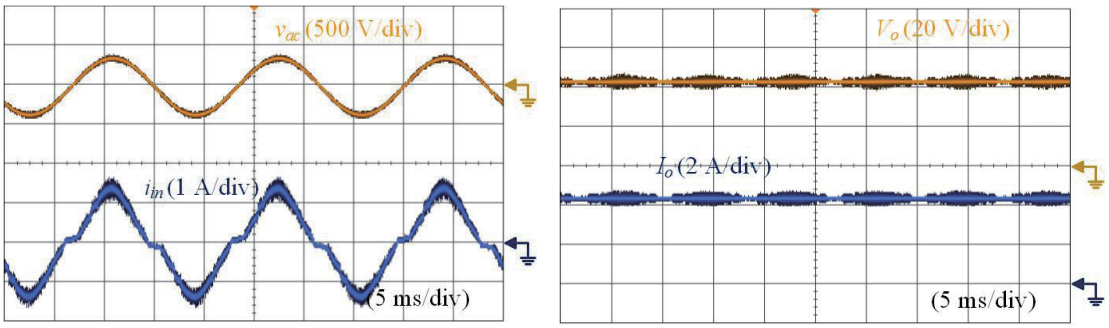
Fig. 7. (Color online) Measured waveforms when AC mains is 110 V_{rms}. (a) Input voltage v_{ac} and input current i_{Lin}. (b) Output voltage V_o and output current I_o.

and output, respectively, when the AC mains voltage increases to 110 V_{rms}. From Fig. 7, a high input power factor and near ripple-free feature are still accomplished. Figures 8 and 9 show the practical measurements performed at inputs of 220 and 264 V_{rms}, respectively, both of which reveal that high performance can also be achieved by the proposed BSSPFC. Figure 10 is the transient response when the output power is stepped up from half load to full load. For the case of 220 V_{rms} input and 200 W power rating, the measured result for SW_1 is shown in Fig. 11.



(a) (b)

Fig. 8. (Color online) Measured waveforms when AC mains is 220 V_{rms}. (a) Input voltage v_{ac} and input current i_{Lin}. (b) Output voltage V_o and output current I_o.



(a) (b)

Fig. 9. (Color online) Measured waveforms when AC mains is 264 V_{rms}. (a) Input voltage v_{ac} and input current i_{Lin}. (b) Output voltage V_o and output current I_o.

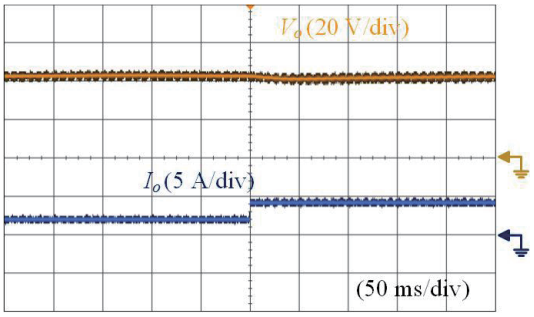


Fig. 10. (Color online) Measured output voltage and current at step change under load.

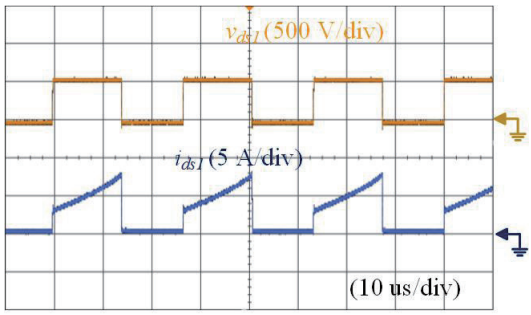


Fig. 11. (Color online) Measured drain-to-source voltage and current of switch SW_1.

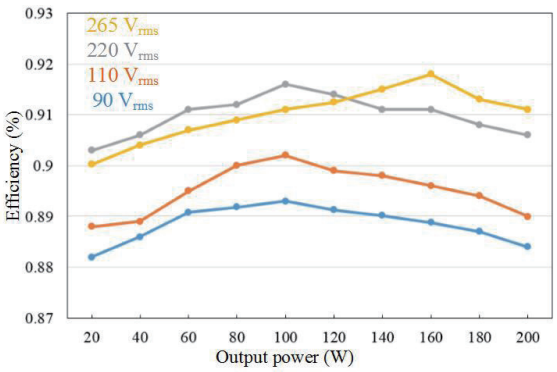


Fig. 12. (Color online) Measured efficiency from light load to full load under different line voltages.

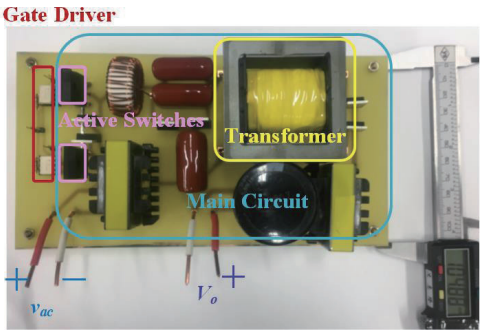


Fig. 13. (Color online) Photo of the prototype of proposed BSSPFC.

From the measured waveform, it is found that the active switch is free from spikes. Figure 12 depicts the measured efficiency of the prototype under different input voltages, which reveals that the peak efficiency is up to 91.8% at 264 V_{rms} line voltage. Figure 12 also reveals that when the input voltage is higher, the current in the entire power stage is lower. Accordingly, conduction loss therefore drops and efficiency is raised. In addition, a photo of the prototype BSSPFC is shown in Fig. 13.

4. Conclusions

A high step-down bridgeless PFC is proposed, which possesses the following advantages: fewer rectifying diodes, a single power stage, galvanic isolation, active switches in synchronous control, universal-line input from 90 to 264 V_{rms}, and a simple control mechanism. The BSSPFC can accommodate universal-line input, and moreover, even at a high input voltage, a high power factor and near ripple-free output can still be obtained. Since fewer components are used, the cost can accordingly be lowered and conversion efficiency is improved. To verify the feasibility of the BSSPFC, hardware measurements from a 200 W prototype are carried out. The experimental results demonstrate the characteristics of the BSSPFC, and the average efficiency achieved is up to 90.08%.

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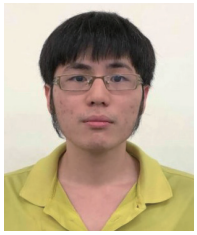

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