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Isolated Single-ended Primary-inductive Converter with a Soft-switching Cell for Implementing Features of Zero-voltage Switching and Zero-current Switching

Cheng-Tao Tsai* and Jyun-Mao Chen

Department of Electrical Engineering, National Chin-Yi University of Technology, Taichung 41170, Taiwan

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Keywords: isolated single-ended primary-inductive converter (ISEPIC), zero-voltage switching (ZVS), zero-current switching (ZCS)

In this paper, an isolated single-ended primary-inductive converter (ISEPIC) with a soft-switching cell for implementing features of zero-voltage switching (ZVS) and zero-current switching (ZCS) is proposed. The ISEPIC has the following advantages: (1) By changing the inductor element of the ISEPIC into a transformer element, the features of electrical isolation can be achieved. (2) By incorporating a soft-switching cell, the power switches (MOSFETs) of the ISEPIC can achieve ZVS and ZCS features during turn-on conditions. Therefore, the power losses of the power switches can be reduced during the turn-on transient, and the overall efficiency of the ISEPIC can be increased significantly. Finally, a prototype of the ISEPIC with a soft-switching cell is built. Experimental results are presented to verify the performance and feasibility of the proposed ISEPIC for implementing features of ZVS and ZCS.

1. Introduction

A number of nonisolated switching power converters have been developed and proposed.[1] For example, Buck, Boost, Cuk, single-ended primary-inductive converter (SEPIC), and Zeta converters have attracted interest, which have simple structures and are widely used at low and medium powers. A nonisolated SEPIC is often adopted for step-down and step-up voltage applications, as shown in Fig. 1. However, the hard-switching conditions of the active switch (MOSFET) are a major contributor to switching losses in a nonisolated SEPIC, resulting in high power losses, high electromagnetic interference (EMI), and low conversion efficiency. To overcome these problems, a number of soft-switching techniques have been proposed.[2–5] Soft-switching techniques improve the imperfect switching of power switches and thereby eliminate switching losses and EMI. Several soft-switching techniques have been developed in recent years. The soft-switching techniques can be divided into zero-voltage-switching (ZVS) and zero-current-switching (ZCS) techniques.[6–10] Both techniques drive the voltage or current of the active switch to zero before any switching action, and avoid a concurrent high voltage and

*Corresponding author: e-mail: cttsai@ncut.edu.tw
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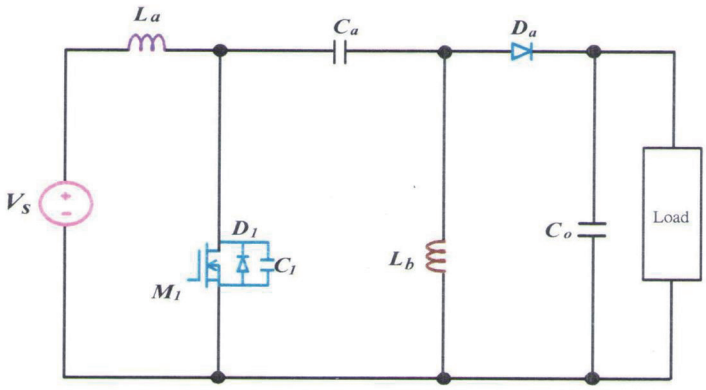

Fig. 1. (Color online) Topology of a nonisolated SPEIC.

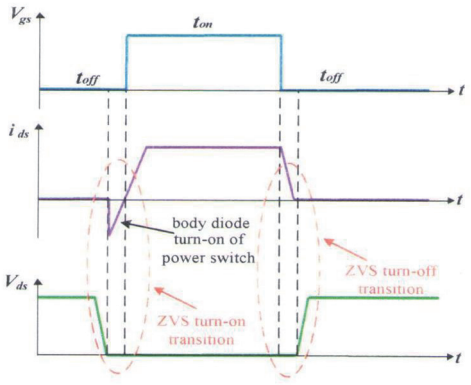

Fig. 2. (Color online) Illustration of ZVS turn-on and turn-off conditions.

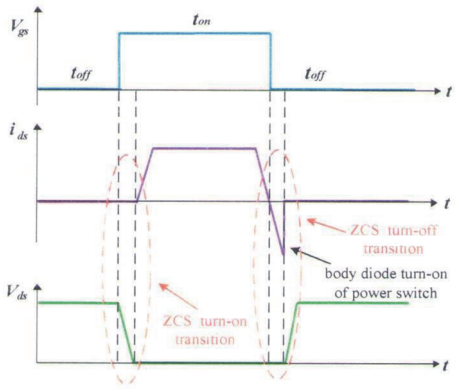

Fig. 3. (Color online) Illustration of ZCS turn-on and turn-off conditions.

high current in the switching transition. A SEPIC with ZVS and ZCS techniques will have no voltage and no current across the power switch at turn-on and turn-off transitions, as illustrated in Figs. 2 and 3, respectively.

In this paper, an isolated single-ended primary-inductive converter (ISEPIC) with a soft-switching cell for implementing features of ZVS and ZCS is presented, as shown in Fig. 4. The soft-switching cell has a simple structure, which consists of a transformer (T_1) and an auxiliary switch (M_2) to implement the ZVS feature of the main switch (M_1) and the ZCS feature of M_2. The operational principles of the proposed ISEPIC are described in Sect. 2. Experimental results obtained from a prototype of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS are presented in Sect. 3. Finally, a conclusion is given in Sect. 4.

2. Operational Principles

As shown in Fig. 4, the proposed ISEPIC with features of ZVS and ZCS consists of a SEPIC and a soft-switching cell. The soft-switching cell is composed of an isolated transformer (T_{r1}),

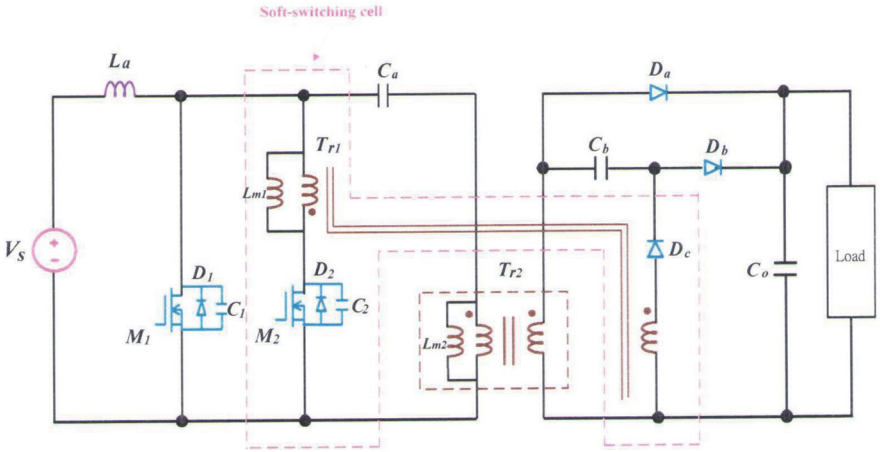

Fig. 4. (Color online) Topology of ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS.

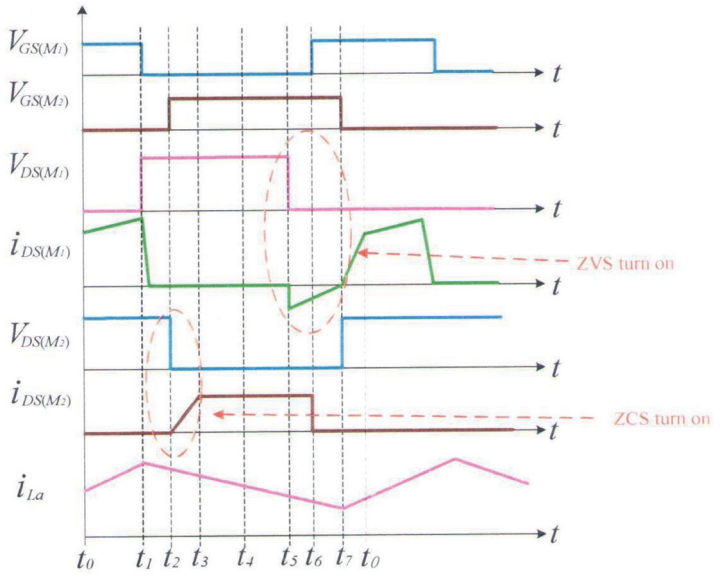

Fig. 5. (Color online) Current and voltage waveforms of the key components and the driving signals of switches (M_1 and M_2) for proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS.

M_2, and a power diode (D_c) to create a ZVS condition for M_1 and a ZCS condition for the auxiliary switch M_2. The operational principles of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS over one switching cycle can be divided into eight major operating modes. Figure 5 shows the current and voltage waveforms of the key components and the driving signals of the switches (M_1 and M_2). Figure 6 shows the equivalent circuits of the proposed ISEPIC. To simplify the description of the operational modes, the following assumptions are made:

(1) To analyze the ZVS feature, the body diode (D_1) and parasitic capacitor (C_1) of M_1 will be considered in the steady-state operation of the circuit.

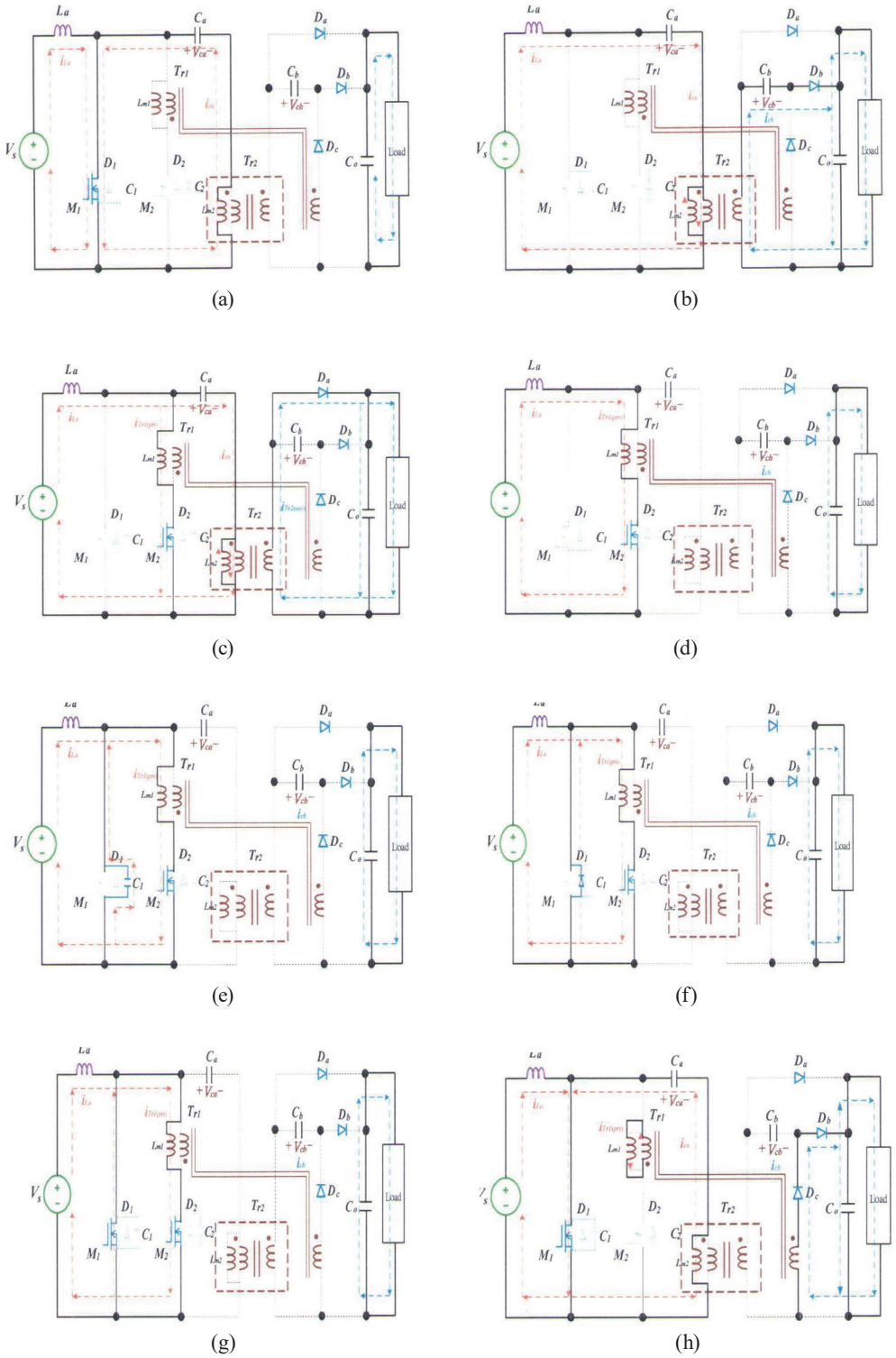

Fig. 6. (Color online) Equivalent circuits of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, and (h) Mode 8.

(2) The output filter capacitor (C_o) is large enough for the voltage across it to be constant over a switching cycle.

Mode 1 [Fig. 6(a), $t_0 < t < t_1$]:

At time t_0, M_1 is turned on, and M_2 is turned off. The inductor current i_{La} flowing through the path $V_s \rightarrow L_f \rightarrow M_1 \rightarrow V_s$ is linearly increased, where V_s is an input source and L_f is a storage inductor. During this interval, the capacitor (C_a) begins discharging. The current i_{ca} of C_a is flowing through the path $C_a \rightarrow M_1 \rightarrow T_{r2} \rightarrow C_a$. At this time, the magnetic inductance current of the transformer (T_{r2}) is linearly increased. In the output terminal, the diodes (D_a, D_b, and D_c) are turned off and the filter capacitor (C_2) delivers power to the output load. The inductor current i_{La} can be expressed as

$$i_{La}(t) = \frac{V_s}{L_a}(t - t_0). \tag{1}$$

The equivalent circuit is shown in Fig. 6(a).

Mode 2 [Fig. 6(b), $t_1 < t < t_2$]:

At time t_1, M_1 is turned off, and M_2 remains off. The inductor current i_{La} flowing through the path $V_s \rightarrow$the main inducter (L_a)$\rightarrow C_a \rightarrow T_{r2} \rightarrow V_s$ is linearly decreased. On the primary side of T_{r2}, the magnetizing current i_{ca} is transferred to the secondary side to discharge C_b. At this time, D_b is turned on by a forward bias, and D_a and D_c are turned off. The secondary current i_{cb} of T_{r2} flows through the path $T_{r2} \rightarrow C_b \rightarrow D_b \rightarrow Load \rightarrow T_{r2}$. i_{La} can be expressed as

$$i_{La}(t) = \frac{V_{ca} + V_{Tr2} - V_s}{L_a}(t - t_1). \tag{2}$$

The equivalent circuit is shown in Fig. 6(b).

Mode 3 [Fig. 6(c), $t_2 < t < t_3$]:

At time t_2, M_1 remains off and M_2 is turned on. Because the limiting current of the magnetizing inductance (L_{m1}) of T_{r1} increases instantaneously, M_2 has a feature of ZCS in the conduction transient state. At this time, the main inductor current i_{La} is divided and flows through two paths: $V_s \rightarrow L_a \rightarrow C_a \rightarrow T_{r2} \rightarrow V_s$ and $V_s \rightarrow L_a \rightarrow T_{r1} \rightarrow M_1 \rightarrow V_s$. At this time, the magnetizing inductance current of T_{r1} is linearly increased. At the output end, because the voltage of C_b is discharged to zero, D_a is turned on by a forward bias, and the secondary current i_{cb} of T_{r2} flows through the path $T_{r2} \rightarrow D_a \rightarrow Load \rightarrow T_{r2}$. i_{La} can be expressed as

$$i_{La}(t) = i_{Tr1} + i_{ca} = \frac{V_{Tr1}}{L_{m1}}(t - t_2) + \frac{(V_{ca} - V_{La} - V_s)}{L_{m2}}(t - t_2). \tag{3}$$

The equivalent circuit is shown in Fig. 6(c).

Mode 4 [Fig. 6(d), $t_3 < t < t_4$]:

At time t_3, M_2 continues to be turned on, and M_1 remains turned off. When the main inductor current i_{La} is equal to the magnetizing inductor current i_{Tr1} of T_{r1}, the current flowing

through C_a drops to zero. At this time, D_a, D_b, and D_c at the output end are turned off by a reverse bias, and the current required by the load is provided by C_o. i_{La} can be expressed as

$$i_{La}(t) = \frac{(V_{La} + V_s)}{L_{m1}}(t - t_3). \tag{4}$$

The equivalent circuit is shown in Fig. 6(d).

Mode 5 [Fig. 6(e), $t_4 < t < t_5$]:

At time t_4, M_2 remains on and M_1 remains off. The main inductor current i_{La} continues to decrease linearly, while the magnetizing inductor current i_{Tr1} of T_{r1} continues to increase linearly. When the main inductor current i_{La} is smaller than the magnetizing inductance current i_{Tr1} of T_{r1}, the magnetizing inductance current i_{Tr1} of T_{r1} is divided and flows through two paths: $V_s \rightarrow L_a \rightarrow T_{r1} \rightarrow M_2 \rightarrow V_s$ and $T_{r1} \rightarrow M_2 \rightarrow C_1 \rightarrow T_{r1}$. C_1 of M_1 starts to be discharged. At this time, D_a, D_b, and D_c at the output end continue to be reversely biased and cut off, and the current required by the load continues to be provided by C_o. i_{La} can be expressed as

$$i_{La}(t) = i_{Tr1}(t - t_4) - i_{M1}(t - t_4). \tag{5}$$

The equivalent circuit is shown in Fig. 6(e).

Mode 6 [Fig. 6(f), $t_5 < t < t_6$]:

At time t_5, M_2 continues to be turned on. When the voltage of C_1 of M_1 is discharged to zero, D_1 of M_1 is turned on, providing a zero-voltage conduction characteristic of M_1. The magnetizing inductance current i_{Tr1} of T_{r1} continues to be divided and flow through two paths: $V_s \rightarrow L_a \rightarrow T_{r1} \rightarrow M_2 \rightarrow V_s$ and $T_{r1} \rightarrow M_2 \rightarrow D_1 \rightarrow T_{r1}$. At this time, D_a, D_b, and D_c at the output end continue to be reversely biased and cut off, and the current required by the load continues to be provided by C_o. i_{La} can be expressed as

$$i_{La}(t) = i_{Tr1}(t - t_5) - i_{M1}(t - t_5). \tag{6}$$

The equivalent circuit is shown in Fig. 6(f).

Mode 7 [Fig. 6(g), $t_6 < t < t_7$]:

At time t_6, M_1 is turned on by ZVS, and M_2 continues to be turned on. The current i_{La} of L_a starts to increase linearly, while the current flowing through M_1 and T_{r1} starts to decrease linearly. At this time, D_a, D_b, and D_c at the output end continue to be reversely biased and cut off, and the current required by the load continues to be provided by C_o. i_{La} can be expressed as

$$i_{La}(t) = i_{Tr1}(t - t_6) - i_{M1}(t - t_6). \tag{7}$$

The equivalent circuit is shown in Fig. 6(g).

Mode 8 [Fig. 6(h), $t_7 < t < t_8$]:

At time t_7, M_1 continues to be turned on, and M_2 is turned off. The current i_{La} of L_a flows through the path $V_s \rightarrow L_a \rightarrow M_1 \rightarrow V_s$, and the main inductor current i_{La} is linearly increased. At the same time, C_a starts to discharge, C_a current i_{ca} flows through the path $C_a \rightarrow M_1 \rightarrow T_{r2} \rightarrow C_a$, and the magnetizing inductance current of T_{r2} is linearly increased. On the primary side of T_{r1}, the magnetizing current $i_{Tr1(pri)}$ is transferred to the secondary side, and then D_b and D_c are turned on by a forward bias. The secondary current $i_{Tr1(sec)}$ of T_{r2} flows through the path $T_{r1} \rightarrow D_c \rightarrow D_b \rightarrow Load \rightarrow T_{r1}$. i_{La} can be expressed as

$$i_{La}(t) = i_{Tr1}(t - t_7) - i_{M1}(t - t_7). \tag{8}$$

The operational mode of the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS over one switching cycle is completed. The equivalent circuit is shown in Fig. 6(h).

3. Experimental Results

To verify the feasibility of the ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS, a 120 W prototype is built. The specifications of the ISEPIC are listed as follows:

- input voltage: V_s = 50 V_{dc},
- output voltage: V_{01} = 120 V_{dc},
- output current: I_{01} = 1 A,
- total output power: 120 W,
- switching frequency: f = 40 kHz.

Figure 7 shows the experimental signal waveforms of M_1 and M_2 at an operating frequency of 40 kHz. Figure 8 shows the experimental voltage and current waveforms of M_1, from

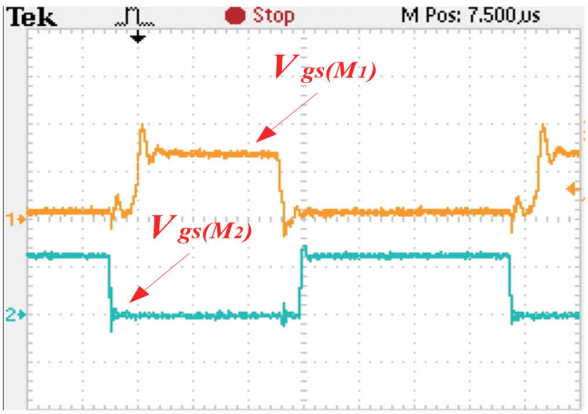

Fig. 7. (Color online) Driving signal waveforms of M_1 and M_2. ($V_{gs(M1)}$: 5 V/div, $V_{gs(M2)}$: 5 V/div, time: 5 µs/div)

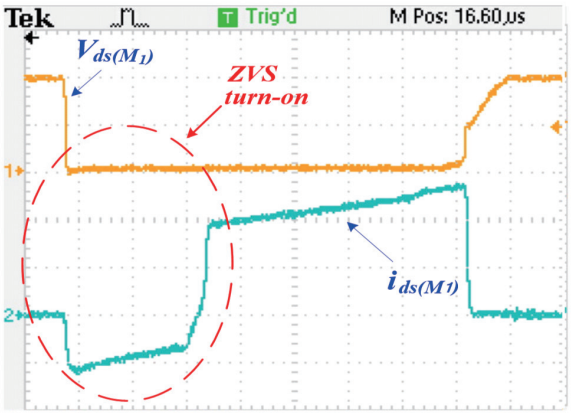

Fig. 8. (Color online) Voltage and current waveforms of M_1. ($V_{ds(M1)}$: 50 V/div, $i_{ds(M1)}$: 1 A/div, time: 5 µs/div)

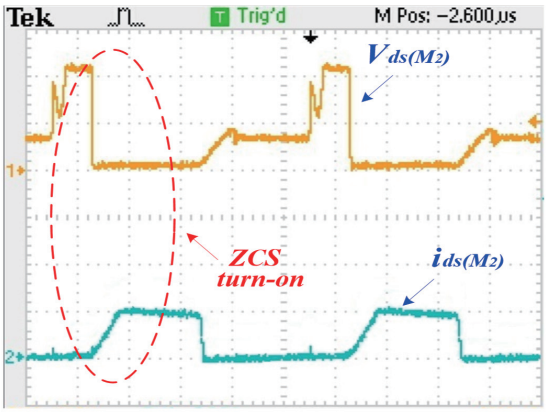

Fig. 9. (Color online) Voltage and current waveforms of M_2. ($V_{ds(M1)}$: 50 V/div, $i_{ds(M1)}$: 1 A/div, time: 5 µs/div)

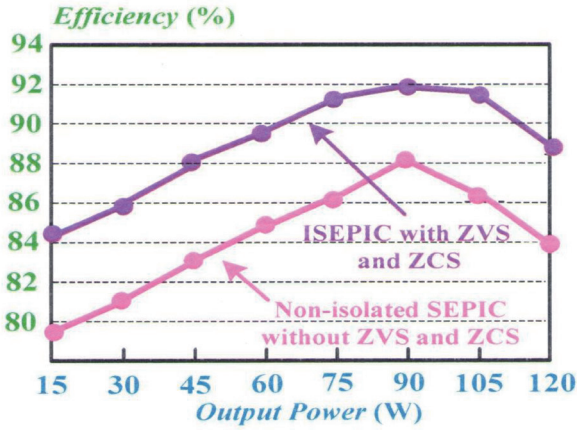

Fig. 10. (Color online) Plots of efficiency versus output current for the ISEPIC and the nonisolated SEPIC at output power of 120 W.

which it can be seen that M_1 has a ZVS feature at the turn-on transition. Figure 9 shows the experimental voltage and current waveforms of M_2, from which it can be seen that M_2 has a ZCS feature at the turn-on transition. Figure 10 shows the efficiency measurements of the ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS, from which it can be seen that the maximum efficiency can reach as high as 92%, about 4% higher than that of the nonisolated SEPIC (as shown in Fig. 1). The reason for the higher efficiency is that M_1 of the nonisolated SEPIC is still operated in a hard-switching manner during the turn-on and turn-off transitions.

4. Conclusions

In this study, the proposed ISEPIC with a soft-switching cell for implementing features of ZVS and ZCS has been built and implemented. It uses a soft-switching cell to implement the features of ZVS and ZCS under turn-on transitions for M_1 and M_2. Therefore, the power losses of the power switches can be reduced during the turn-on transient, and the overall efficiency of the ISEPIC can be increased significantly. The experimental results have verified that the proposed ISEPIC with a soft-switching cell is relatively suitable for the high-frequency requirements of power supplies.

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Author Contributions

All of the authors contributed to publishing this paper. Cheng-Tao Tsai wrote the paper, and Jyun-Mao Chen contributed to the experimental results of the circuit.

Conflicts of Interest

The authors declare that there are no conflicts of interest, regarding the publication of this paper.

References

1 H. M. Sizkoohi, J. Milimonfared, M. Taheri, and S. Salehi: IET Trans. Power Electron. **8** (2015) 1786. https://doi.org/10.1016/j.apenergy.2016.12.094.
2 C. T. Tsai, J. C. Su, and S. R. Wei: Sens. Mater. **31** (2019) 327. https://doi.org/10.18494/SAM.2019.2086
3 A. A. Tropina, L. Lenarduzzi, S. V. Marasov, and A. P. Kuzmenko: IEEE Trans. Plasma Sci. **37** (2009) 2286. https://doi.org/10.1109/TPS.2009.2029692
4 H. Wang, H. S. Chung, and A. Ioinovici: IEEE Trans. Power Electron. **27** (2012) 2242. https://doi.org/10.1109/TPEL.2011.2173588
5 G. S. Peter Castle, I. I. Inculet, and K. I. Burgess: IEEE Trans. Ind. Gen. Appl. **5** (1969) 489. https://doi.org/10.1109/TIGA.1969.4181060
6 K. J. Boelter and J. H. Davidson: Aerosol Sci. Technol. **27** (1997) 689. https://doi.org/10.1080/02786829708965505
7 P. A. Lawless: Aerosol Sci. Technol. **24** (1996) 217. https://doi.org/10.1080/02786829608965365
8 A. Elasser and D. A. Torry: IEEE Trans. Power Electron. **11** (1996) 710. https://doi.org/10.1109/63.535403
9 L. M. Redondo: IEEE Trans. Plasma Sci. **38** (2010) 2725. https://doi.org/10.1109/TPS.2010.2050495
10 J. Zhang, D. D.-C. Lu, and T. Sun: IEEE Trans. Ind. Electron. **57** (2010) 1041. https://doi.org/10.1109/TIE.2009.2028336

About the Authors

Cheng-Tao Tsai received his B.S. degree in electrical engineering from Feng Chia University, Taichung, Taiwan, in 1991, and his M.S. and Ph.D. degrees from National Chung Cheng University, Chia-Yi, Taiwan, in 2003 and 2008, respectively. Recently, he joined National Chin-Yi University of Technology, Taichung, Taiwan, where he is currently a professor in the Department of Electrical Engineering. His current research interests include the design of switching-mode power supplies, power factor correction technology, and chargers for electric vehicles.

Jyun-Mao Chen received his B.A. degree in electrical engineering in 2019 from National Chin-Yi University of Technology, Taiwan. Currently, he is a master student. His area of research is switching-mode power supplies.