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77 GHz Quadrature Frequency Multiplier-by-nine with Superior Suppression for Radar Sensors

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A 77 GHz quadrature frequency multiplier-by-nine is demonstrated using the 90 nm CMOS process. The implemented multiplier-by-nine is composed of a high conversion gain quadrature frequency tripler with coupled lines as the buffer stage to reduce power consumption and increase power output. This frequency multiplier-by-nine achieves good suppression for the fundamental, second, and other harmonics. The conversion loss is −33 dB at 77 GHz. The DC power consumption is only 5.2 mW. The chip area is 0.46 mm^2. This device can help to improve the performance of high-frequency radar sensors.

1. Introduction

Recently, CMOS-based millimeter-wave integrated circuits (MWICs) have become increasingly important for their application to communication systems.[1]

Their main applications are as follows:

(1) 60 GHz wireless personal area networks (IEEE 802.15.3c),

(2) 77 GHz automotive radars,

(3) 81 to 86 GHz point-to-point high-speed data link.

Of all the applications, the millimeter-wave local oscillators are the core element, which bring big challenges in phase-locked loops (PLLs) design. Because there are tradeoffs between high-frequency signal generation and power consumption, the goal is to maximize the efficiency of circuit design.

Many frequency multipliers have been studied for high frequency applications. A K- to V-band CMOS fully differential subharmonic injection-locked frequency tripler has been proposed and analyzed,[2–6] but the harmonic suppression is low.[2,3,7,8] By cascading two frequency triplers together, a frequency multiplier-by-nine achieves high working frequency and wide bandwidth; however, the power consumption is too high.[9] A previous study[6] showed that one way to reduce the power consumption is to add one frequency multiplier at the output port of a voltage-controlled oscillator (VCO), which reduces the operation frequency and power consumption.

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In this paper, a 77 GHz quadrature frequency multiplier-by-nine fabricated using the CMOS 90 nm process is presented. It cascades a high-conversation-gain quadrature frequency tripler with coupled lines as a buffer stage. The multiplier has a power consumption of 5.2 mW with a chip area of 0.46 mm^2.

2. Circuit Design and Implementation

Early commonly used frequency multipliers were the A-class amplifier type and injection-locked type. Figure 1 shows the A-class amplifier-type frequency multiplier. It mainly takes advantage of the nonlinear characteristics of the transistor itself to extract the frequency multiplier harmonic signal ($N*f_{in}$), and uses the band-pass filter to suppress the remaining harmonics [$(n-1)*f_{in}$, $(n-2)*f_{in}$, ..., $1*f_{in}$]. The biggest disadvantage of this architecture is that the bandpass filter occupies a very large chip area, and both the input and output signals are single-ended, which limits the design architecture of the transceiver and makes it impossible to realize an IQ signal demodulation architecture with high demodulation quality. The injection-locked-type frequency multiplier is shown in Fig. 2. It is usually a differential input type. If the circuit is designed for an orthogonal signal output, an additional set of the same circuit is needed, which will increase the power consumption. In this paper, we propose a frequency multiplier-by-nine by cascading several orthogonal frequency triplers. As shown in Fig. 3, the biggest differences between this multiplier and the aforementioned ones are as follows:(1) harmonic suppression and output matching can be achieved through inductive coupling, which can greatly reduce the chip area;(2) the multiplier-by-nine can provide good conversion efficiency at a high frequency with orthogonal injection and its output can be directly applied to a millimeter-wave orthogonal receiver.

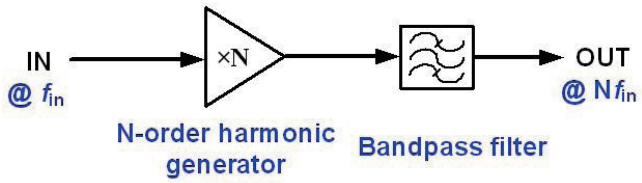

Fig. 1. (Color online) Structure of A-class amplifier-type multiplier.

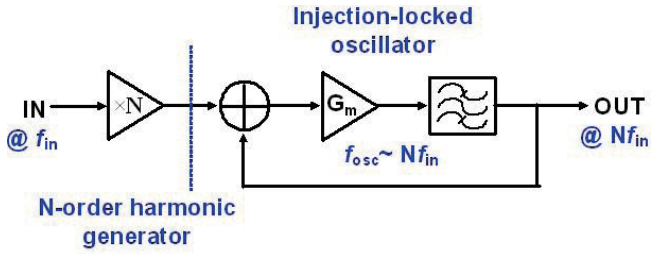

Fig. 2. (Color online) Structure of injection-locked-type multiplier.

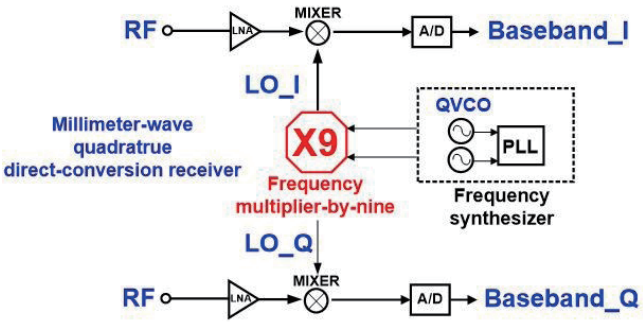

Fig. 3. (Color online) Structure of proposed frequency multiplier-by-nine.

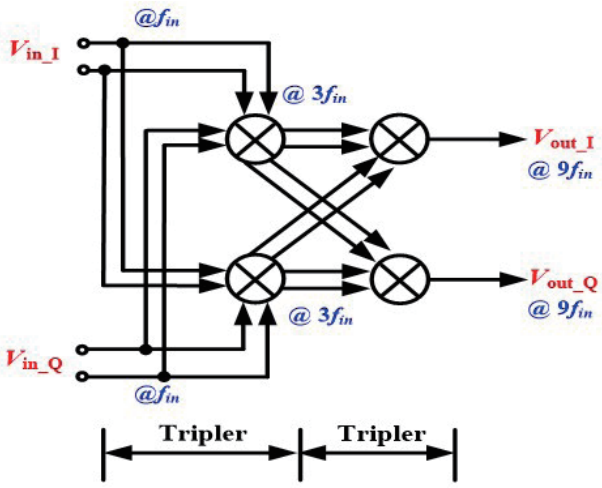

Fig. 4. (Color online) Inner structure of frequency multiplier-by-nine.

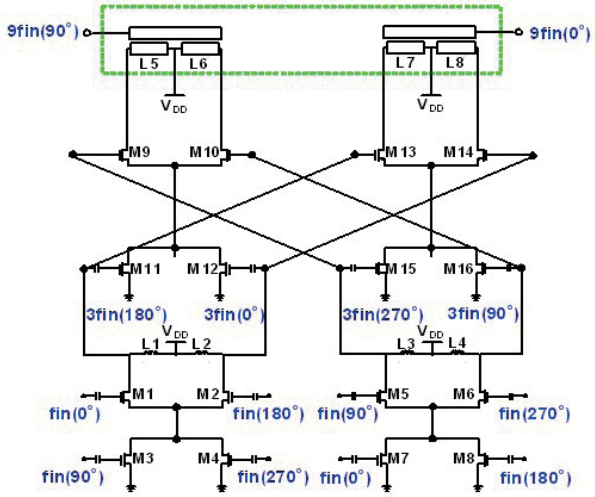

Fig. 5. (Color online) Schematic of quadrature frequency multiplier-by-nine.

The inner structure of the proposed frequency multiplier-by-nine, as depicted in Fig. 4, constitutes two triplers cascading together. A schematic of the quadrature frequency multiplier-by-nine is shown in Fig. 5. At the end of the circuit, a coupler line balun as shown in Fig. 6 is used to transmit the signal to the loading. The coupled-line balun works in the same way as the output inductors designed for 77 GHz resonance frequency, and offers good impedance matching for 50 Ω. It has the function of transforming the differential signals to a single-ended signal. The cancellation characteristic of the balun results in the suppression of the harmonics. As a result, the coupled lines effectively suppress the second harmonic signal of 51.33 GHz generated from the 77 GHz tripler. Figure 7 shows the reflectance coefficient of the couple line balun. For good impedance matching, the return loss of a port should be larger than 10 dB. At the frequency of 77 GHz, both the input and output return losses are larger than 14 dB. Figure 8 is the schematic of the tripler. The two transistors at the tail of the circuit

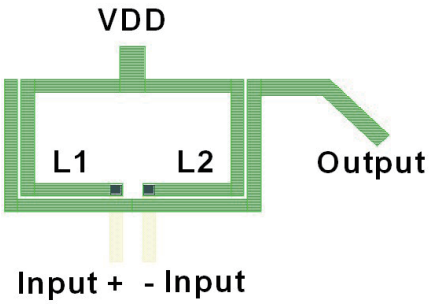

Fig. 6. (Color online) Layout of coupled-line balun.

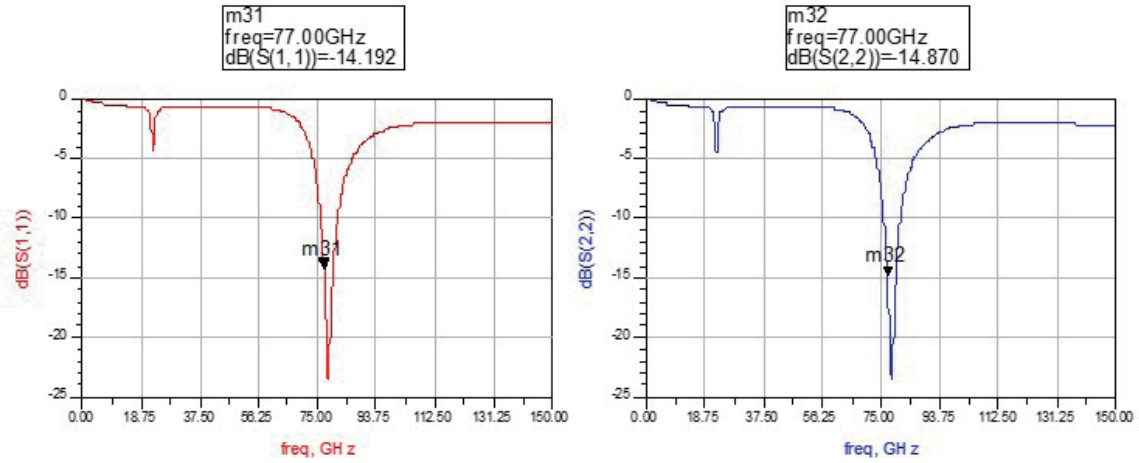

Fig. 7. (Color online) Reflectance coefficient of coupled-line balun.

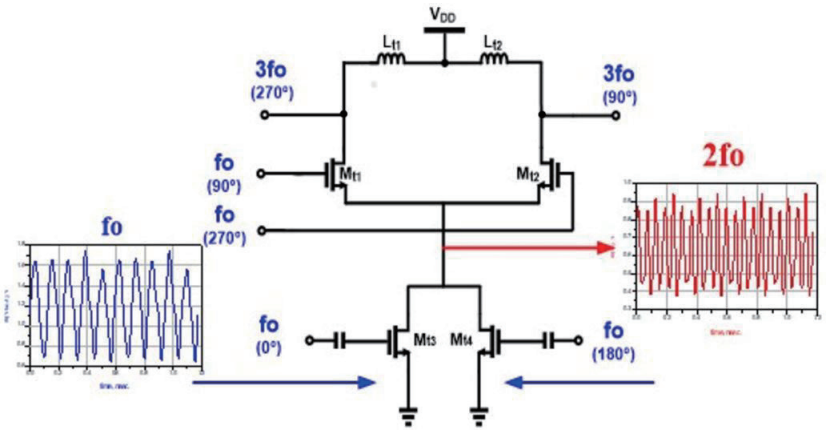

Fig. 8. (Color online) Schematic of tripler.

form a differential pair. By inputting a pair of differential signals f_{in}, a signal $2f_{in}$ is generated at the drain port. Then it is mixed with another input signal f_{in} and the output signal $3f_{in}$ is generated.

The measurement configuration is shown is Fig. 9. The chip uses on wafer measurement with an FR4 board. Quadrature signals are generated from the signal generator in series with balun and quadrature generators. These signals are transferred into the FR4 board through SMA connectors. The DC supply voltage is 1.2 V.

3. Results and Discussion

Figure 10 shows a micrograph of the fabricated chip. The chip is designed and fabricated using 90 nm CMOS technology and the area is 0.6 × 0.69 mm^2. Figure 11 shows the measured output power spectrum. The input signal is 8.33 GHz with a power of 0 dBm. The pre-layout and post-layout simulated results of the output power are −18.493 and −20.69 dBm, respectively. The measured result is −35.11 dBm with little frequency variation caused by the

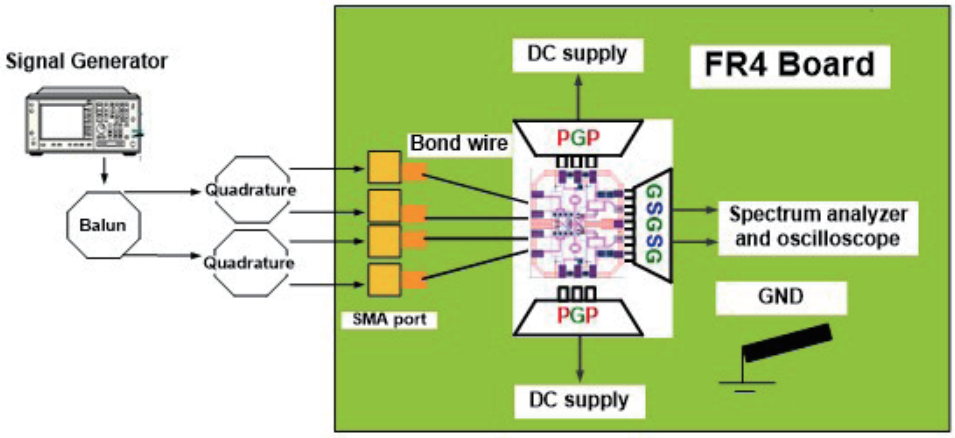

Fig. 9. (Color online) Measurement configuration of chip.

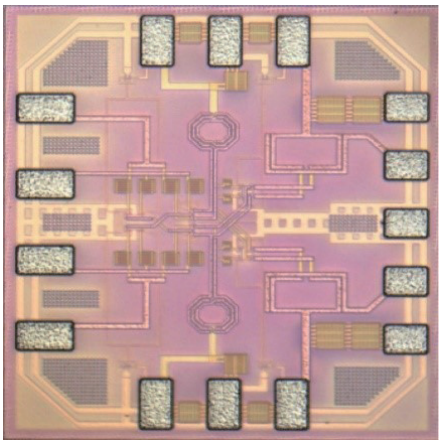

Fig. 10. (Color online) Micrograph of fabricated chip.

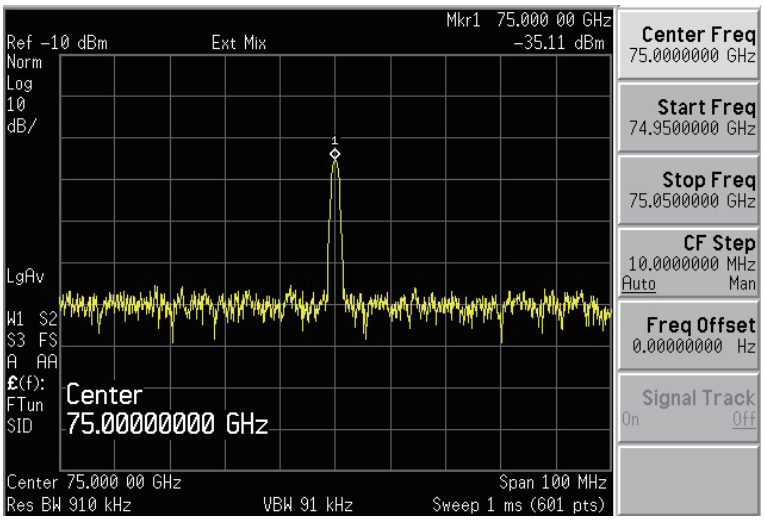

Fig. 11. (Color online) Output power spectrum with input power of 0 dBm.

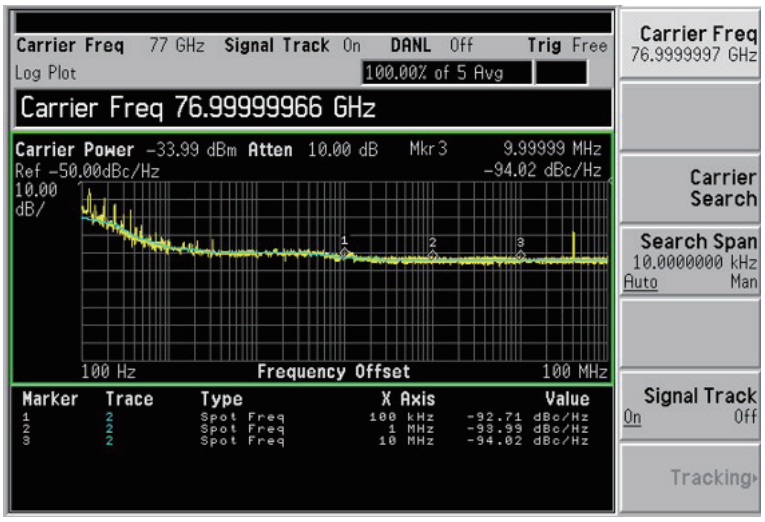

Fig. 12. (Color online) Output phase noise with input power of 0 dBm.

board's capacitors. The difference between simulation and measurement is mainly caused by the unilateral characteristic of the FET at a very high working frequency. The phase noise is measured with an input signal of 8.555 GHz. Figure 12 shows that the phase noise is −94.02 dBc/Hz at an offset of 10 kHz.

Figure 13 shows the calculated harmonic rejection ratios (HRRs) of the two major harmonics. The fundamental and second-order HRRs with the input signal at 8.555 GHz are as high as 46.9 and 41.6 dBc, respectively. The results demonstrate the good performance of the anti-interface of the multipliers, which confirms its applicability in radar sensors.

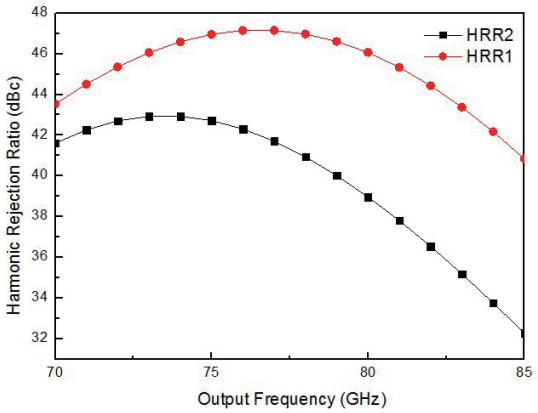

Fig. 13. (Color online) Harmonic rejection ratios of the multiplier.

Table 1
Comparison of reported multipliers.

Ref.	Technology	Multiplier ratio	Frequency (GHz)	Bandwidth (GHz)	P_{in}/P_{out} (dBm)	P_{diss} (mW)	HRR1 (dBc)	V_{DD} (V)	Chip size (mm^2)
(2) D-input D-output	0.13 μm CMOS	3	60	1.42 (locking range)	6/−14.81	1.86	22.65	1.2	0.46
(3) D-input Q-output	90 nm CMOS	3	60.6	9 (locking range)	0/−27.3	9.6 (core) 14.2 (buff)	<10	1	0.81
(7) D-input D-output	0.13 μm CMOS	3	58.92	3.9 (locking range)	0.5/−9.47	9.96 (core) 16.1 (buff)	31.3	1.2	0.85
(8) S-input S-output	GaAs mHEMT	9	92	14 (3 dB bandwidth)	9/−5	119	<15	1.2	2.25
This work Q-input Q-output	90 nm CMOS	9	77	5 (3 dB bandwidth)	0/−35.11	5.2	46.9	1.2	0.46

The performance of the proposed multiplier compared with those in other reported papers is summarized in Table 1.[2–5] The proposed multiplier can provide quadrature input and output signals with low power consumption. The 77 GHz multiplier has a multiplier ratio of 9 and its 3 dB bandwidth is 5GHz. The chip area is 0.46 mm^2 with a power consumption of 5.2 mW. The harmonic rejection of the proposed multiplier is the best among the multipilers.

4. Conclusion

A 77 GHz quadrature frequency multiplier-by-nine implemented by a 90 nm CMOS process has been presented. A coupled-line balun is utilized to improve the harmonic suppression and reduce power consumption. The cascading of two triplers and one buffer stage gives the circuit better performance for wireless communication systems and radar sensors.

Acknowledgments

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