Sensors and Materials, Vol. 34, No. 10 (2022) 3693–3706
MYU Tokyo

S & M 3070

Frequency Compensation with Capacitor Multiplier in DC–DC Converter

Lei Tian,[1*] Zhong Chen,[2] Qinqin Li,[1] and Weiheng Wang[3]

[1]School of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an 710121, China
[2]Department of Electrical Engineering, University of Arkansas, Arkansas 72201, USA
[3]Institution Sup Galilée, Université Paris 13, Villetaneuse, Paris 75001, France

(Received June 20, 2022; accepted August 22, 2022)

Keywords: frequency compensation, capacitor multiplier, current-mode, DC–DC converter

In this paper, we present on-chip frequency compensation with a capacitor multiplier for a current-mode control DC–DC converter. The capacitor multiplier technique can effectively remove the crossover frequency from the origin. An equivalent capacitance is obtained by amplifying the small current in the capacitor. The value of the equivalent capacitor can be adjusted. The functional block diagram and small-signal transfer function of a buck DC–DC converter are derived for a simplified system loop for on-chip frequency compensation with a capacitor multiplier. In this paper, the derived system transfer function for frequency compensation is verified by simulation and from test results. The proposed circuit is suitable for low-cost and small-size applications. Simulation results and experimental results are presented to demonstrate the theoretical analysis.

1. Introduction

Nowadays, many personal digital assistant (PDA) devices such as mobile phones, PDAs, and navigation systems are in great demand. A DC–DC converter is widely used in these devices to reduce power consumption and prolong battery life.(1) A traditional DC–DC converter is shown in Fig. 1(a). Outside the chip, capacitors C_c and C_2 and resistor R_C generate a low-frequency pole–zero pair. It is difficult to integrate such large capacitors into an IC.(2,3) Therefore, an extra external pin is needed to connect the large capacitors, which increases the PCB space of the whole system.

To reduce the harmful effect of parasitic elements and power loss in the bonding wire, it is necessary to make all circuits on the chip, as shown in Fig. 1(b). With the integration of the passive components, the chip minimizes the PCB space and the use of external pins.

*Corresponding author: e-mail: tianlei@xupt.edu.cn
https://doi.org/10.18494/SAM3980

ISSN 0914-4935
https://myukk.org/

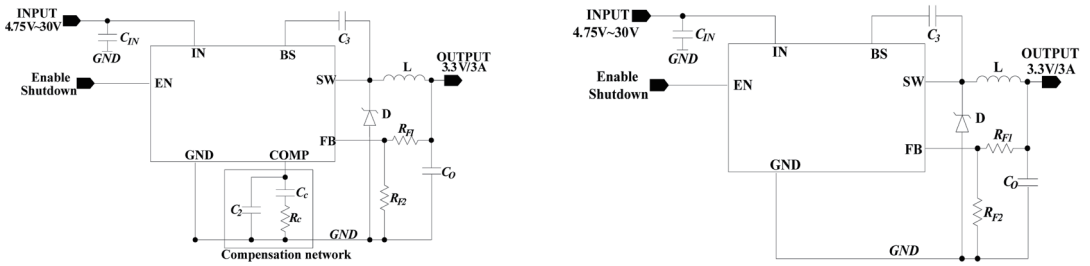

Fig. 1. (a) Typical DC–DC converter and (b) proposed DC–DC converter for DC–DC converter.

2. Analysis of Conventional Buck Converter

2.1 DC analysis

The duty cycle of a buck converter is proportional to the difference between the feedback voltage V_{FB} and the reference voltage V_{REF}. Within the inductor in the current loop, to ensure the stability of the closed loop, the system compensation network only compensates the pole by the filter capacitor and the zero by the relevant series resistors.[4,5] The buck DC–DC converter is shown in Fig. 2.

The DC value of V_{OUT} in Fig. 2 can be expressed as

$$V_{OUT} = g_m(MOD) \times V_{COMP} \times R_{LOAD}, \tag{1}$$

where $g_m(MOD)$ represents the transconductance of the modulator,[6] $g_m(MOD) \times V_{COMP}$ is the output current of the DC–DC converter, and R_{LOAD} represents the load resistance.

2.2 AC analysis

The loop transfer function of the system can be derived from Fig. 2 and is given as

$$H(s) = ADC * \frac{(1 + s/\omega_{z1})(1 + /\omega_{z2})}{(1 + s/\omega_{p1})(1 + /\omega_{p2})}. \tag{2}$$

ADC represents the DC gain of the system:

$$ADC = g_m(EA) \times \frac{R_{EA} \times R_{F2}}{R_{F1} + R_{F2}} \times g_m(MOD) \times R_{LOAD}, \tag{3}$$

where $g_m(EA)$ and R_{EA} represent the transconductance and output resistance of the error amplifier (*EA*), respectively. R_{F1} and R_{F2} are feedback resistances. From Eq. (2), there are two poles and two zeros in the compensator, which can be described as

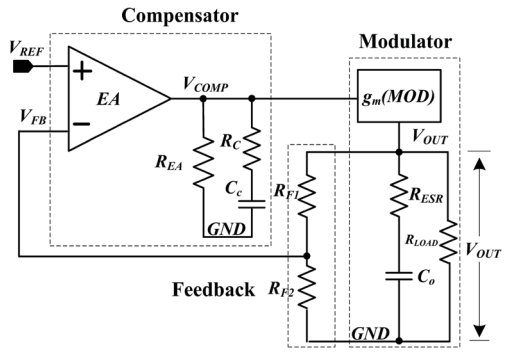

Fig. 2. Simplified loop of buck DC–DC converter.

$$\omega_{p1} = \frac{1}{(R_{EA} + R_C) * C_C}, \ \omega_{p2} = \frac{1}{R_{LOAD} * C_O}, \tag{4}$$

$$\omega_{z1} = \frac{1}{R_C * C_C}, \ \omega_{z2} = \frac{1}{R_{ESR} * C_O}. \tag{5}$$

Here, R_c is the compensation resistor, C is the compensation capacitor, R_{LOAD} is the load, and R_{ESR} represents the equivalent series resistance (ESR) of the output capacitor C_O.

3. Analysis of Proposed Capacitor Multiplier

3.1 Proposed capacitor multiplier

It is difficult to integrate the compensation capacitor on a chip because of its large volume, making it necessary to add an extra pin on the package for the outside capacitor. To integrate the capacitor into the IC, here, an operational transconductance amplifier (OTA) and voltage parallel negative feedback are combined. When the OTA and the feedback work together, the input impedance of the amplifier increases. This decreases the capacitance, which will reduce the volume of the capacitance and facilitate integration into the IC. The design flowchart is shown in Fig. 3.

To mitigate the negative effects of the conventional converter and reduce the area, the capacitor multiplier is widely used to realize large-capacitor integration.(7) The simplified system loop of the current-controlled DC–DC converter with the proposed capacitor is shown in Fig. 4.

Some modifications have been made compared with Fig. 2 and the compensator block has changed. The proposed compensator is achieved by the OTA, the EA, the capacitor C_C, and the resistor R_C. The control voltage V_{COMP} can respond to the value of the output voltage V_{OUT} and turn the power stage on or off.

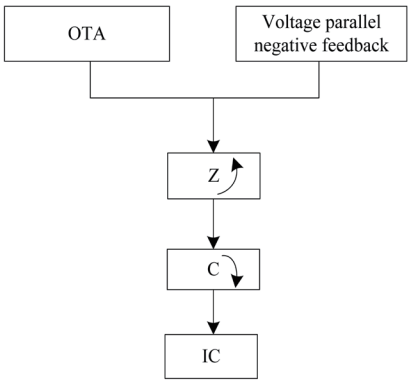

Fig. 3. Design flowchart.

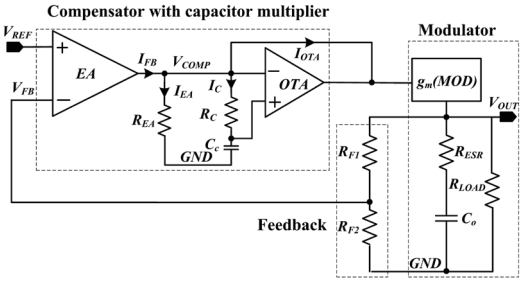

Fig. 4. Proposed simplified system loop of buck DC–DC converter.

3.2 Cascode OTA structure

The OTA is suitable for various voltage-mode and current-mode signal-processing tasks within a wide frequency range.[8,9] The capacitor multiplier technique can effectively move the crossover frequency compared with the original configuration.

The circuit implementation of this Cascode OTA is shown in Fig. 5. The transistors M_{P1} to M_{P5} are implemented as a standard Cascode bias circuit. A Cascode OTA is used as a single-stage amplifier with high gain and only one dominant pole.

3.3 Small-signal model

For the proposed system loop, the small-signal model (continuous buck converter model) is reviewed first.[10,11] Both the ESR of the capacitor and the direct current resistance (DCR) are considered to increase the accuracy of the model.

Figure 6 shows the three-terminal nonlinear terminal designations, where a, p, and c refer to active, passive, and common, respectively. R_i and $H_e(s)$ constitute the current loop. G_m, R_{EA}, gEA, OTA, and AC_{IN} constitute the voltage loop.[12] The invariant relations in the DC terminal quantities are given by

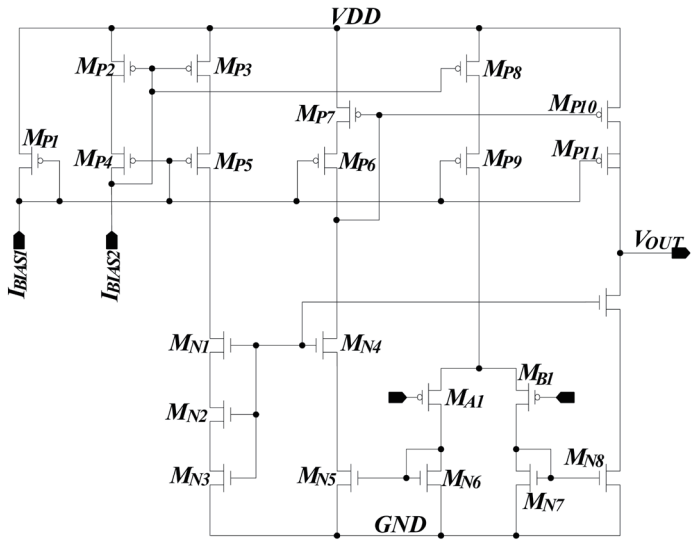

Fig. 5. OTA circuit.

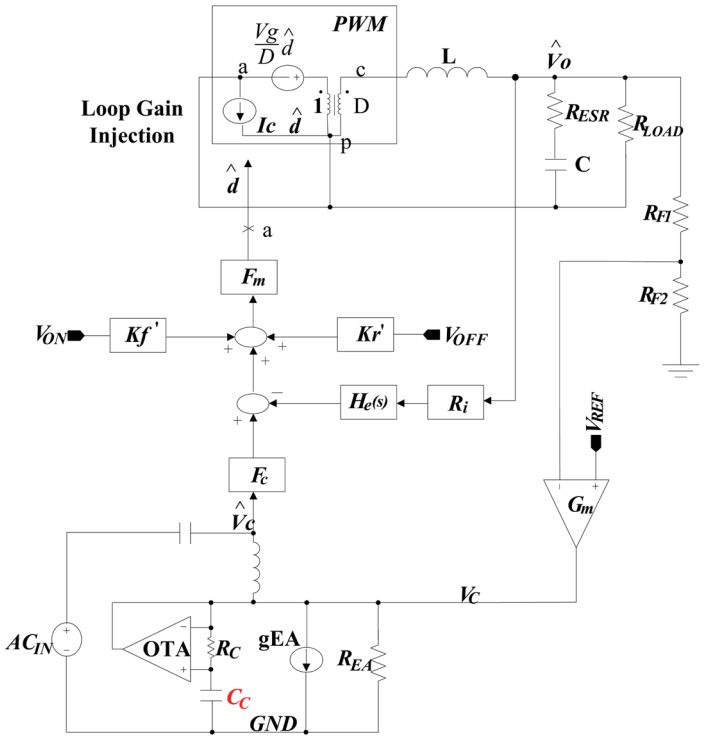

Fig. 6. (Color online) Small-signal model for proposed buck converter.

$$I_a(t) = \begin{cases} I_c(t), & 0 < t < Td \\ 0, & Td < t < T \end{cases} \tag{6}$$

$$V_{cp} = \begin{cases} V_{ap}(t), & 0 < t < Td \\ 0, & Td < t < T \end{cases} \tag{7}$$

where T and d represent the duty cycle and switching period of the DC–DC converter, respectively.

From Eqs. (6) and (7), the average currents $\overline{I_a(t)}$, $\overline{I_c(t)}$, $\overline{V_{ap}(t)}$, and $\overline{V_{cp}(t)}$ can be simplified to

$$\overline{I_a(t)} = \overline{I_c(t)} * d, \tag{8}$$

$$\overline{V_{cp}(t)} = \overline{V_{ap}(t)} * d. \tag{9}$$

We assume that the system works at a DC point and then add a small AC instantaneous signal. The terminal DC current is I_a, the instantaneous AC is $\widehat{i_a}$, the DC duty cycle of $d(t)$ is D, the instantaneous AC is $\hat{d}$, the DC component of $V_{ap}(t)$ is V_{ap}, the instantaneous AC is $\widehat{V_{ap}}$, the DC component of $V_{cp}(t)$ is V_{cp}, and the instantaneous AC is $\widehat{V_{cp}}$. The signals are given by

$$I_a(t) = I_a + \widehat{i_a}, \tag{10}$$

$$d(t) = D + \hat{d}, \tag{11}$$

$$V_{cp}(t) = V_{cp} + \widehat{V_{cp}}, \tag{12}$$

$$V_{ap} = V_{ap} + \widehat{V_{ap}}. \tag{13}$$

From Eqs. (8)–(13), we obtain

$$I_a + \widehat{i_a} = \left(D + \hat{d}\right)\left(I_c + \widehat{i_c}\right) = DI_c + D\widehat{i_c} + \hat{d}I_c + \hat{d}\widehat{i_c}, \tag{14}$$

$$V_{ap} + \widehat{V_{ap}} = \left(D + \hat{d}\right)\left(V_{ap} + \widehat{V_{ap}}\right) = DV_{ap} + D\widehat{V_{ap}} + \hat{d}V_{ap} + \hat{d}\widehat{V_{ap}}. \tag{15}$$

For a very small instantaneous AC value, the values of $\hat{d}\widehat{i_a}$ and $\hat{d}\widehat{V_{ap}}$ can be neglected, giving

$$\widehat{i_a} = D\widehat{i_c} + \hat{d}I_c, \tag{16}$$

$$\widehat{V_{ap}} = D\widehat{V_{ap}} + \hat{d}V_{ap}. \tag{17}$$

Thus, the PWM switching model in Fig. 5 can be achieved. For the power stage of the current-mode converter, the control-to-output transfer function has two separate real poles as described in Refs. 13 and 14. One pole from the output filtering capacitor is heavily dependent on the equivalent resistance of the output load R_{LOAD}. The compensator in the feedback network is used to generate poles and zeros for pole–zero cancellation as shown in Fig. 4.

As shown in Fig. 3, the output current of the EA is given by

$$I_{FB} = gm(EA) * V_{FB} . \tag{18}$$

The current through resistor R_{EA} is then given by

$$I_{EA} = I_{FB} - I_C - I_{OTA} . \tag{19}$$

The output current of the OTA is then given by

$$I_{OTA} = gm(OTA) * I_C * R_C . \tag{20}$$

The output voltage of the EA is

$$V_{COMP} = I_{EA} * R_{EA} = I_C * (R_C + \frac{1}{C_C S}) . \tag{21}$$

From Eqs. (18)–(21), V_{COMP} can be expressed as

$$V_{COMP} = \frac{I_{FB} * R_{EA} * (1 + R_C * C_C S)}{1 + [(1 + gm(OTA) * R_C) * R_{EA} + R_C] C_C S} . \tag{22}$$

The transfer function of this compensator is

$$\frac{V_{COMP}}{V_{FB}} = gm(EA) * R_{EA} * \frac{(1 + R_C * C_C S)}{1 + [(1 + gm(OTA) * R_C) * R_{EA} + R_C] C_C S} . \tag{23}$$

3.4 Transfer function of system with proposed compensator

We next calculate the poles and zeros of the proposed compensator circuit.[15,16] As shown in Fig. 4, the transfer function of the system with the proposed compensator can be obtained as

$$H(s) = ADC' * \frac{(1 + s / \omega'_{z1})(1 + / \omega'_{z2})}{(1 + s / \omega'_{p1})(1 + / \omega'_{p2})}. \tag{24}$$

The gain of the system is then given by

$$ADC' = gm(EA) * R_{EA} * \frac{R_{F2}}{R_{F1} + R_{F2}} * gm(MOD) * R_{LOAD} = ADC. \tag{25}$$

From Eq. (24), the proposed compensation circuit utilizes two zeros and two poles, which are expressed as

$$\omega'_{p1} = \frac{1}{\left(R_{EA} + R_C + gm(OTA) * R_{EA} * R_C\right) * C_C}, \quad \omega'_{p2} = \frac{1}{R_{LOAD} * C_O}, \tag{26}$$

$$\omega'_{z1} = \frac{1}{R_C * C_C}, \quad \omega'_{z2} = \frac{1}{R_{ESR} * C_O}. \tag{27}$$

For $R_{EA} >> R_C$,

$$\omega_{p1} = \frac{1}{R_{EA} * (1 + gm(OTA) R_C) * C_C}. \tag{28}$$

To design the transconductance of the OTA properly, we set $f''_{p1} = f'_{p1}$. Comparison of Eqs. (4) and (5) with Eqs. (26) and (27) shows that capacitor C_C is much smaller than that in the conventional system. Thus, the first zero f''_{z1} of the proposed system is larger than that of the traditional system. The second pole f_{p2} and second zero f''_{z2} are the same as those of the traditional system. Moreover, the second zero f'_{z2} has no effect on the stability of the system because it lies out of the bandwidth. According to Eq. (28), the capacitor C_C is effectively multiplied by a factor of 1 + $g_m(OTA)$ * R_C. Figure 7 shows the frequency response of the conventional system and the proposed system.

According to Fig. 6, f_c can be expressed as

$$f_c = A_V \cdot f_{p1} \cdot f_{p2} / f_{z1}. \tag{29}$$

The phase at point f_c is

$$-arctg \frac{f_c}{f_{p1}} - arctg \frac{f_c}{f_{p2}} - arctg \frac{f_c}{f_{z1}}. \tag{30}$$

The crossover frequency f_c has moved to the lower frequency $f_{c'}$, making the system more stable than the conventional one.

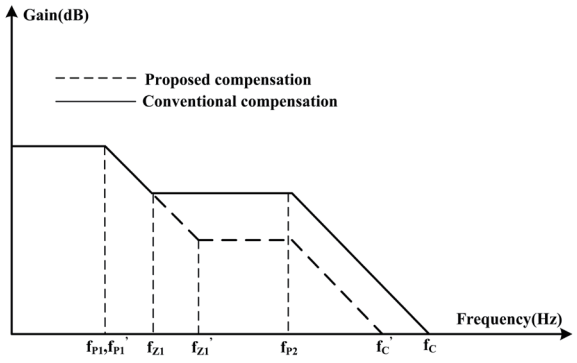

Fig. 7. Frequency response of the current-mode DC–DC converter.

4. Simulation Results

For the designed buck DC–DC converter, the switching frequency is 500 kHz, the MOSFET on resistance is 100 mΩ, and the diode forward resistance is 100 mΩ. Its operating conditions are shown in Table 1.

Bode plots of the loop transfer function given in Eq. (24) are shown in Fig. 8, which illustrates its amplitude-frequency and phase-frequency characteristics. The derived transfer function is a low-pass filter transfer function with two zeros and two poles. In addition, the phase margin of the loop is larger than 60° through the entire range of the load current. Hence, the proposed capacitor multiplier technique has sufficient phase margin to maintain a stable loop.

5. Experimental Results

This DC–DC converter using the proposed capacitor multiplier technique is implemented with a 0.35 μm CMOS process. Its layout is shown in Fig. 9, the die size is 1600 × 1600 μm^2, and the proposed compensator area is 120 × 300 μm^2. The experimental results indicate that the output is stable with no oscillation regardless of the load condition and duty cycle.

The start-up waveform with an input voltage of 12 V, output voltage of 5 V, and current load of 3 A is shown in Fig. 10(a). The output voltage smoothly increases without the overshoot issue. The result of the load transient response under conditions V_{IN} = 12 V and V_{OUT} = 5 V is shown in Fig. 10(b). The load current jumped from 1.5 to 3 A and the output voltage recovered in 50 μs.

The load regulation is less than 0.6% at room temperature. Additionally, the current of the inductor has no overshoot. The performance of the proposed compensator is in good agreement with the theoretical analysis.

The results of power on and power off under the conditions V_{IN} = 12 V, V_{OUT} = 5 V, and I_{LOAD} = 3 A are shown in Figs. 10(c) and 10(d), respectively. As can be seen, the converter can switch between power on and power off. Under the conditions V_{IN} = 12 V, V_{OUT} = 5 V, and I_{LOAD} = 1 A, the short waveform and short recovery waveform are shown in Figs. 11(a) and 11(b), respectively.

Table 1
Chip performance parameters.

Performance parameter	Value
Input voltage	12 V
Output voltage	5 V
Output current range	<3 A
Inductor (off-chip)	4.7 μH
Inductor ESR	10 mΩ
Input capacitor (off-chip)	10 μF
Output capacitor (off-chip)	44 μF

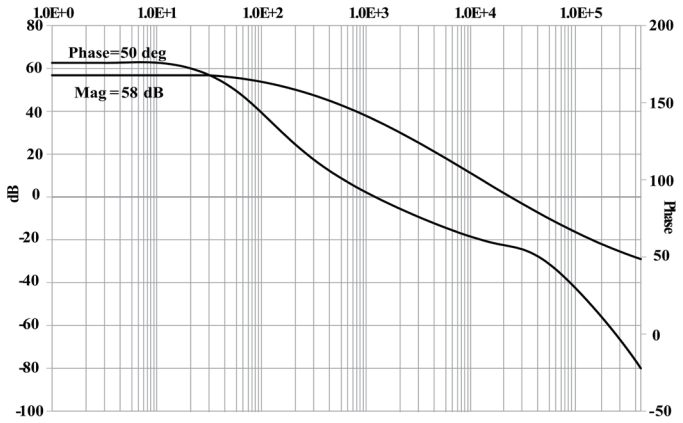

Fig. 8. Bode plots of the loop transfer function.

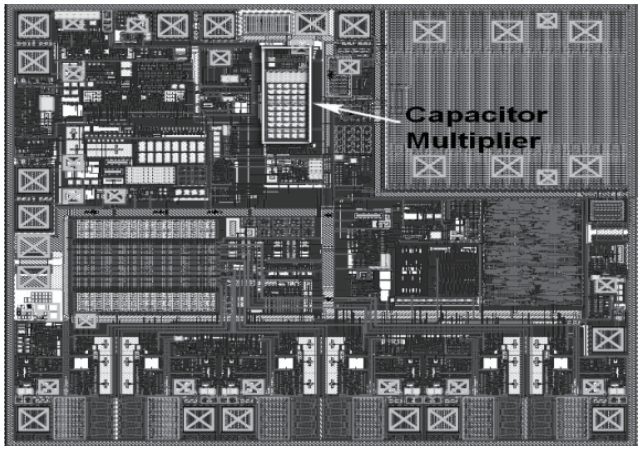

Fig. 9. Layout of the DC–DC converter.

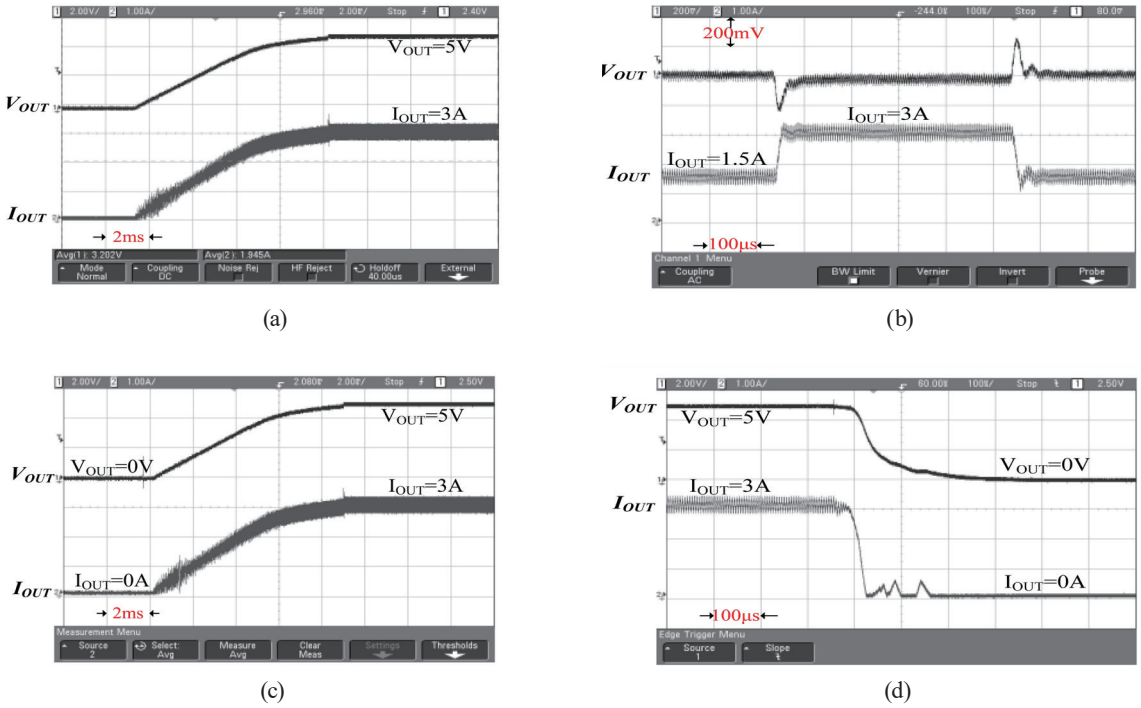

Fig. 10. (Color online) Start-up waveform in different situations. (a) Start-up waveform with I_{LOAD} = 3 A. (b) Output transient with I_{LOAD} (1.5–3 A). (c) Power on waveform with I_{LOAD} = 3 A. (d) Power off waveform with I_{LOAD} = 3 A.

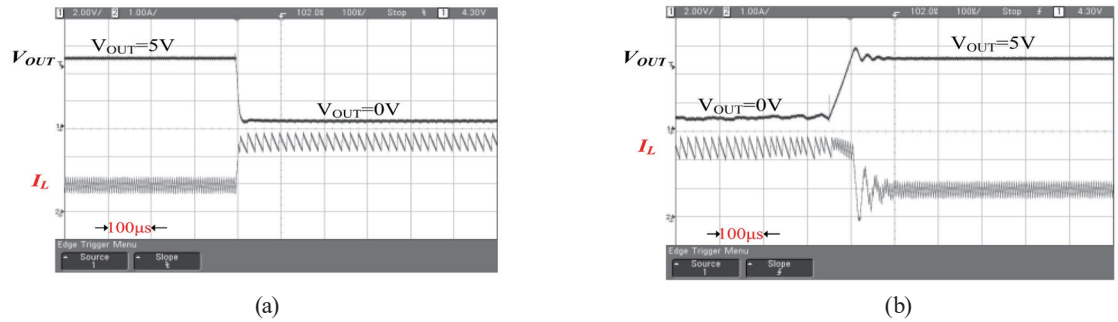

Fig. 11. (Color online) Output waveforms. (a) Short waveform with I_{LOAD} = 1 A. (b) Short recovery waveform with I_{LOAD} = 1 A.

In Fig. 11, V_{OUT} is the output voltage and I_L is the inductor current. In the normal operation, the output voltage is 5 V, the load current is 1 A, and the average value of the inductor current I_L is also 1 A. As can be seen, during the short period, the output voltage V_{OUT} reaches zero. Since the current limit value is 2.5 A, the average value of the I_L is 2.5 A. Moreover, during the recovery, both waveforms return to their initial shapes.

The efficiency with an input voltage of 12 V and an output voltage of 5 V is shown in Fig. 12. The maximum efficiency is 94% at a loading current of 500 mA. There are two major power dissipations, namely, conduction loss and switching loss. In Fig. 12, conduction loss is dominant when the loading current is larger than 500 mA, and efficiency decreases. On the other hand, switching loss is dominant when the loading current is less than 500 mA, and efficiency decreases with decreasing load current.

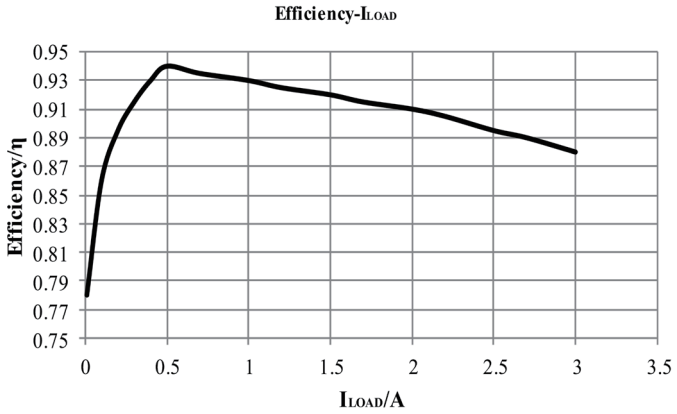

Fig. 12. Efficiency waveform with I_{LOAD} (0–3 A).

6. Conclusion

A small capacitor compensation buck DC–DC regulator based on novel on-chip frequency compensation with a capacitor multiplier for a current-controlled DC–DC converter was proposed. The proposed structure is simple to implement. An equivalent capacitance is obtained by amplifying the small current in the capacitor. The value of the equivalent capacitor can be adjusted by the transconductance of the OTA and the compensation resistor. Using the proposed compensation, the footprint area is significantly reduced and the external pins are simplified. The proposed buck DC–DC regulator achieves full load-current stability and high efficiency. These features make it very attractive as a DC–DC regulator. In addition, the proposed compensation is suitable not only for buck DC–DC regulators, but also for boost DC–DC regulators.

Acknowledgments

This work was partly supported by the Natural Science Basic Research Program of Shaanxi (Program No. 2021JM-460) and the Scientific Research Program of Shaanxi Provincial Education Department (No. 21JC033).

References

1 D. Kilani, M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail: IEEE Trans. Circuits Syst. **63** (2016) 10. https://doi.org/10.1109/TCSI.2016.2586117
2 B. Poorali, E. Adib, and H. Farzanehfard: IET Power Electron. **13** (2017) 13. https:// 10.1049/iet-pel.2016.0513
3 A. Ghosh, S. Banerjee, M. K. Sarkar, and P. Dutta: IET Power Electron. **9** (2016) 5. https://doi.org/10.1109/TIE.2016.2551201
4 M. Saoudi, A. El-Sayed, and H. Metwally: IEEE Aerosp. Electron. Syst. Mag. **6** (2017) 1. https://doi.org/10.1109/MAES.2017.150261
5 S. R. Challa, D. Kastha, and A. Patra: IEEE Trans. Power Electron. **31** (2015) 1. https://doi.org/10.1109/TPEL.2015.2398574

6 Y. P. Su, W. C. Chen, Y. P. Huang, Y. H. Lee, K. H. Chen, and H. Y. Luo: IEEE Trans. VLSI Syst. **22** (2014) 10. https://doi.org/10.1109/TVLSI.2013.2283606
7 K. Y. Cheng, F. Yu, F. C. Lee, and P. Mattavelli: IEEE Trans. Power Electron. **28** (2010) 3. https:// 10.1109/TPEL.2012.2206403
8 O. Abdelfattah, G. W. Roberts, I. Shihand, and Y. C. Shih: IEEE Trans. Circuits Syst. **62** (2015) 10. https://doi.org/10.1109/TCSI.2015.2469011
9 A. P. Nicholson, A. N. Irfansyah, J. Jenkins, T. J. Hamilton, and T. Lehmann: IEEE Trans. VLSI Syst. **25** (2017) 6. https://doi.org/10.1109/TVLSI.2017.2657885
10 K. Zhang, Z. Shan, and J. Jatskevich: IEEE Trans. Power Electron. **32** (2017) 3. https://doi.org/10.1109/TPEL.2016.2555929
11 S. R. Challa, D. Kastha, and A. Patra : IEEE Trans. Power Electron. **31** (2016) 1. https://doi.org/10.1109/TPEL.2015.2398574
12 C. T. Tsai, J. C. Su, and S. R. Wei: Sens. Mater. **31** (2019) 2. https:// 10.18494/SAM.2019.2086
13 P. H. Liu, Y. Yan, F. C. Lee, and P. Mattavelli: IEEE Trans. Power Electron. **33** (2018) 2. https://doi.org/10.1109/TPEL.2017.2736005
14 A. Tahavorgar and J. E. Quaicoe: IEEE Trans. Power Electron. **32** (2017) 5. https://10.1109/TPEL.2016.2593867
15 B. Yuan, X. Q. Lai, H. Y. Wang, and Q. Ye: IEEE Trans. Circuits Syst. **6** (2014) 12. https://doi.org/10.1109/TCSII.2014.2356915
16 C. L. Wei, C. H. Wu, L. Y. Wu, and M. H. Shih: IEEE Trans. Circuits Syst. II. **57** (2010) 10. https://10.1109/TCSII.2010.2058594

About the Authors

Lei Tian received his master's degree in mobile communication from Xi'an University of Science and Technology in 2006. In 2015, he received his Ph.D. degree in optoelectronic integrated circuit design (OEIC) from Xidian University. In 2019, he completed his postdoctoral study in Northwest University. His research interests include analog and mixed integrated circuits, photoelectric signal processing, optocouplers, SOC design, and IR communications. (tianlei@xupt.edu.cn)

Zhong Chen received his doctorate degree in electrical engineering from North Carolina State University, a master's degree in electrical engineering from National University of Singapore, and a bachelor's degree in instrumentation science and engineering from Zhejiang University, China. He worked for six and half years as an ESD specialist in analog technology development at Texas Instruments prior to joining the Faculty of Electrical Engineering, University of Arkansas in 2015 as an assistant professor.

Qinqin Li received her master's degree in circuits and systems from Xidian University in 2014. Since then, she has been pursuing a doctoral degree from Xidian University. Her research interests include digital and analog mixed integrated circuits and optoelectric processing circuits.

Weiheng Wang received his B.S. degree in electronics from Xi'an University of Posts and Telecommunications in 2010. He received his master's degree and engineer title in telecoms and networks from Institut Sup Galilée, Université Paris 13, Villetaneuse, France in 2014. Since 2014, he has been working for Vente-Privée (French's top e-commerce firm). His research interests include power electronics and the design and testing of integrated optoelectric circuits.