

Influence of Buried Oxide Layer and Bias State on Total Ionizing Dose of Fully Depleted Silicon-on-insulator Devices

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A fully depleted silicon-on-insulator (FDSOI) device is a promising structure for future ultrascaled devices because of its high radiation resistance. The buried oxide (BOX) layer of an FDSOI device not only enhances its robustness against single event effects (SEE) but also greatly reduces its ability to resist the effect of the total ionizing dose (TID). We studied factors such as the thickness of BOX layers and the bias state of FDSOI devices and proposed a 22 nm N-type FDSOI 2D device structure. The method of adding fixed charges to the BOX layer and adding state charges to the interface was used to simulate the TID effect. We showed that the thinner the BOX layer, the better the device's ability to resist the effects of the TID. Increasing the total radiation dose causes the electron density of the channel to increase, indicating that the electron mobility of the channel is degraded. Because a large number of electrons are generated by irradiation, their density increases, causing a large number of electrons to collide with each other and scatter under a bias voltage, resulting in decreased electron mobility. By activating the built-in radiation model of the Sentaurus next-generation technology computer-aided design (TCAD) simulation tool, the device was used to simulate the TID effect under different doses in different bias states (OFF, ON, and transmission). The results showed that the most unappealing bias state of the TID effect for the short-channel N-type FDSOI device is the off state. This research provides new insights into the TID for FDSOI devices and can provide guidelines for future applications of radiation-hardened FDSOI-based circuits. The study of single particle effects plays an important role in the study of image sensors in space stations.

1. Introduction

When a spacecraft is in orbit, its built-in semiconductor electronic components are continuously irradiated by particles in space, leading to the formation of trap charges at the oxide layer and at the interface between the silicon layer and the oxide layer. These trap charges degrade device performance, which is referred to as the total ionizing dose (TID) effect.^(1–3) The TID effect leads to threshold voltage drift, increased off-state leakage current, decreased transconductance, and other issues^(4,5) up to the permanent failure of the circuit function. For nanoscale fully depleted silicon-on-insulator (FDSOI) devices,^(6–10) the gate oxide layer may be

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very thin,^(11–13) which makes the effect of gate oxygen trap charges generated by irradiation on device performance negligible. Therefore, the buried oxide (BOX) layer is the main factor influencing the response to radiation.^(14–18)

In recent years, single event effects (SEEs) research on FDSOI technology has been performed worldwide. At present, the process parameters used in the traditional study of SEEs are relatively large, mainly 130, 90,⁽¹⁹⁾ and 65 nm.⁽²⁰⁾ Research on the SEE in FDSOI devices with sizes below 22 nm is still lacking. In 2019, Pasupathy and Bindu analyzed the bipolar amplification induced by heavy ion irradiation in 45 nm FDSOI devices.⁽²¹⁾ They compared the sensitivity of a device with a thick BOX layer with that of a device with a thin BOX device and a doped back layer. They concluded that the bipolar gain of an FDSOI with a thin 45 nm BOX layer is smaller than that of a device with a thick BOX layer. In 2019, Cai *et al.* proposed an anti-single event upset 8T-static random access memory (SRAM) cell using 22 nm ultrathin body BOX FDSOI technology and implemented it on a test memory chip.⁽²²⁾ For FDSOI devices, the extremely thin top silicon film reduces the amount of charge generated. FDSOI devices are considered to reduce the SEE. However, when the technology node was reduced to 28 nm and below, because of the very short channel length, the amplification effect was further enhanced,⁽²³⁾ and both the power supply voltage and the charge stored on each sensitive node were reduced. These factors may increase the TID sensitivity of FDSOI devices. Therefore, it is necessary to study the TID effect on ultrathin FDSOI devices.

Technology computer-aided design (TCAD) software is important for simulating the TID of devices. Currently, most software simulates the TID effect by adding a fixed charge. Although this method can simulate some of the performance degradation of devices after irradiation, the distribution and charge density of the fixed positive charge at the interface added in the simulation process are subjective and arbitrary and are often not consistent with the actual situation.

2. Device Model and TID Simulation

We studied an N-type FDSOI device with a 22 nm process node. The thickness of the gate oxide layer of the device was about 3 nm and the operating voltage was about 0.8 V. Figure 1 shows a 2D N-type FDSOI device built using Sentaurus Structure Editor (SDE). Table 1 gives the parameters of the device.

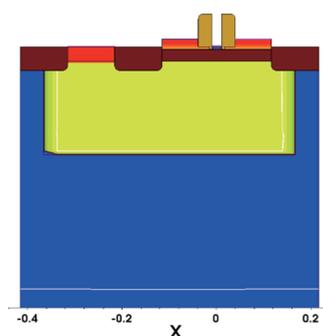


Fig. 1. (Color online) Two-dimensional structure of N-type FDSOI device.

Table 1
Device parameters.

Parameters	Lg (nm)	Louter (μm)	Lactive (μm)	Doping body (cm^{-3})	Doping SD (cm^{-3})	TBP (μm)	t_{ox} (nm)	T_{BOX} (nm)	Doping ldd (cm^{-3})	Doping BP (cm^{-3})	Depth value (cm^{-3})
Value	22	0.1	0.1	1×10^{15}	2.4×10^{20}	0.2	3	10/20	1×10^{18}	1×10^{17}	5×10^{18}

Figures 2(a) and 2(b) respectively show transfer characteristic curves and output characteristic curves obtained using the process library provided by the chip foundry and calibrated by Spectre. The output characteristic curves and transfer characteristic curves of the 2D device model constructed by TCAD are basically consistent with those of the standard device in order of magnitude, which verifies the correctness of the device structure.

2.1 Simulation of TID by adding fixed charge

Studies have shown that the threshold voltage drift caused by radiation has the following relationship with the trap charge and oxide layer thickness:^(11,15)

$$\Delta V_{ot} = -\frac{q}{\epsilon_{ox}} t_{ox} \Delta N_{ot}, \quad (1)$$

where q is the electric charge, ϵ_{ox} is the dielectric constant of the oxide, t_{ox} is the thickness of the oxide layer, and ΔV_{ot} is the density of the net positive trap charge of the oxide layer. The threshold voltage drift is toward the negative direction on the transfer curve.

The relationship between the interface state charge of Si/SiO₂ caused by radiation and the induced threshold voltage drift is^(11,15)

$$\Delta V_{it} = \frac{q}{\epsilon_{ox}} t_{ox} \Delta N_{it}, \quad (2)$$

where ΔV_{it} is the density of the net negative trap charge at the interface. The threshold voltage drift is in the positive voltage direction on the transfer curve. Because the interface state of an N-type transistor reflects the acceptor type and is significantly electronegative, the threshold voltage drift is in the direction of positive voltage. Because the charge density of the oxide traps generated by radiation is greater than the density of the interface states, the charge on the interface state traps compensates for part of the positive charge; thus, the drift of the threshold voltage partially recovers.^(14–16)

According to the literature,⁽¹⁷⁾ there is a linear relationship between the density of the oxide trap charge and the irradiation dose. The volume density N_{ot} of oxide traps has a linear relationship with the irradiation dose:

$$N_{ot} = g_0 D f_Y(E_{ox}) f_{ot}, \quad (3)$$

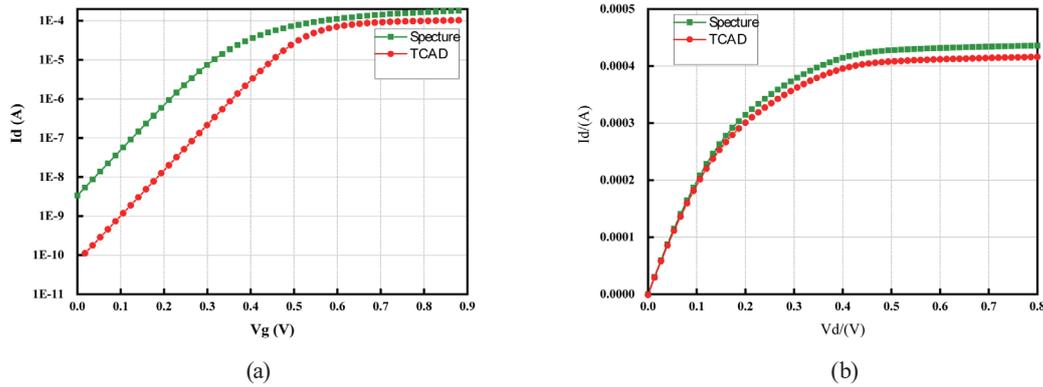


Fig. 2. (Color online) (a) Transfer characteristic curves and (b) output characteristic curves.

where $g_0 = 7.88 \times 10^{12} \text{ rad}^{-1} \cdot \text{cm}^{-3}$ represents the number of electron–hole pairs generated in a unit of SiO_2 by a unit radiation dose; D is the radiation dose in rad; f_{ot} is an empirical parameter related to the process and is taken to be 0.7 ($T_{BOX} = 20 \text{ nm}$) in this study. In Eq. (4), $f_Y(E_{ox})$ is the hole generation rate, which is related to the electric field and the radiation particle energy. When the radiation source is ^{60}Co , its value is expressed as

$$f_Y(E_{ox}) = \left[(0.55/E_{ox}) + 1 \right]^{-0.7}, \quad (4)$$

where E_{ox} is the electric field in the BOX layer in MV/cm. Because the interface state of an N-type metal–oxide–semiconductor field-effect transistor (MOSFET) transistor primarily reflects the acceptor type and is significantly electronegative, Eq. (5) shows that an increase in the charge surface density N_{it} in the interface trap is directly related to radiation dose D :⁽¹⁷⁾

$$N_{it} = K d_{ox} D^{2/3}, \quad (5)$$

where K is the proportionality coefficient and d_{ox} is the thickness of the oxide layer.

The values of K and f_{ot} are determined and given in Table 2. Because a 100 nm oxide layer radiates $1.0 \times 10^4 \text{ Gy}$ under a positive gate voltage, it normally forms a boundary state charge of $5.0 \times 10^{11} \text{ cm}^{-2}$.⁽¹⁸⁾ The results in this paper are of the same order of magnitude as the values in Ref. 18.

After the value of K is calculated, because K and f_{ot} are strongly dependent on the process, it is necessary to fit the experimental data to obtain an approximate value. For the BOX layers of similar thickness, the values of f_{ot} are 0.1 and 0.7, and the results of the simulation are shown in Table 2. When the radiation dose is 0, 10, 100, 300, 500, 700, or 900 krad (Si) and H_{BOX} is 10 nm, the amount of fixed positive charge added to the BOX layer should be from 0 to $6.40 \times 10^{17} \text{ cm}^{-3}$ and the fixed negative charge density at the interface between the top silicon and the BOX layer should be from 0 to $6.50 \times 10^{10} \text{ cm}^{-3}$. When H_{BOX} is 20 nm, the amount of fixed positive charge added to the BOX layer should be from 0 to $4.50 \times 10^{18} \text{ cm}^{-3}$, and the fixed negative charge

Table 2

Values of K and f_{ot} corresponding to BOX layers of different thicknesses.

Thickness of BOX	f_{ot}	K
$H_{BOX} = 10$ nm	0.1	$K = 3.48 \times 10^5 \text{ cm}^{-2}/(\text{nm}\cdot\text{rad})$
$H_{BOX} = 20$ nm	0.7	$K = 3.48 \times 10^5 \text{ cm}^{-2}/(\text{nm}\cdot\text{rad})$

density at the interface between the top of the silicon and the BOX layer should be from 0 to $6.50 \times 10^{10} \text{ cm}^{-3}$. The total dose effect is simulated by adding a fixed charge model.

2.2 Simulation of TID using radiation model of Sentaurus

Because the radiation model in the Sentaurus device does not work in the SiO_2 BOX layer modeled by SDE,^(17,18) the BOX layer in the simulation structure is defined as the “OxideAsSemiconductor” (OAS) material in the Sentaurus TCAD. The parameters of the OAS parameter file are replaced so that the radiation model can be activated. In the process of simulating irradiation, a fixed bias is added to the device to produce a device under three different offsets: ON state, OFF state, and transmission state (TG). These three bias states correspond to the three most common operating states of MOS devices in digital circuits. A more detailed description of each bias state is shown in Table 3. The Poole–Frenkel model was used to capture and launch the trap centers. The Poole–Frenkel model is often used to explain the transport effect in a dielectric layer, and it predicts the emission probability of intensified charge trap centers under a high applied electric field.

3. Results and Discussion

3.1 TID simulation of adding fixed charge on BOX layers of different thicknesses

Figures 3(a) and 3(b) show that a device with a BOX layer thickness of 20 nm is more affected by the TID effect than one with a BOX layer thickness of 10 nm. As the TID increases, the device characteristics deteriorate. The main reason for this behavior is that the hole–electron pairs generated by the radiation in the BOX layer collect in the drain electrode under the combined action of the positive gate voltage and the scanning voltage of the drain pair source, resulting in a significant increase in the output current of the drain electrode. Figure 3(c) shows that the transconductance gradually increases as the TID increases, the subthreshold swing becomes smaller, the subthreshold characteristics deteriorate, and the ON/OFF speed of the device decreases. Figure 3(d) shows that when the thickness of the gate oxide layer is 10 nm, the threshold voltage drift is much smaller than that when the thickness of the gate oxide layer is 20 nm. This also indicates that the TID has less influence on the thin gate oxide device. However, owing to the development of technology for the preparation of ultrathin body silicon-on-insulator (UTB SOI) substrates, a UTB BOX layer (with a BOX thickness of less than 25 nm) is currently rare. Therefore, we only focused on the case of BOX layers of 20 nm thickness.

Table 3
Three bias states in TID simulation.

Offset state	Grid (V)	Source (V)
ON	0.8	0
OFF	0	0
TG	0	0.8

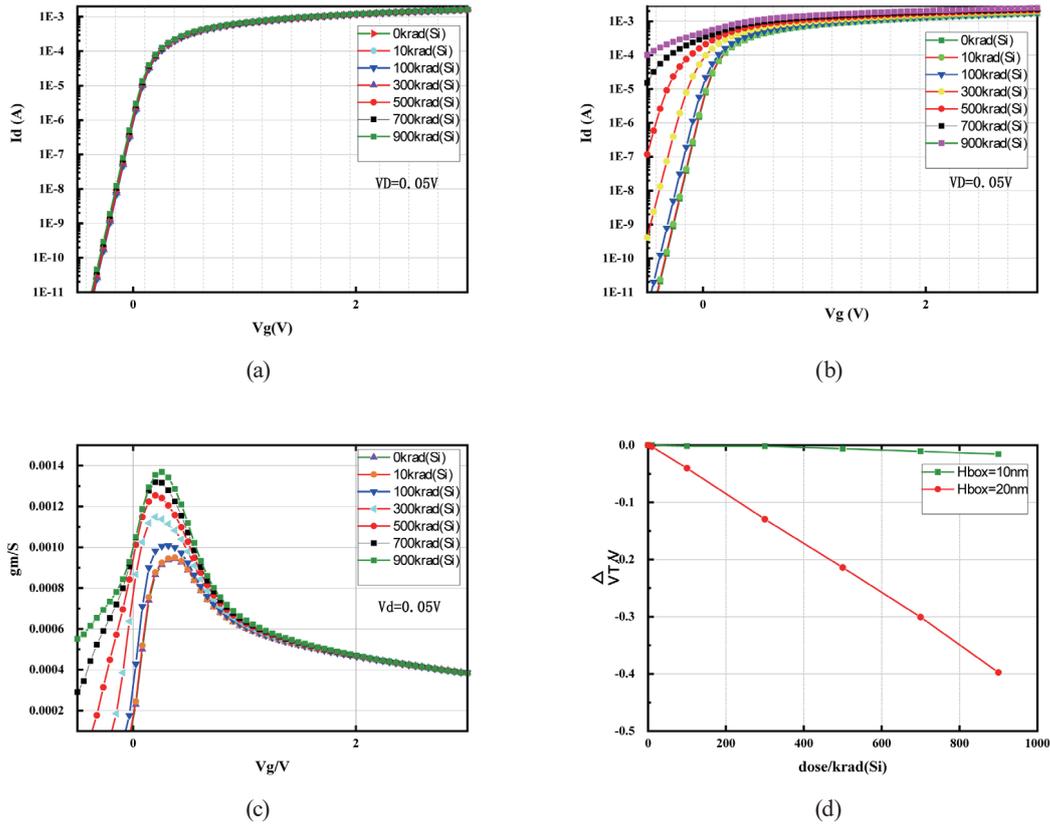


Fig. 3. (Color online) (a) Variation curve of transfer characteristic with TID for $H_{BOX} = 10$ nm, (b) variation curve of transfer characteristic with TID for $H_{BOX} = 20$ nm, (c) variation curve of transconductance characteristic with TID for $H_{BOX} = 20$ nm, and (d) variation curve of threshold voltage drift with TID for different BOX layer thicknesses.

Figures 4(a) and 4(b) show the current density in the channel region in the Y -direction ($X = -0.006$ nm). In the subthreshold region ($V_g = 0.05$ V), the current density in both the forward channel and the back channel increased as the TID increased, but this effect was more pronounced in the back channel. In the saturated region ($V_g = 0.8$ V), the current densities of the positive channel and back channel both increased as the TID increased, but the increase in the positive channel was more pronounced, as shown in Figs. 4(c) and 4(d). This is easy to understand: when the device is in the subthreshold region, the gate voltage is small and only a small number of electrons in the BOX layer can be swept into the vicinity of the positive channel;

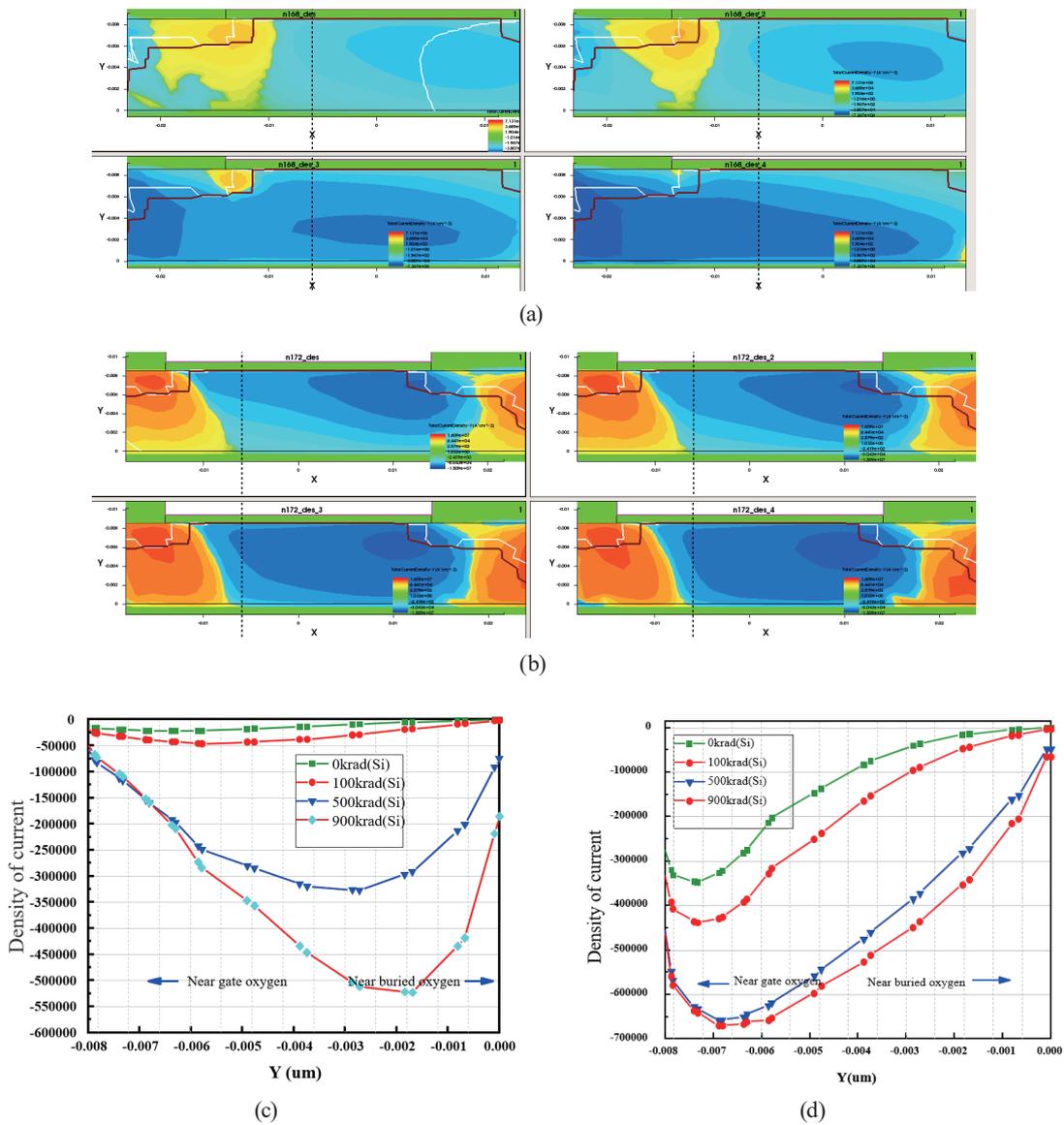


Fig. 4. (Color online) (a) and (b) Channel current density in Y -direction at $X = -0.006 \mu\text{m}$ for $V_g = 0.05$ V. (c) and (d) channel current density in Y -direction at $X = -0.006 \mu\text{m}$ for $V_g = 0.8$ V.

thus, the back channel current density is high. When the device is in the saturated region, the gate voltage is sufficiently large to sweep most of the electrons generated by the BOX into the vicinity of the positive channel; thus, the positive channel current density is high.

As shown in Fig. 5(a), when the device is in normal operation ($V_g = 0.8$ V in the saturated region), the electron mobility at the front-gate channel (0.2 nm below gate oxide) and the back-gate channel (0.2 nm above BOX) changes with the radiation dose, and the electron mobility in the positive channel decreases gradually as the radiation dose is increased, because a large number of electrons are scattered after collision, which results in a decrease in electron mobility. The two ends of the source and the drain are almost unchanged; the electron mobility

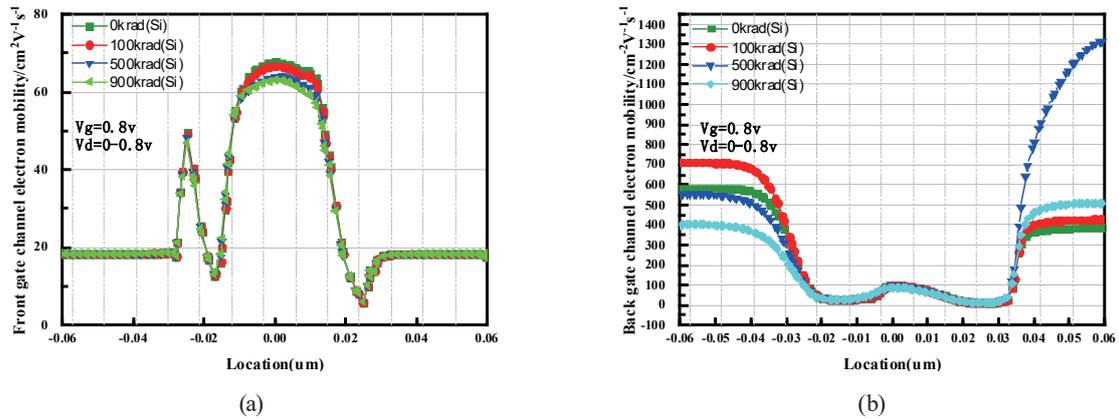


Fig. 5. (Color online) (a) Change in electron mobility with radiation dose at 0.2 nm from the front-gate channel below the gate oxide. (b) Change in electron mobility with radiation dose at 0.2 nm from the back-gate channel above the BOX.

in the back channel is almost zero and does not change, as shown in Fig. 5(b). This is because the electron concentration in the back-gate channel itself is small when the device is under a positive gate voltage. The electron mobility at the source first increases and then decreases with increasing irradiation dose. When the irradiation dose is too large, the electron mobility decreases to less than that before the irradiation, and the drain electron mobility first increases and then decreases. When the irradiation dose is too large, the electron mobility remains higher than that before irradiation. Moreover, the electron mobility at both ends of the source and drain is one order of magnitude higher than that in the positive channel.

3.2 Simulation of total dose effects under different offset states using the activated radiation model

Figure 6 shows that when the dose rate is 200 rad (SiO₂)/s, the corresponding total dose is 10 krad (SiO₂), 100 krad (SiO₂), 200 krad (SiO₂), and 400 krad (SiO₂). The results shown in Figs. 6(a)–6(c) show that when the device has the same dose rate but different total dose, after radiation under three biases, as the total dose increases, the transfer characteristics of the device shift to the left and the TID effect on the device becomes increasingly obvious. Figure 6(d) shows that, under the same radiation conditions, the off-state (OFF-state) threshold voltage drift is the largest and the anti-TID capability is the weakest.

Figures 7(a)–7(c) show the ionized charge distribution induced by the BOX layer of a device under different bias states at a dose rate of 200 krad (SiO₂)/s. The red region in the figures represents areas with high radiation-induced charge. Compared with the ON bias, the higher electric field intensity in the BOX under OFF and TG biases led to the generation of more radiated charge. The trap charge near the interface between the BOX layer and the volume layer below the channel region has the greatest influence on the TID effect of the device. Figure 7(d) shows the distribution of the radiation-induced charge generation rates in the BOX layer along the channel length 2 nm below the interface between the BOX layer and the volume region. The

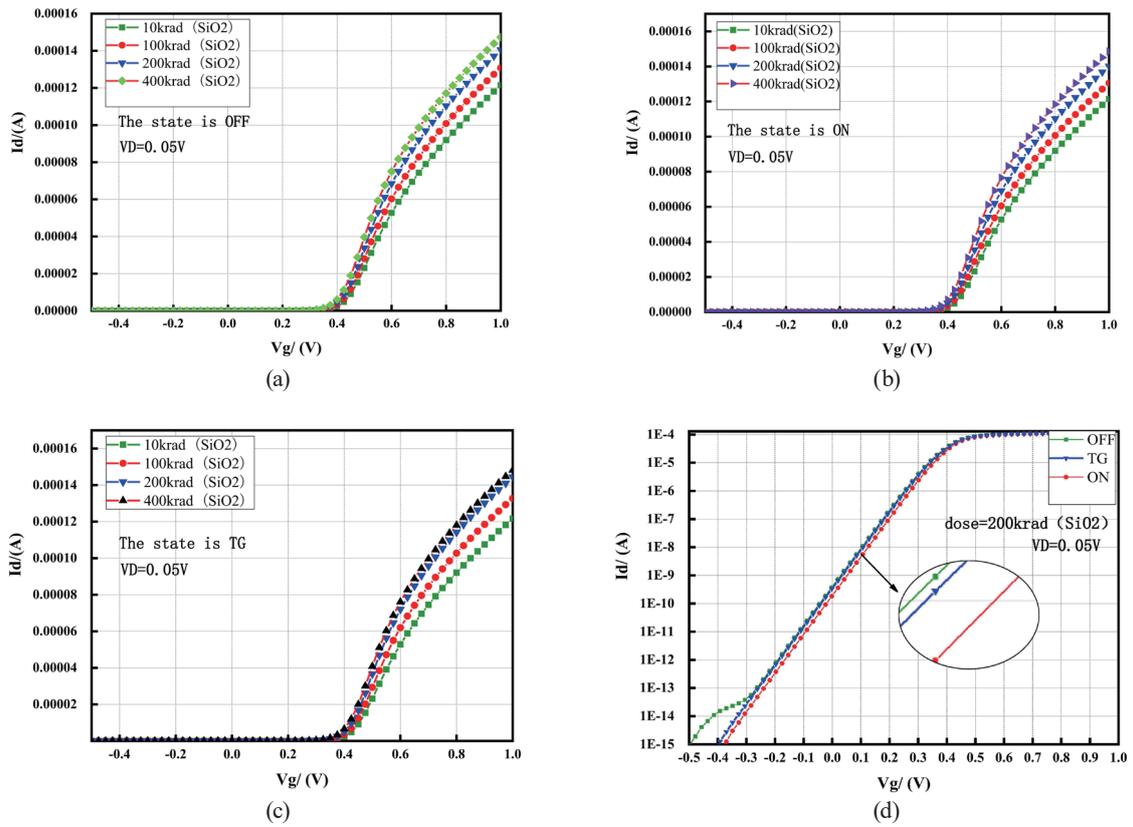


Fig. 6. (Color online) (a)–(c) Variation of device transfer characteristics with radiation dose in the OFF state, ON state, and TG state respectively. (d) Transfer characteristics with the three kinds of offset at a dose of 200 krad (SiO_2).

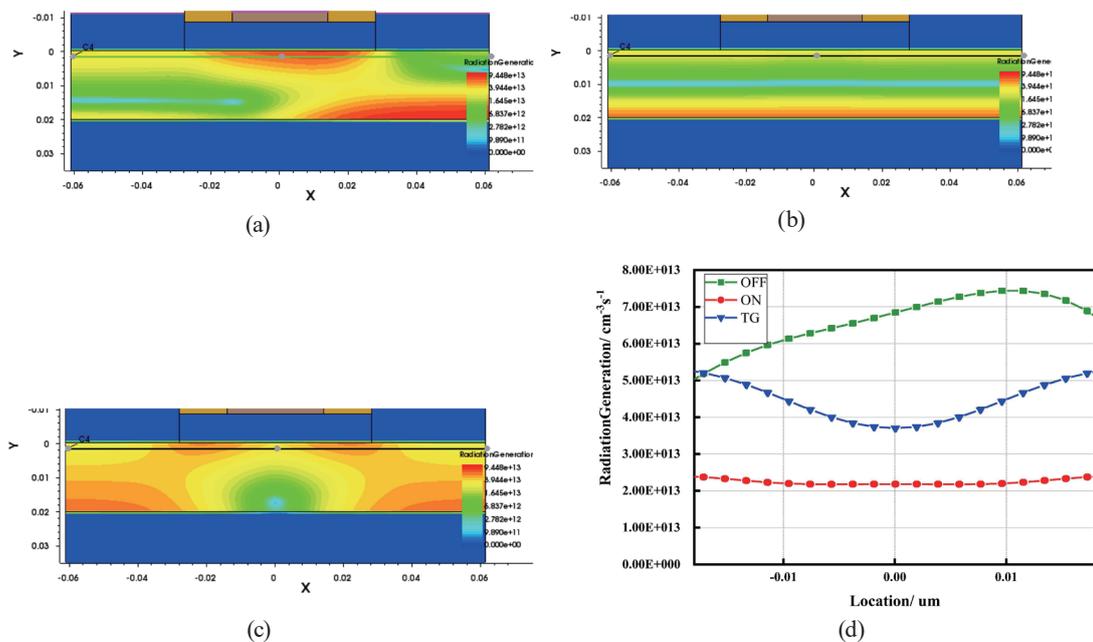


Fig. 7. (Color online) Ionized charge density distribution curves induced by irradiation in the BOX layer for (a) OFF state, (b) ON state, and (c) TG state. (d) Distribution of radiation generation rates along the channel direction 2 nm below the interface between the BOX layer and the body region of the device.

distribution shows that the radiation-induced charge generation rate remains at a high level. Under OFF bias, a large number of trap charges are formed near the interface between the BOX layer and the body region, which leads to the depletion of the back-gate channel. The simulation shows that, for devices with short channels, the OFF bias is the worst bias for mitigating the TID effect of the BOX layer.

Figures 8(a) and 8(c) show that the channel electron mobility of a device degrades as the radiation dose is increased, which is caused by the scattering of a large number of electrons. This result is consistent with that obtained by simulating the TID effect by adding a fixed charge and also reflects the feasibility of the fixed charge model.

Figure 8(b) shows that, at the same radiation dose, the electron mobility of the channel decreases in the order of OFF > TG > ON. This conclusion is the same at any position in the top silicon layer perpendicular to the channel direction, which further reduces the contingency of the result, as shown in Fig. 8(d). This result illustrates that the electron mobility in the transport state is the largest under the same irradiation dose, and the mobility is proportional to the drain current. This confirms the previous conclusion that the OFF state is the worst state for reducing irradiation bias.

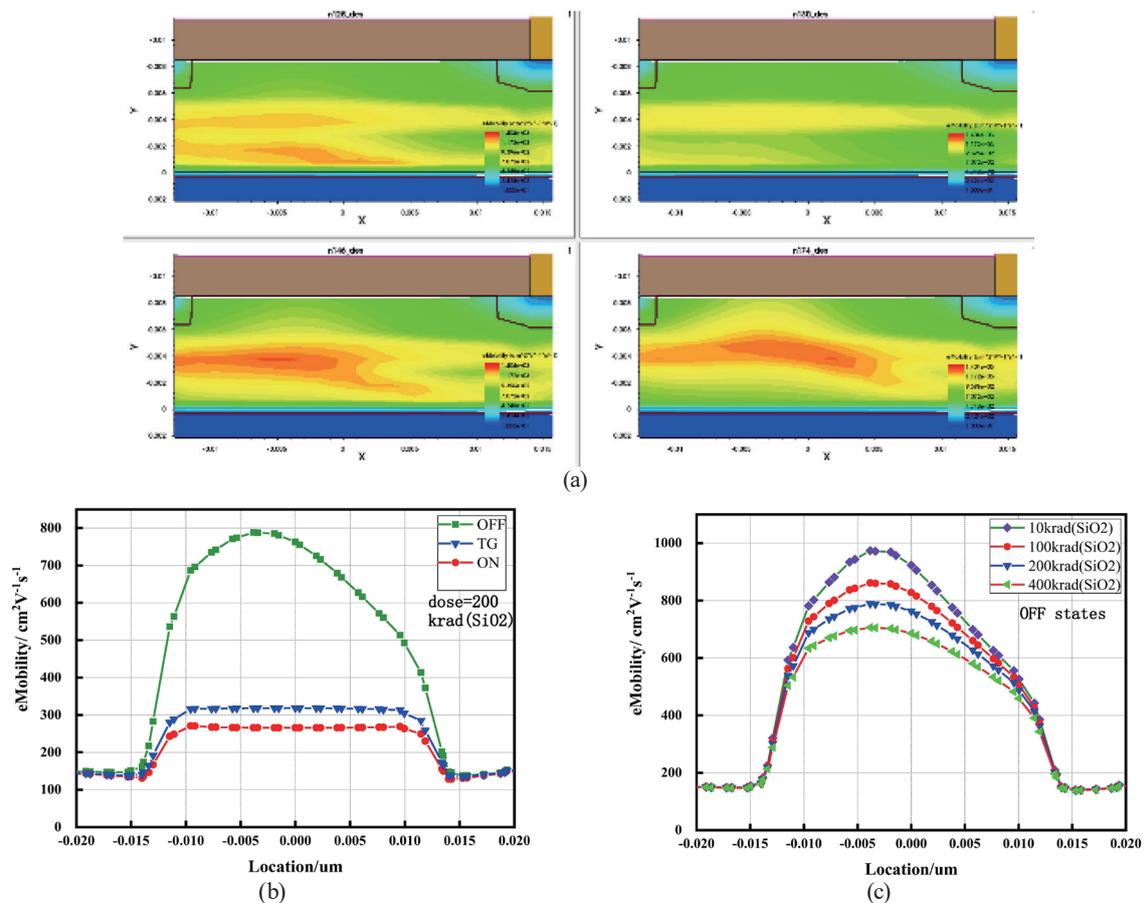


Fig. 8. (Color online) (a) and (c) Electron mobility distribution in the device with different doses of radiation in the channel direction at 2 nm under the interface between the gate oxide and the top layer of silicon during OFF bias. (b) Electron mobility distribution in the device at different bias states in the channel direction at 2 nm under the interface between the gate oxide and the top layer of silicon at a dose of 200 krad (SiO₂). (d) Electron mobility distribution in the device at a dose of 200 krad (SiO₂).

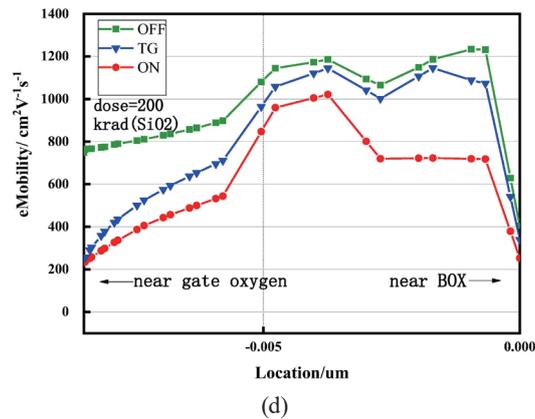


Fig. 8. (Continued) (Color online) (a) and (c) Electron mobility distribution in the device with different doses of radiation in the channel direction at 2 nm under the interface between the gate oxide and the top layer of silicon during OFF bias. (b) Electron mobility distribution in the device at different bias states in the channel direction at 2 nm under the interface between the gate oxide and the top layer of silicon at a dose of 200 krad (SiO_2). (d) Electron mobility distribution in the device at a dose of 200 krad (SiO_2).

3. Conclusions

A 22 nm N-type FDSOI device was built using the process parameters provided by the chip foundry. We investigated the TID of the 22 nm FDSOI device for different thicknesses of BOX layers and bias voltages by simulation.

First, the effects of the TID on the device transfer characteristics, output characteristics, transconductance characteristics, threshold voltages, front-gate and back-gate channel electron mobilities, and channel carrier concentrations were simulated and evaluated by adding fixed charges. The results showed that the thinner the BOX layer of the device, the better the TID radiation-hardening capability of the device. Moreover, as the total irradiation dose was increased, the electron density of the channel increased, indicating a reduced electron mobility of the channel. This degradation occurs because a large number of electrons are generated by irradiation, causing their density to increase, whereas a large number of electrons collide with each other and scatter under bias voltage, resulting in lower electron mobility. Compared with the addition of a fixed charge, the activated radiation model can better simulate the actual radiation effects under different bias voltages.

The tolerance of the device to the TID effect under different bias voltages was simulated using the radiation model. The results of the simulation showed that the tolerance to the TID effect is lowest in the OFF state, followed by the TG state, and the total dose effect is least affected when the device is in the ON state. The models of the two methods in the simulations were different, resulting in a small error in the data obtained from the simulations, but the values were of the same order of magnitude, verifying the feasibility of the two methods.

There are still some defects in this study, such as a failure to establish a more accurate 3D diagram of the FDSOI device structure owing to time limitations and a failure to study the influence of the established shallow trench isolation (STI) on TID. These areas offer opportunities for future research.

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