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Monolithic Three-Dimensional Single-Crystal Silicon Microelectromechanical Systems

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We present two processes for the fabrication of monolithic three-dimensional single-crystal silicon (SCS) microelectromechanical systems (MEMS). They are extensions of the SCREAM (single-crystal reactive etching and metallization) process developed at Cornell. A brief review of the original SCREAM process is followed by the discussion of the multiple-depth and multiple-level extensions of the process, including a metallization and isolation scheme for the three-dimensional MEMS. SCREAM MEMS are characterized by their high aspect ratio, the use of SCS as a stress-free, high-quality mechanical material, and integrated electrical and thermal isolation along the beams and at the beam supports. They are released in a dry RIE release step, which avoids the stiction problems encountered in wet release processes. The multiple-depth and multiple-level, self-aligned processes increase the flexibility in the design of MEMS and allow the fabrication of compact devices with reduced chip area. Complex MEMS and microinstruments are fabricated from a single silicon substrate and thus require no assembly.

1. Introduction

Moving microstructures and microelectromechanical systems (MEMS) have been made from etched single-crystal semiconductors, deposited thin films, and plated metals. Two popular micromachining methods[1] are surface micromachining[2,3] and bulk micromachining.[4-6] Surface micromachining typically uses a thin-film (2 μm) polysilicon layer[1,2] supported by a silicon dioxide sacrificial layer: after patterning the polysilicon layer to delineate the suspended or moving portions of the structures, the sacrificial layer is

removed using a wet chemical etch. The polysilicon-based surface micromachining process has received widespread acceptance for making small (on the order of a few 100 μm on-a-side) microstructures, low-force (<100 μN) actuators and sensors. The major fabrication issues are stress in the deposited thin films, stiction during the wet release step and the limited aspect ratio of the released structures. A second popular approach, bulk micromachining, of single-crystal silicon[1,4,5] or quartz[1,6] uses directional wet chemical etching[4,5] to produce structures and shapes defined by the convolution of the mask pattern and the etch properties of the crystallographic planes. Thus, closely spaced structures with micrometer-scale dimensions or high aspect ratios are difficult to fabricate. Sharp corners defined by the crystallographic planes can contribute to structural failures.

A few more recently developed processes address the aspect ratio limitations of the above approaches: a MEMS process called LIGA[7,8] (a German acronym for Lithographie, Galvanoformung, Abformung) uses X-ray or photolithography to define a mold pattern in a (500 – 600 μm) thick resist layer that is filled by a plating process. Injection molding allows the fabrication of multiple plating molds from this original, high-aspect-ratio metal structure. Sacrificial layer techniques combined with multiple lithography and plating steps allow the fabrication of truely three-dimensional MEMS.[8] The Hexsil[9] process also uses a mold with a silicon dioxide sacrificial layer to form polysilicon structures that are released by removing the silicon dioxide film. A third approach is the SCREAM (single crystal reactive etching and metallization) bulk micromachining process[10,11] developed at Cornell: high-aspect-ratio single-crystal silicon (SCS) suspended microstructures are formed from a silicon wafer using anisotropic reactive ion etching (RIE). The process includes steps to isolate the suspended structures electrically and thermally along the beams and at the supports.[10] It has been used to fabricate a wide variety of complex microinstruments, sensors and actuators.[12] It has been extended to include the fabrication of sharp silicon tips (< 20 nm tip diameter)[13,14] to fabricate a complete scanning probe microscope on a single silicon wafer. In another approach similar to SCREAM, high-aspect-ratio SCS MEMS have been fabricated from silicon on insulator (SOI) wafers[15,16] by deep vertical RIE: the buried silicon dioxide layer provides the etch stop, the isolation of the suspended structures and the sacrificial release layer.

This paper focuses on recent extensions of the SCREAM process for the fabrication of monolithic three-dimensional SCS MEMS.[17,18] A brief review of the history and fabrication sequence of the original SCREAM process is followed by the discussion on the multiple-depth and multiple-level extensions of the process. A metallization and isolation scheme is presented, which requires only a single metallization step to contact all the suspended structure levels. A presentation of some of the devices that have been fabricated using this process is followed by some concluding remarks.

2. Fabrication of Monolithic Silicon MEMS

2.1 *Background*

The precursor process to SCREAM is a process used to make isolated islands of submicron silicon by selective lateral oxidation (ISLO).[19] The ISLO process uses RIE of

SCS to form submicron SCS structures, which are then isolated from the silicon substrate by a lateral thermal oxidation of the bottom portion of the silicon microstructure. The removal of the silicon dioxide from the bottom of the SCS beams, using a hydrofluoric acid release-etch step, generates a MEMS process called COMBAT (cantilevers by oxidation for mechanical beams and tips).[20] COMBAT has been used to fabricate suspended SCS microstructures and integrate nm-scale (< 20 nm diameter) tips on fixed[21] and moving structures.[20] In the SCREAM process, the oxidation and hydrofluoric acid etch steps for structure release are replaced by an isotropic SF_6 RIE.[10] The SCREAM process produces suspended high-aspect-ratio single-crystal silicon (SCS) microstructures that span distances of up to many millimeters.[22] The shapes are independent of the crystallographic directions, so even circular SCS structures can be fabricated.

SCS is a high-quality, stress-free mechanical material and its well-known properties are very suitable for MEMS applications.[23] The high aspect ratio provides a large vertical or out-of-plane stiffness and a large sensor or actuator capacitance. The large vertical stiffness, which is required for released structures of mm-scale to cm-scale dimensions, scales as $(b/l)^3$ where b is the height of the silicon beam and l is the length or span of the beam. The depth of the silicon anisotropic etch step and the amount of undercutting during the release step determine the height b. For SCREAM capacitive sensors and actuators, the capacitance is proportional to the sidewall area of each plate, which is proportional to bl and to the number of plates N. Large sensing capacitors and high-force actuators (>100 mN/cm^2 of silicon at 40 V)[22] have been realized with SCREAM-based processing.

Electrical and thermal isolation of the SCS microstructures is achieved by local thermal oxidation along the beam[10] and at the beam anchors.[10,20] Thermal silicon dioxide exhibits good mechanical properties[24,25] and excellent electrical isolation. A low-temperature process (SCREAM-I) allows the integration of released and movable structures on prefabricated VLSI wafer.[26] Only a few masking layers are required to produce movable microstructures.

2.2 *Fabrication of silicon MEMS by the SCREAM process*

The original SCREAM process flow is shown in Fig. 1. The first step is the deposition or growth of a thick masking oxide on the SCS substrate. The silicon dioxide is patterned using standard optical lithography and RIE (Fig. 1(a)). Pattern transfer to the silicon is accomplished by vertical RIE to produce silicon structures and trenches. The SCS structures are conformally covered by a thermal or chemical vapor deposited silicon oxide layer to protect the patterned structures during the subsequent release step. Aluminum is sputtered onto the structures for use as contacts and interconnects (Fig. 1(e)). A second lithography step before release requires nonconventional trench patterning to remove the silicon dioxide and aluminum from the suspended beam and the bottom of the trench. Finally, an isotropic SF_6 release RIE is used to undercut and separate the SCS structures from the substrate (Fig. 1(h)). The released SCS microstructures are suspended over the substrate and are anchored to the substrate at the ends of the supporting beams or springs (Fig. 2(a)).

A key feature of the SF_6 RIE release step is the undercutting of both the suspended silicon beams and the silicon dioxide coated sidewalls of the silicon trenches. The

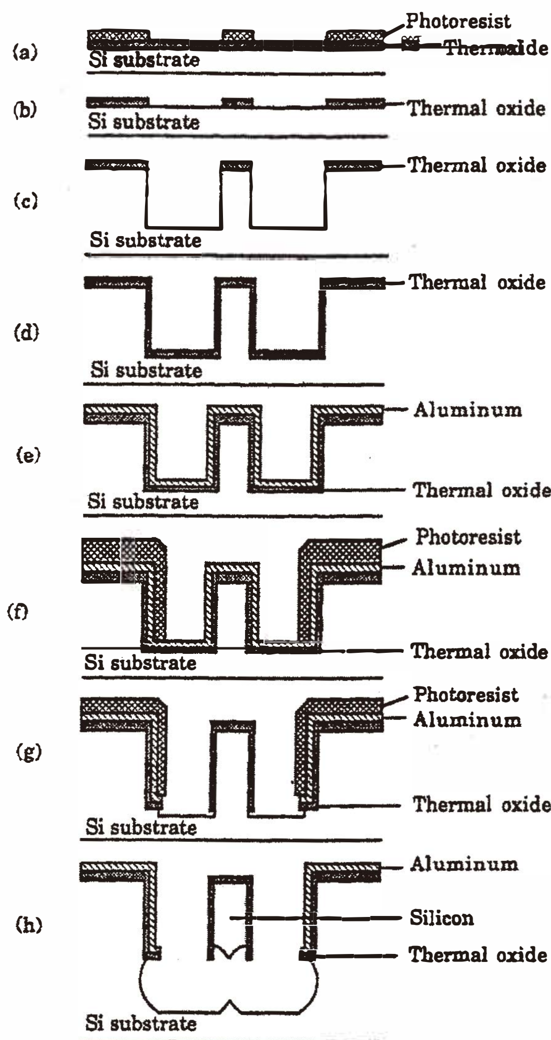
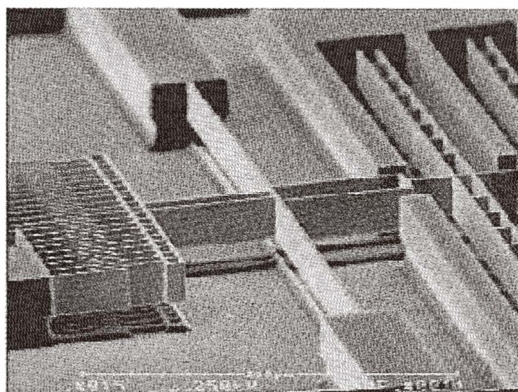
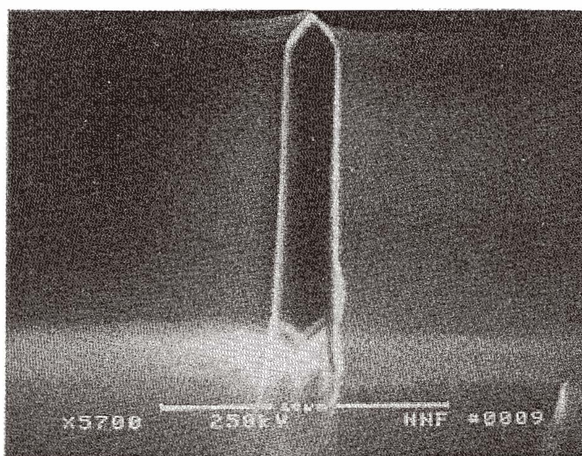


Fig. 1. Fabrication sequence for a basic SCREAM structure.

undercutting of silicon produces an overhang of silicon dioxide that electrically isolates the deposited metal (aluminum) conductor from the silicon substrate (Fig. 2(b)). The SCREAM process shown in Fig. 1 has been further refined to include electrical isolation along the released beam and electrical isolation at the beam support structures. The electrical isolation is accomplished by a local thermal oxidation of thinner beam segments and the beam supports.



(a)



(b)

Fig. 2. SCS MEMS fabricated by the SCREAM process: (a) springs, actuators and sense capacitance plates of a SCREAM accelerometer and (b) cross section of a SCREAM beam showing the SCS core and the oxide overhang.

Another version of the SCREAM process[11] requires a single masking and photolithography step to define the structure. This version of SCREAM, SCREAM-I, has advantages for fabricating simple MEM structures: (1) the second mask-alignment step is eliminated; (2) the metal is deposited in the last process step and does not require patterning; and (3) it is a low-temperature process (< 400°C). Consequently, SCREAM-I MEMS can also be implemented on fully processed VLSI wafers.[26]

2.3 *Fabrication of multiple-depth monolithic silicon MEMS*

The fabrication of SCS structures on a single wafer can be extended to multiple depths.[17] This is accomplished by taking advantage of the features of the deep Si RIE process developed by Bosch.[27] The Bosch process uses alternating etch and passivation steps to achieve a high silicon etch rate, high selectivity and a vertical profile. There are strong loading effects and the etch profile can be tailored by varying the etch and deposition step parameters.

The fabrication sequence is illustrated in Fig. 3. The first few steps (Figs. 3(a) – (c)) follow the original SCREAM process: A 2-μm-thick PECVD (plasma-enhanced chemical vapor deposition) silicon dioxide layer is deposited as an etch mask (Fig. 3(a)) and patterned using photolithography and a CHF_3 RIE step (Fig. 3(b)). This oxide thickness is sufficient to etch 100 μm of silicon (the typical selectivity of silicon to oxide in the Bosch RIE is better than 100:1) and to still leave about 1 μm of remaining mask oxide to protect the silicon structures during the isotropic silicon release etch.

A first deep silicon etch is performed using the Bosch process to a depth of approximately 22 μm. The etch rate, and thus the etch depth, is reduced in narrow trenches due to the aforementioned loading effects. The patterned silicon structure is conformally passivated with PECVD oxide (Fig. 3(c)). After clearing the floor oxide using another CHF_3

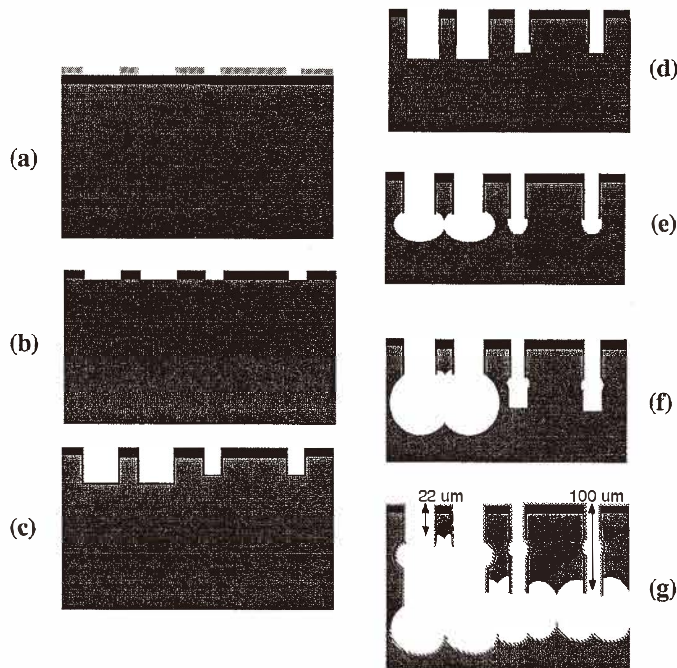


Fig. 3. Fabrication sequence for a two-depth monolithic SCS structure.

RIE, a second deep silicon etch is carried out for an additional 30 μm, resulting in 50-μm-tall silicon structures (Fig. 3(d)). A time-controlled, nearly isotropic SF_6 RIE undercuts the silicon structures by etching the exposed silicon below the PECVD mask on the sidewalls. This step selectively releases the narrow (2 μm) beams of the spring system while the wider (4 μm) beams of the comb fingers and backbone are only partially undercut. The undercutting of the comb fingers is reduced by the lower etch rate in the narrow trenches separating them.

Once the springs are released, a third silicon etch step is carried out for an additional 50 μm, making the 4-μm-wide beams 100 μm tall (Fig. 3(f)). In order to release the movable fingers and the backbone, another layer of PECVD oxide is deposited. After the floor oxide etch, a 30 μm vertical silicon etch followed by an isotropic SF_6 etch is used to release the structures. Finally, aluminum is conformally sputtered for metallization (Fig. 3(g)). As in the original SCREAM process, the electrical isolation is provided by a PECVD oxide overhang. This overhang isolates the sputtered metal from the silicon substrate. The final SF_6 release does not reduce the height of the silicon structures that are already released: the PECVD oxide deposition is sufficiently conformal to also cover the bottom of the released structures and protects the released silicon springs against etching from below.

The first isotropic SF_6 etch step used to release the thinner (2 μm) beams also produces a notch on the wider (4 μm) beams (*e.g.* the comb fingers) that are not released. This notch may lead to a discontinuous metallization of the sidewalls and must be minimized. The loading effect inherent in the Bosch process is used to reduce the undercutting by surrounding the wider beams such as comb fingers with narrower trenches to lower the etch rate.

2.4 *Fabrication of multiple-level monolithic silicon MEMS*

The multiple-level monolithic SCS MEMS are fabricated using a self-aligned process. This process is an extension of the single-level SCREAM[10] and COMBAT processes.[20] All levels are formed from the same silicon wafer by deep RIE of the substrate. After an initial etch mask deposition and lithography step, all levels are fabricated using an identical sequence of steps for each level. A second lithography step (without critical alignment) is used at the end of the fabrication sequence to open up contact windows. All levels are electrically isolated from each other and the substrate and are contacted in a single metallization step. The process has been used to fabricate a number of two- and three-level resonators and actuators as well as electrostatic microlenses and lens arrays.

The fabrication sequence for a two-level structure is illustrated in Fig. 4. The steps used to fabricate the upper-level structures (Figs. 4(a)–(d)) are identical to those of the basic SCREAM process. First, a thick (2–4 μm) silicon dioxide film is deposited and patterned using photolithography and CHF_3 reactive ion etching (Fig. 4(a)). This SiO_2 film serves as an etch mask for a vertical Cl_2 or Bosch RIE of silicon (Fig. 4(b)). Typical etch depths range from 10 to 20 μm. A subsequent thermal oxidation or oxide deposition covers all surfaces with a thin (200–400 nm) oxide layer. An anisotropic RIE removes this film from the horizontal surfaces. Thus the floor oxide is removed while the top of the silicon structures is still covered with the remainder of the first oxide etch mask (Fig. 4(c)). A high-pressure (80–90 mTorr) isotropic SF_6 RIE of silicon then undercuts the masked

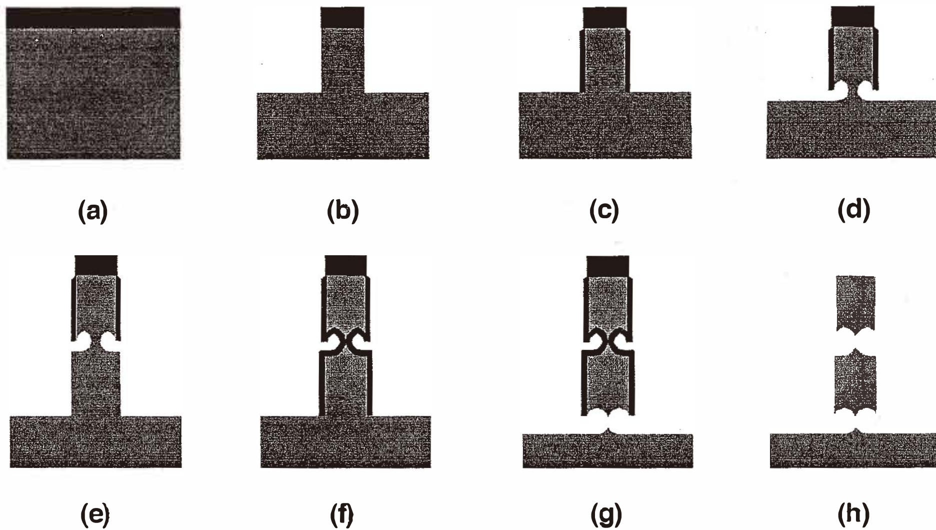


Fig. 4. Fabrication sequence for a two-level monolithic SCS structure.

silicon structures, forming a narrow neck connecting the structure to the substrate (Fig. 4(d)).

The whole upper-level masked silicon structure then serves as a mask for another vertical Si RIE (Fig. 4(e)). The exposed silicon underneath the masked silicon structure is not etched due to the high degree of anisotropy of the etch. The resulting lower-level silicon structure is self-aligned to the upper-level structure, but is slightly wider due to the sidewall oxide deposition. The following thermal oxidation again provides a conformal oxide coat on all surfaces. An anisotropic CHF_3 RIE step removes the oxide from the horizontal surfaces (Fig. 4(f)) — the top of the silicon structures is still covered by the remaining part of the first (thick) mask oxide — and is followed by an isotropic SF_6 RIE to undercut and release the masked silicon structures (Fig. 4(g)). This sequence (Figs. 4(e)–4(g)) is repeated for each additional level.

After the completion of all levels of suspended microstructures, a longer oxidation step consumes the silicon of the thinned neck sections connecting the released silicon levels and the thinnest beam elements. A second lithography step and a wet oxide etch are used to open contact windows on the structures and, if desired, to strip the oxide from some of the elements (Fig. 4(h)). The thick resist required to cover the structures (typically > 20 μm) poses no problem in exposing the large features (>10–20 μm) and the alignment is not critical. The resist forms an etch mask in a wet etch strip of the silicon dioxide. Metal contacts are formed after stripping the resist by the evaporation of aluminum followed by a sintering step.

3. Isolation and Metallization of Complex Monolithic Silicon MEMS

In the single-level SCREAM (and SCREAM-I) process, the sidewall oxide overhang provides isolation of the sputtered metal on the structures. This metal layer forms both the moving and the fixed electrodes — the silicon core of the suspended composite beam is connected to the substrate. This approach no longer works for multiple-level structures as the metal films covering multiple levels are connected at the supports, shorting all levels of suspended structures to each other. Moreover, the high aspect ratio of the narrow trenches in multiple-level structures (*e.g.* between the comb drive fingers) leads to large thickness variations in the sputtered metal film.

For the multiple-level structures, the (highly doped) silicon core of the suspended structures is used as the conducting element. This requires an extension of the isolation scheme developed as a part of the basic SCREAM process: electrical isolation is accomplished by a local thermal oxidation of thinner beam-segments and at the beam supports.

The method of achieving isolation and contacts of two suspended SCS levels using a single metallization step is illustrated in Fig. 5. It shows cross sections of beams of four different widths after completion of the process. The thinnest beam (a) (typically 0.6 μm in the CAD pattern) has been completely consumed by the oxidation on both levels and forms an insulating oxide spacer on both levels. The second (b) is slightly wider (typically 0.8 μm) and has been converted to oxide on the upper level while maintaining a silicon core on the lower level. The third beam (c) is wider again (typically 1.5 μm) and has not been completely oxidized on either level. The undercut etch/oxidation has completely severed the two levels from one another. The last beam (d) is the widest (typically 3.0 μm) and the two levels are suspended above the substrate but connected to one another through a thinned silicon 'neck.'

The electron micrographs in Fig. 6 illustrate how these beams are used to contact two levels of suspended silicon structures while isolating them from the substrate. Figure 6(a) shows the structure to contact the upper level: the two levels of structural beams (1.5 μm

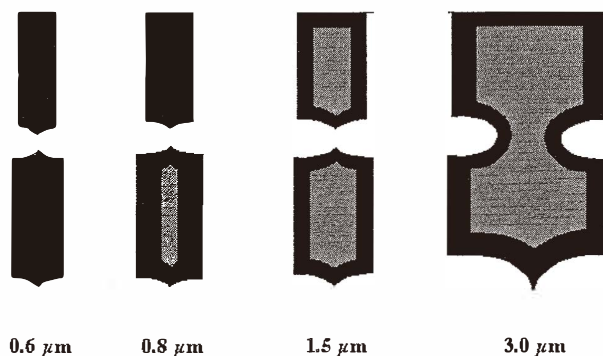


Fig. 5. Two-level isolation scheme: cross sections of two levels of beams of different widths.

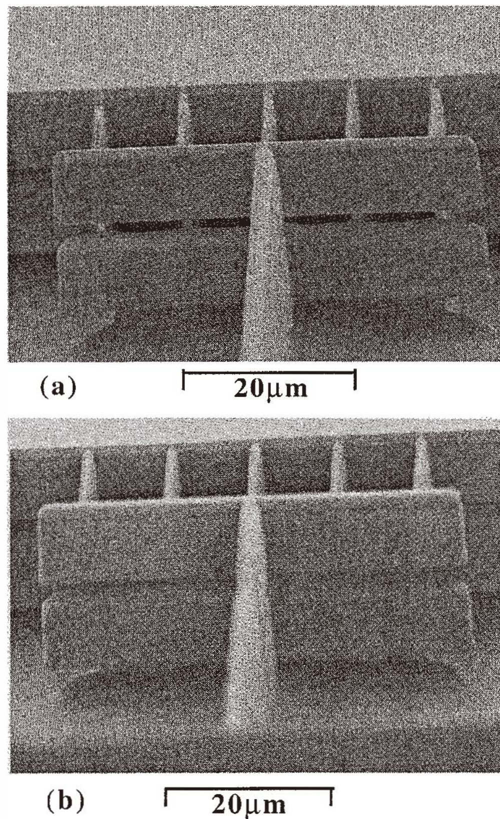


Fig. 6. Contact and isolation for a two-level structure: (a) contact to the upper level and (b) contact to the lower level.

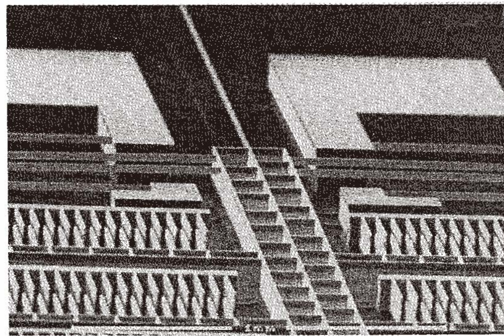
wide) are isolated from one another. They are mechanically connected to and electrically isolated from the substrate through a set of parallel 0.6-μm-wide beams that have been completely oxidized. Figure 6(b) shows the equivalent structure to contact the lower level: a wide (3.0 μm) beam connecting the two suspended silicon levels is electrically isolated from the substrate through the 0.6-μm-wide beams. The connecting 1.5-μm-wide structure beam contains a 0.8-μm-wide segment, which isolates the upper level suspended silicon structure from the 3.0-μm-wide beam.

This contact and isolation scheme can be extended to more than two levels. For a three-level structure, for example, there could be 0.6 μm, 0.8 μm and 1 μm-wide beams to provide the isolation of all three levels, the top and middle levels, and the top level, respectively. Structural elements could be 2 μm wide, with 3-μm-wide beams connecting the top and middle levels, and 4-μm-wide beams connecting all three.

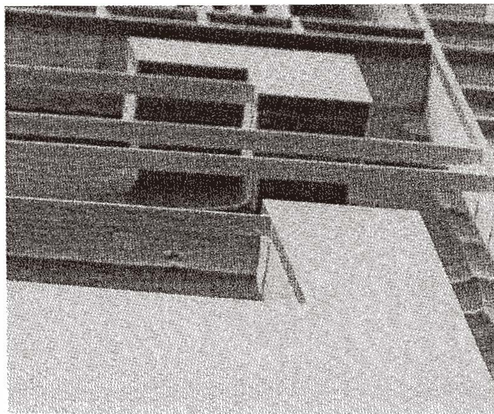
4. Results

Many examples of SCREAM devices and microinstruments have been fabricated and characterized, including a microelectromechanics-based artificial cochlea,[28] a microtribology machine,[29] latching snap fasteners for microassembly,[30] micromanipulation actuator arrays,[31] capacitance-based tunable micromechanical resonators,[32,33] tunable, mm-wave resonators and waveguides,[34] a motion amplifier,[35] a milli-Newton microloading device[23] and a microscanning tunneling microscope.[14]

The multiple-depth process has been used to fabricate large-displacement (close to 100 μm) actuators and xy stages. A two-depth process was used to build comb-drive actuators with 100-μm-tall capacitor plates supported by 22-μm-tall springs. Displacement of 130 μm was achieved for an applied bias of 37V.[17] Figure 7(a) shows the actuator with 100-



(a)

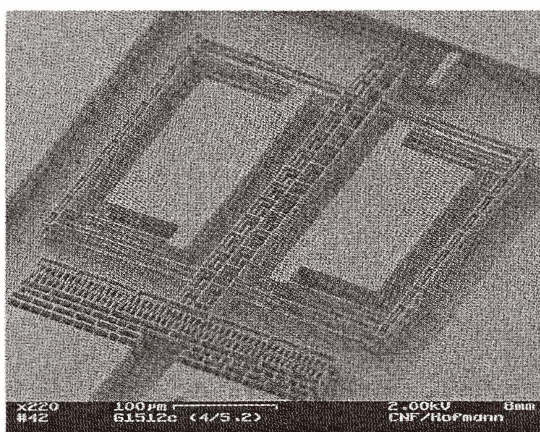


(b)

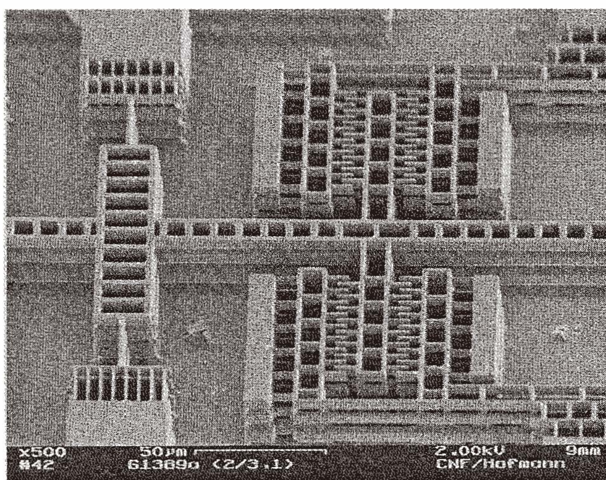
Fig. 7. A two-depth SCS resonator: (a) a 22-μm-tall spring attached to a 100-μm-tall actuator and (b) close-up of the spring and anchor.

μm-tall comb fingers and backbone structure and the 22-μm-tall springs. Figure 7(b) shows a close-up of the springs connecting the structure backbone to the substrate anchors.

The multiple-level process has been used to fabricate a number of two-level and three-level structures. Figure 8(a) shows a two-level linear resonator: the two structural levels are independently movable and the actuator electrodes on both levels are electrically isolated from each other and the substrate. Figure 8(b) shows part of a three-level torsional



(a)



(b)

Fig. 8. Multiple-level monolithic SCS MEMS devices: (a) a two-level linear resonator with independently moving levels and (b) part of a three-level torsional resonator showing the high-force vertical comb-drive actuator.

resonator. The comb actuators consist of three electrically isolated levels of comb fingers that form a novel, high-force vertical comb-drive motor. Non-MEMS examples of multiple-level SCS structures include electrostatic einzellenses and quadrupoles for use in arrayed micro electron sources.[18]

5. Summary

The SCREAM process has been developed to fabricate high-aspect-ratio, suspended silicon structures with micrometer-scale features over large areas — up to 1 cm $\times$ 1 cm. A number of integrated MEMS devices and device arrays have been fabricated using this process, including nested X-Y-Z actuators and other complex MEMS. SCREAM MEMS and microinstruments are characterized by their high aspect ratio, SCS as a stress-free mechanical core material, and integrated electrical and thermal isolation along the beams and at the beam supports. They are released in a dry RIE release step, which avoids the stiction problems encountered in wet release processes.

In this paper, we addressed in particular the recent extensions of the SCREAM process for the fabrication of monolithic three-dimensional SCS MEMS. A brief review of the history and fabrication sequence of the original SCREAM process was followed by the discussion on the multiple-depth and multiple-level extensions of the process. A metallization and isolation scheme was presented, which requires only a single metallization step to contact all the suspended structure levels.

Many of the high aspect ratio MEMS fabricated using the original SCREAM process can also be fabricated using deep etching of SOI wafers down to the buried silicon dioxide layer followed by a wet oxide etch as the release step. This approach, however, cannot produce the three-dimensional monolithic SCS MEMS presented here. The multiple-depth and multiple-level, self-aligned processes increase the flexibility in the design of MEMS and allow the fabrication of novel, complex microinstruments from a single silicon wafer. These three-dimensional structures offer the possibility to produce complex MEMS with reduced chip area. Since these devices are fabricated from the same silicon substrate, no assembly is required.

Acknowledgments

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