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Radiation-resistant Silicon-on-insulator MOSFETs Realized by Neutron Irradiation

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A novel partially depleted (PD) silicon-on-insulator (SOI) structure is realized by a modified process flow highlighting the improved radiation hardness. The key step to modifying the initial SOI wafers is neutron irradiation, followed by a standard post-irradiation laser annealing process that introduces localized traps with a deep level. The deep-level traps in the silicon film act as recombination centers that reduce the minority carrier lifetime effectively. A trap-rich layer is generated near the back interface after the wafer is exposed to neutron irradiation, followed by laser annealing to remove top defects. It is confirmed by simulation and experimental results that the body potential instability in PD devices, which may be introduced by high-electrical-field ionization and the single-event effect, has been efficiently suppressed.

1. Introduction

In the last decades, the silicon-on-insulator (SOI) integrated circuit has boosted its applications over traditional planar silicon ICs in integrated circuit fabrication, particularly in low-power, high-frequency, and high-radiation fields. The feasibility of the SOI process with excellent performance is mainly due to the low cost of SOI wafers with Smart-Cut technology. Generally, parasitic capacitance, sensitive volume, and gate control ability are the intrinsic keys in obtaining the overwhelming advantages.[1,2] Planar and nonplanar SOI technologies also have partially (PD) and fully depleted (FD) types. The PD-type SOI process is easily copied from the same tech-node bulk counterpart. Moreover, the PD-type SOI requires extra designs such as specific effects modeling and device layout design. The FD-type SOI is less sensitive to the charging body effect, whereas silicon film thickness fluctuation and front–back channel coupling probably affect the final device performance.

Since the body potential instability in PD SOI invokes the kink effect, memory effect, and reliability degradation, numerous studies have been conducted to understand the underlying mechanisms and suppress the negative effects. The body potential instability is caused by

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several physical mechanisms: charging of gate tunneling, impact ionization at the strongly reverse-biased junction, and ionizing irradiation of high-energy particles. The supersteep subthreshold region and breakdown characteristics can be significantly degraded. In aviation and space applications, both PD and FD transistors have faced the undesirable parasitic NPN/PNP effect. This effect can probably enhance the transistors' sensitivities to the incident ion effect. External body ties such as T-shape, H-shape, I-shape, and BTS structures are the first solutions to this problem.[3–16] However, the solutions based on body contact require layout modifications and additional lithography masks. Another problem with the body contact scenarios is that the effectiveness of reducing the body potential instability decreases for wide devices with large body contact resistance. Aside from device layout modifications, ion implantation, which creates recombination centers, can also stabilize body potential. However, special ion species such as Ar cannot be realized in a regular process owing to the lack of a species source. As a result, the mentioned solutions suffer from either large area, complex process, or compatibility issues.

Radiation-related defects are traditionally considered to be responsible for device degradation and reliability issues. Specifically, neutron irradiation damage, including transmutation, dislocations, interstitials, and clusters at silicon–oxide interfaces, can affect flicking noise, conducting current, transconductance, and threshold voltage.[17–24] Interface traps at silicon–oxide or surface traps affect the conductivity of the silicon layer according to the results of previous research. Neutrons penetrate the whole silicon film, introducing damage to the full silicon film. The damage-induced traps act as deep-level donor-like and acceptor-like traps. The carrier lifetime is strongly affected by the accumulated damage. Fortunately, traps acting as active carrier recombination centers can be utilized to maintain body potential. In other words, the previous neutral body region with unstable electric potentials can be stabilized through the recombination effect at traps.

A modified SOI body structure with embedded deep-level traps introduced by neutron irradiation and laser annealing is reported in this article. The proposed device highlights the suppression of the body potential instabilities that are strongly related to the parasitic PNP/NPN effect. Traps in a region reduce the minority lifetime locally. The Si^+ as-implanted buried oxide followed by annealing is embedded with silicon nanocrystals, which stop interface trap formation during neutron irradiation. Therefore, the parasitic back-channel path rarely forms during post-irradiation. At the same time, the coupling effect between the front and back channels is alleviated to a considerable extent. The proposed novel structure suppresses the coupling caused by total dose radiation and the transient effects caused by heavy ion radiation.

2. Proposed Device Fabrication Flow

In this work, MEMS processes including patterning, etching, and deposition were applied during the device fabrication. Specifically, nMOSFETs were realized in a 0.13 μm PD SOI platform, where STI isolation and $CoSi_2$ silicide side-wall etching were applied. The initial wafer specifications were a 200-mm-thick Smart-Cut wafer, a 100-nm-thick top silicon, and a 145-nm-thick buried oxide (BOX) layer. The final gate oxide (Gox) thickness after oxidation and

chemical mechanical polishing (CMP) was about 6 nm. The Si film was thinned to 90 nm because of sacrificial and gate oxidation. Control devices were fabricated without body ties, whereas the H-shape gate contact was fabricated for comparative samples.

A combined process wherein comparative samples were fast-neutron-irradiated and laser-annealed was introduced for devices without body ties. In this way, radiation damage or traps were introduced locally within the lower region of the top Si film. The initial SOI wafers were treated by multiple-step Si implantation and post-implantation rapid thermal annealing, as demonstrated in our previous study.[25,26] As a result of Si implantation and annealing, Si nanocrystals with large electron capture cross sections were created within the Si–BOX interface. Transistors fabricated with the Si implantation hardening process have been shown to be tolerant to a 3.0 Mrad (Si) radiation dose. The neutron energy in this radiation work reached 14.2 MeV. The irradiation dose of neutrons for this work varied from 10^{14} to 5×10^{15} n/cm^2. According to Ref. 23, the minority carrier lifetime follows the relationship

$$\frac{1}{\tau} = \frac{1}{\tau_0} + \frac{\Phi}{K_{gn}}, \tag{1}$$

where τ represents the post-radiation lifetime, τ_0 is the pre-radiation lifetime, and K_{gn} is the radiation damage factor and is assumed to be 8×10^6 s/cm^2. Assuming that the initial lifetime is 1.0 μs, the calculated final minority carrier lifetime is 0.4 μs, which is a decrease of 60%. Another important result caused by neutron irradiation is the recombination rate at the Si–BOX interface:

$$s(\Phi) = s(0) + \Phi / k_{sn}, \tag{2}$$

where $s(\Phi)$ and $s(0)$ are the recombination rates at the neutron irradiation doses Φ and 0, respectively. k_{sn} represents the introduced radiation damage coefficient. In our case, k_{sn} was assumed to be 2×10^{12} s/cm^3 for n-type silicon and 4×10^{12} s/cm^3 for p-type silicon. The overall results of neutron irradiation originate from two sides, damage in the silicon film and that at the SiO_2–Si interface.

To introduce traps or damage to the silicon film locally, it is critical to select the proper laser annealing parameter, i.e., laser source (laser wave), annealing step size (sweeping speed), and annealing power. In consideration of the required damage distribution in silicon film and film thickness, the Q-Switched Nd: YAG laser was chosen to perform the silicon annealing. The laser wavelength is ≈1064 nm, which corresponds to 1.17 eV photon energy, which is close to the silicon bandgap. In this case, the photons were easily absorbed and transformed into heat immediately since the relaxation time was neglected. The final critical parameters were determined as 4 W average power, 3 cm/s x-axial scanning speed, and 30 μm y-axial scanning step, where the laser spot diameter was intrinsically 40 μm. The average annealing depth reached ~50 nm with ~35.4 nm silicon film left, as shown in Fig. 1. Thus, the sheet resistance was reduced to 13 Ω/□ from ~10^5 Ω·cm before neutron irradiation, which implies that the upper

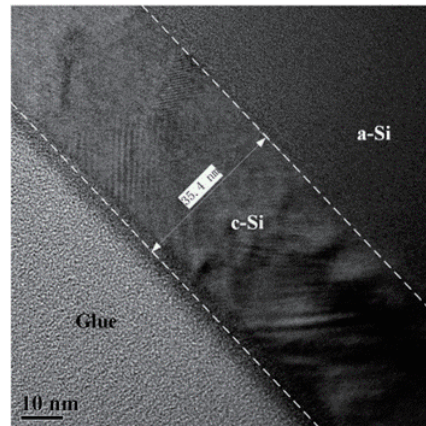


Fig. 1. HRTEM image of mono/amorphous Si structure of silicon film.

part of the silicon film became monocrystalline after laser annealing. Figure 1 shows the HRTEM image of an annealed sample.

The control devices and devices with modified SOI substrates were then manufactured with a commercial 0.13 μm SOI platform. After front-end fabrication, the samples were packaged in dual in-line package (DIP). The total irradiation dose (TID) experiment was performed at the Xinjiang Technical Institute of Physics & Chemistry, Chinese Academy of Sciences. The TID source was a ^{60}Co nuclear radiation source, and the samples were irradiated with a 200 rad (Si)/s dose rate. The devices were biased in the OFF mode during the irradiation experiment because the radiation performance can be evaluated properly in the OFF mode. In this mode, front gate and source terminals were grounded, and the drain terminal was biased at 3.3 V. After the irradiation experiment, device curves were determined within 20 min based on IV sweeping.

Cross-sectional illustrations of the SOI structure without body contact and the proposed neutron-hardened (NH) SOI structure are shown in Fig. 2. There is a thin silicon layer in the lower half of the top silicon film in the NH SOI device, as shown by the black dots in Fig. 2(b). Considering the n-type MOSFET, the majority holes in the body are created by high-field carrier generation, thin oxide quantum tunneling, and single-event effect flow into the neutral body. In the next step, the excess holes disappear because the hardening process creates traps, and interface states serve as recombination centers. The process flow of FB SOI and NH SOI nMOSFETs is described in Refs. 15 and 16. In addition, the trap-rich layer was also created initially beneath the source and drain regions. The additional neutron irradiation before the threshold voltage adjustment implant was achieved directly without additional masks. The laser annealing only treats the upper half of the entire wafer with careful selection of the process parameters. Therefore, the S/D regions were not completely thermally recovered. The key commercial 0.13 μm SOI platform parameters are listed in Table 1.

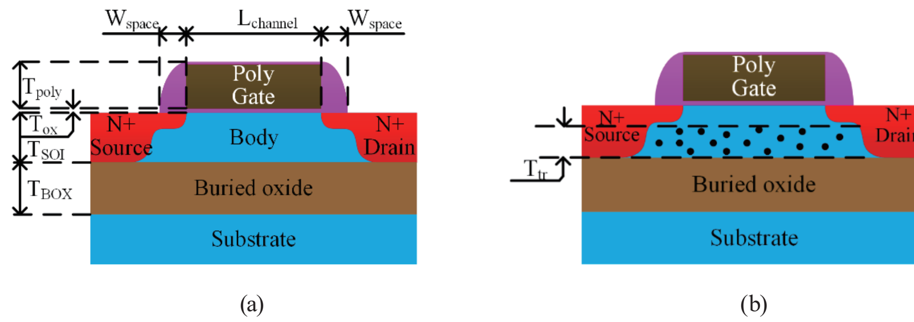


Fig. 2. (Color online) SOI device structures: (a) without body contact and (b) with trap-rich region.

Table 1
Typical parameters of SOI structures.

Parameter	Description	Value
$L_{channel}$	Channel length	350 nm
T_{SOI}	Thickness of Si film	90 nm
W_{space}	Width of spacer	65 nm
T_{poly}	Thickness of poly gate	130 nm
T_{ox}	Thickness of gate oxide	6 nm
T_{BOX}	Thickness of buried oxide	145 nm
T_{tr}	Thickness of trap-rich layer	≈60 nm
NNS	Doping of N+ source/drain	≈1 × 10^{20} cm^{-3}

3. Simulation Evaluation

3.1 Process simulation

The Sentaurus TCAD simulation toolkit was used to simulate the process and electrical behaviors.[27] A rigid calibration was successfully intrinsically conducted using the TCAD simulation toolkit based on SIMS experimental data. Advanced adjustment was applied to precisely simulate the SOI and hardening processes. Process simulation procedures were based on reliable published data and were referenced to our previous research.

The trap-rich region was defined directly in the SOI layer instead of using the real neutron irradiation and laser annealing process in the simulator. Otherwise, direct simulation of neutron irradiation and laser annealing is hardly practicable owing to the complexity and simulation accuracy. Thus, the trap density and carrier capture section were determined by both the experimental results (i.e., HRTEM images) and theoretical calculations. The 2D device structure and doping profile for a 0.35 μm NH SOI nMOSFET are shown in Fig. 3.

3.2 Device simulation

The device electrical characteristic simulation tool Sdevice was applied in the IV and transient simulation research. Basic device simulation models including mobility, carrier velocity, SRH, and the Auger carrier recombination model were implemented. As for the strong

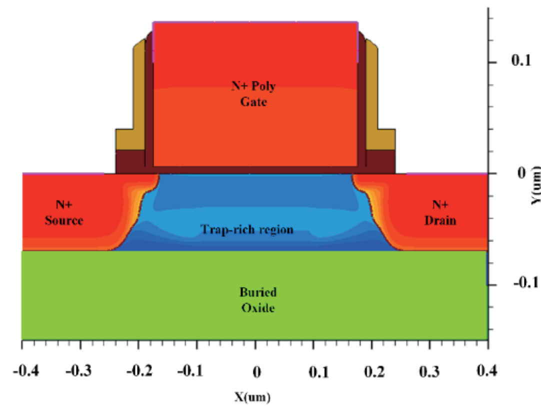


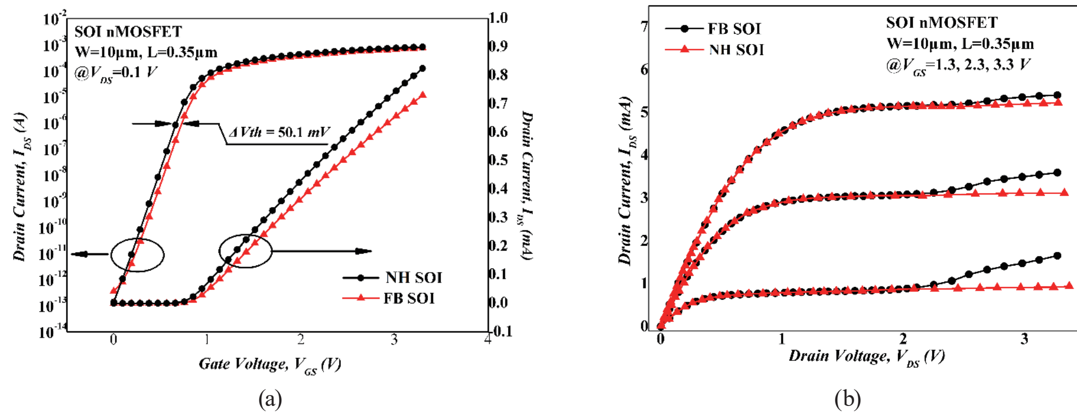
Fig. 3. (Color online) 2D device structure and doping results of NH SOI nMOSFET.

electrical field ionization, the Lackner avalanche model was used. For deep sub-micrometer SOI devices, neither internal nor external characteristics can be precisely simulated using the traditional carrier dynamic model. We applied the hydro model, which is recommended in the TCAD toolkit manual, in the device electrical characteristics simulation instead of the drift-diffusion model. Figure 4(a) shows the I_{ds}–V_{gs} characteristics of NH SOI and FB devices simulated using the TCAD tool. Data curves were plotted in both logarithmic and linear coordinates to show the subtle differences in the subthreshold region. It is known that the neutron-related transmutation doping effect changes the doping concentration, resulting in the increase in the front-channel doping concentration. Although the peak value was set above the Si–BOX interface and laser annealing removed the top defects, the transmutation effect still cannot be ignored. The neutron transmutation doping effect lowers the P+ doping level and V_{th} [Fig. 4(a)]. In Fig. 4(a), the NH SOI device shows 53 mV V_{th}, which is lower than that of the device without body ties. At the same time, the saturation I_{ds} was 0.15 mA lower for the NH SOI device. Figure 4(b) shows that kink effects were well controlled in the NH SOI device.

4. Discussion

4.1 Breakdown characteristics analysis

The BUSFET structure was first used in the attempt to realize a radiation-immune SOI device structure.[28] In this structure, the asymmetric source–drain structure was introduced, where the source junction did not touch the BOX. This created a noncontinuous back channel that stopped the formation of a conducting current channel. With this clever design, the BUSFET was resistant to ionizing radiation. Another recently proposed novel-structure TDBC SOI has been discussed in detail.[29] The source PN junction was changed to a tunneling junction, which can be turned on at a low forward voltage. Although the TDBC structure exhibited strong radiation immunity, it had subthreshold abnormality owing to edge leakage. Another key issue is that a lightly doped body arises from the front–back interconnection. Devices exposed to ionizing radiation show the phenomenon that back-channel charge can easily impact the front-



(a) (b)

Fig. 4. (Color online) (a) I_{DS}–V_{GS} curves of NH SOI and device without body ties. (b) I_{DS}–V_{DS} curves of NH SOI and device without body ties.

channel electrical characteristics. An alternative method to solve this problem is to introduce an extra doping level at the Si–BOX interface. Overall, this can be realized even with the same mask steps as those in the common SOI device flow. The final device structure maintains the original S/D symmetry without the need for other careful considerations during IC design.(25)

Generally, BV_{dss} is referenced as the drain breakdown voltage where the drain current reaches a certain criterion. Since the doping profile of hardened devices has been altered, the breakdown characteristics should be investigated thoroughly. As shown in Fig. 5, BV_{dss} was extracted for FB, H-body contact, and 10-μm-wide NH SOI devices with various gate lengths. The parasitic bipolar amplification effect dominated the BV_{dss} reduction of FB SOI devices. A small H-shape device exhibits a reduction of breakdown voltage, whereas a long-channel H-gate SOI device shows improved BV_{dss} characteristics. As the channel length of H-gate SOI MOSFETs is scaled down, the narrow channel resistance increases, preventing majority flow out. Thus, the parasitic bipolar amplification effect can be magnified. Unfortunately, the drain breakdown voltage performance of the NH SOI device worsens. This degradation can be inferred from the extra doping level at the Si–BOX interface. A heavily doped body naturally forms a body-drain PN junction with both heavily doped sides, which easily reduces the final breakdown voltage. As a result of the extra doping level, the drain leakage current is enhanced, which can also exacerbate the relative parasitic NPN effect and reduce the BV voltage.

4.2 TID radiation response

Figure 6 shows the pre- and post-radiation transfer characteristics of the H-shape SOI device at V_{DS} of 0.1 and 3.3 V. V_{th} changes of −82 and −111 mV can be observed at V_{DS} = 0.1 V at radiation doses of 300 and 500 krad (Si), respectively. Notably, SS decreased after irradiation, where the calculated SS values were 86 mV/dec pre-radiation and 74 mV/dec post-irradiation. The off-state leakage remained unchanged with the radiation dose of 500 krad (Si) with normal current fluctuation of pico-ampere order. However, a supersteep subthreshold can be observed in Fig. 6(b), regardless of pre- or post-radiation at a high drain voltage. In extreme cases, the front gate lost its turn-off controllability when the radiation dose reached 1 Mrad (Si) and the drain current became as high as 6.5×10^{-5} A.

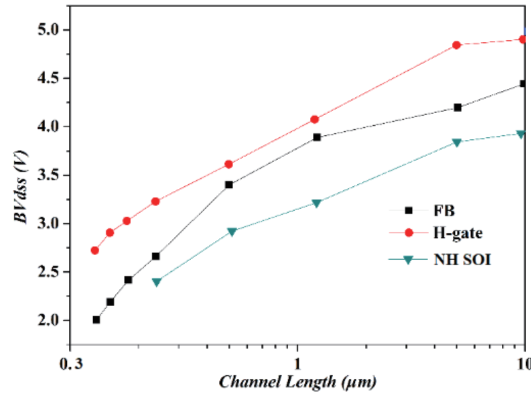
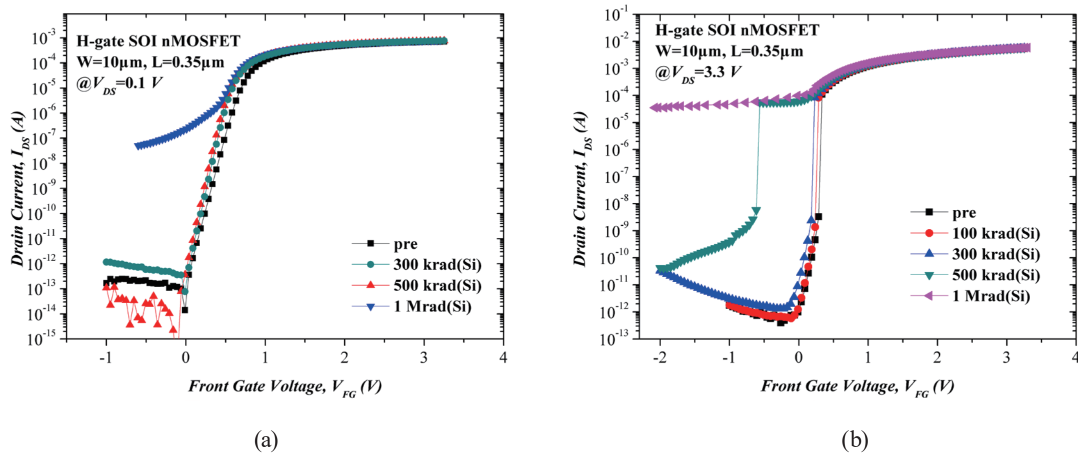


Fig. 5. (Color online) Breakdown voltages of FB, H-body contact, and 10-μm-wide NH SOI devices.



(a) (b)

Fig. 6. (Color online) I_{DS}–V_{FG} characteristics at (a) V_{DS} = 0.1 V and (b) V_{DS} = 3.3 V of H-shape device.

The post-radiation-induced edge leakage current can be ignored in the edgeless H-gate SOI MOSFETs. Therefore, the clear I_{DS} off-state current and *SS* shift are probably due to the front–back interconnections.[30,31] By the method introduced in Ref. 32, N_{ot} and N_{it} are separated and extracted, which can help us to understand the underlying mechanisms. Following the previous calculation procedure, the net charges in BOX $Q_{net} = q(N_{ot} - N_{it})$ are 1.3 × 10^{12} and 1.4 × 10^{12} cm^{-2} at 500 krad (Si) and 1 Mrad (Si), respectively. Notably, the front and back depletion regions expand with increased gate voltage and accumulated TID and finally come into contact with each other. Then the PD device transfers to the FD mode when

$$X_d + X_b > t_{si}\,. \tag{3}$$

X_d and X_b are the maximum widths of the front and back depletion regions, respectively, and t_{Si} represents the silicon film thickness. X_d can be expressed as

$$X_d = \sqrt{\frac{2\varepsilon_s(2\phi_b)}{qN_A}}. \quad (4)$$

N_A is the front-channel doping level, Φ_b is the Fermi potential of the SOI body region, and ε_s is the Si permittivity. X_b was calculated using the definition

$$\frac{Q_{net}}{qN_{bg}}. \quad (5)$$

N_{bg} represents the doping level at the Si–BOX interface. By applying $N_A = 4.3 \times 10^{17}$ cm^{-3}, X_d was calculated to be 51 nm, wherein X_d was 26 nm and 27 nm at 100 krad (Si) and 500 krad (Si), respectively. It is clear that the device transferred from the PD mode to the FD mode at 100 krad (Si), since the total depletion region thickness surpassed the Si film thickness. The trapped charge at the back interface would reinforce the front electrical field through coupling, thus lowering the normal threshold voltage. Figure 6(b) shows an abnormal steep *SS* even at pre-radiation at a high drain voltage. This abnormal phenomenon can be explained by the aforementioned parasitic NPN/PNP effect.(24) The basic mechanism can be explained as follows. Impact ionization at a high drain voltage induced charge, elevating the body potential, which then caused the source PN to turn on. As a result, the emitter-base forward biases and the parasitic NPN/PNP transistor operated in the amplification region. This amplification effect finally caused an uncontrolled current boost. N_{ot} in the BOX in the buried oxide region increased the body potential, which decreased the onset level of the amplifying effect.

As shown in Fig. 7, a 10 µm/0.35 µm NH SOI device at low and high V_{DS} exhibited tolerance to high radiation levels. From Eq. (4), it is clear that a higher bulk doping level induces a smaller depletion width. By applying $N_{bg} = 2.4 \times 10^{20}$ cm^{-3}, the calculated back- channel X_d was about 3.3 nm. The 1.3 and 1.5 nm back-channel depletion region widths were obtained at the other two radiation doses. The NH SOI device had a doping concentration at the front channel similar to

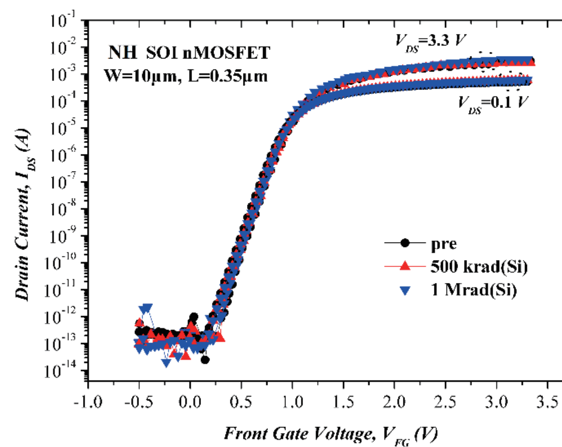


Fig. 7. (Color online) I_{DS}–V_{GS} curves of 10 µm/0.35 µm NH SOI device at different TID levels.

that of the normal device; therefore, the total maximum depletion region width comprising the front and back channels was 53 nm. Consequently, the NH SOI device was tolerant to the ultra-TID level where I_{off} and the thin Si film interconnection effect can be totally suppressed. The radiation-related loss of the front gate turn-off controllability at high V_{DS} also recovered.

4.3 Single ion strike simulation study

Breakdown characteristics and total dose radiation response have been discussed experimentally above. Unfortunately, single-event transient response comparisons between different SOI structures could not be realized through device simulation owing to the lack of necessary experimental equipment. However, it is believed that TCAD simulation can also provide insight into the single-event radiation response differences between different device structures. The effect of incident ions was studied by applying the single ion track module in the Sdevice simulation tool. The incident ion effect in the single event effect (SEE) module can be simulated by applying a certain amount of free carriers in a certain column region. In detail, the Gaussian radial carrier distribution was selected in the model. The specific radius was set as 0.05 μm. Meanwhile, the specific time was fixed at t_0 = 50 ps. In other words, the corresponding LET value was changed to be 0.1 pC/μm in accordance with the relationship 1 pC/μm ≈ 100 MeV·cm^2/mg. The incident angle of the incident ion was assumed to be 0°, which means that the incident track is vertical to the Si surface. During the ion irradiation, all the devices were biased in the OFF mode, i.e., V_{DS} = 3.3 V and other electrodes were grounded.

The drain current [Fig. 8(a)] and collected charge [Fig. 8(b)] are shown with a defined 20 MeV·cm^2/mg LET at different incident locations for the FB SOI nMOSFET. The same simulation curves are also shown in Fig. 9 for the NH SOI MOSFET. As shown in Figs. 8(a) and 9(a), it is clear that the current curve has a rising stage before t_0 + 10 ps, followed by a dropping stage after the peak value. The rising stage represents the initial separation stage of electron–hole pairs. The peak value of the drain current is for incident ions closer to the drain PN junction, which indicates more e–h pairs escaping from recombination. After t_0 + 10 ps, the current curve represents the dominant parasitic bipolar amplification of the injected charge. It can be concluded that the prompt current was first affected by carriers created by ionized particles, and then by impact ionization. It is important to note that the drain current decay lasted 1.1 ns for the FB nMOSFET, whereas it was 0.1 ns in the case of NH SOI devices. Furthermore, Fig. 8(b) shows that the total collected charge remained unsaturated owing to the body potential instability at different ion incident locations. For example, the FB device continues to collect drain charge at a relatively low I_{DS} at 1 ns. The total drain charges $Q_{collected}$ at 1 ns were 56.1, 94.4, 101.3, and 101 fC; however, at 10 ns, they were equal to 102.2, 153.2, 157.5, and 159 fC for x = 0.3, 0.0, 0.2, and 0.1 μm, respectively. Nevertheless, for the NH SOI device at 2 ns, the total collected charges saturated as 8.0, 10.0, and 13.0 fC. As expected, this saturation effect indicates that the body potential instability has been reduced in NH SOI devices. The total collected charges at 2 ns were 8.2, 10, 12.8, and 13.5 fC, and at 10 ns, they were 9.2, 11.0, 14.4, and 14.7 fC for x = 0.3, 0.0, 0.2, and 0.1 μm, respectively. In the NH structure, the total collected charge increased by only 13.5, 13.3, 10.3, and 9.8% from 1 to 10 ns, whereas in the FB devices, it increased by 85.0, 64.5, 52.1, and 57.8%, respectively.

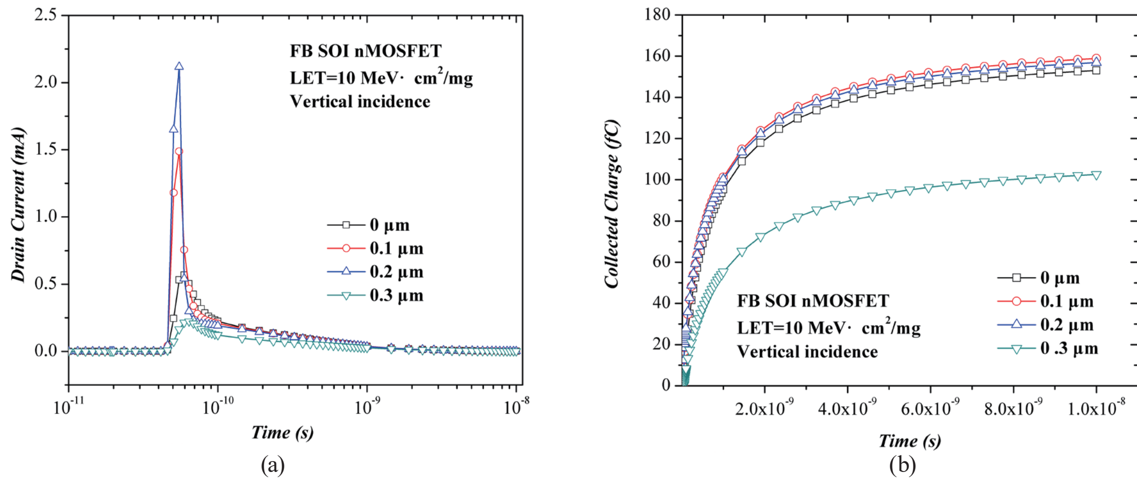


Fig. 8. (Color online) Current and collected drain charge versus incident time with LET = 20 MeV·cm^2/mg of FB SOI n for different incident positions (cf. Fig. 3).

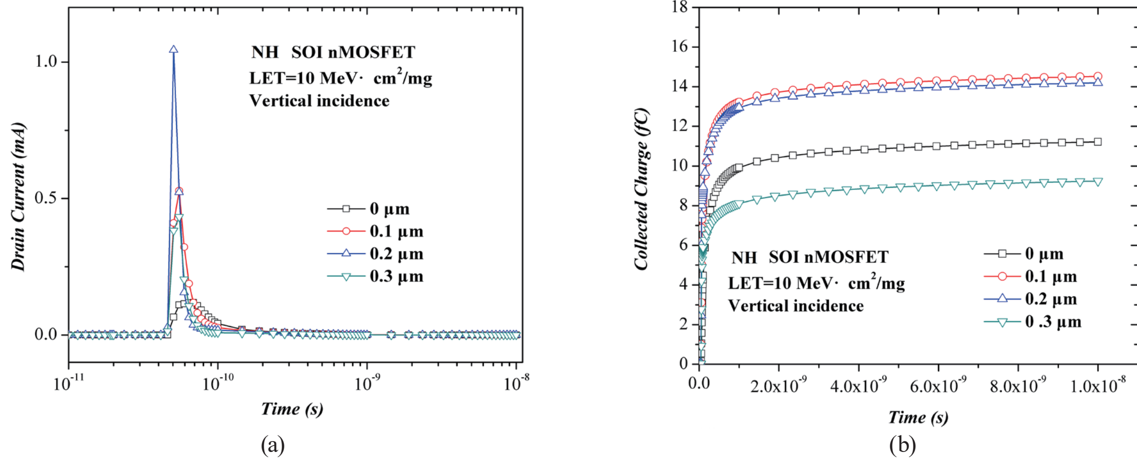


Fig. 9. (Color online) Simulated I_{DS} and $Q_{collected}$ evolution for ion LET = 20 MeV·cm^2/mg of NH SOI device at different incident positions.

Here, we define a parameter to describe the bipolar amplification $\beta_{HI.}$ For the single ion incident, it is defined as

$$\beta_{HI} = \frac{Q_{collect}}{Q_{dep}}. \quad (6)$$

Figure 10 shows the bipolar gain β_{HI} versus the ion incident positions for FB and NH SOI devices. $Q_{collect}$ is the total drain collected charge; the collected time here was set as 10 ns in this work when I_{DS} saturated.

Figure 10 shows that the bipolar gain of the NH SOI device was much smaller than that of the FB counterpart at any incident coordinate. Both transistors showed a peak bipolar gain at $x = 0.1$ or 0.2 µm. This is because the lightly doped drain (LDD) region locates near the drain pn

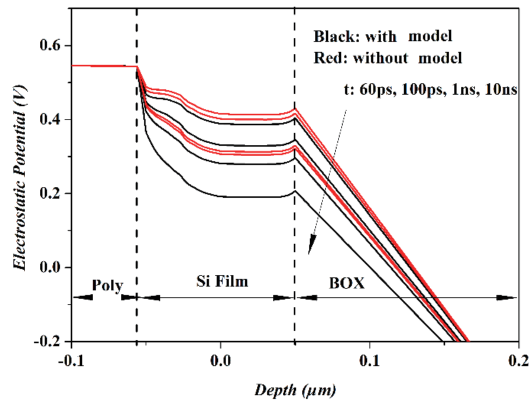


Fig. 10. (Color online) β_{HI} of FB and NH SOI devices versus ion incident position.

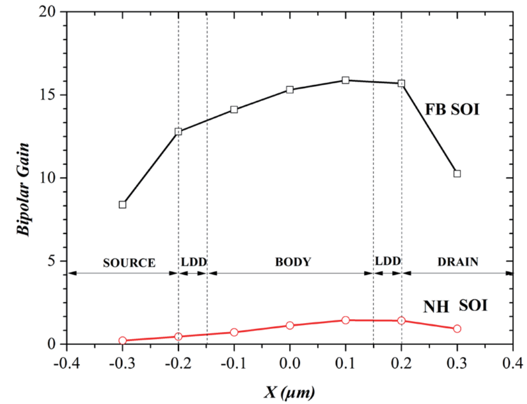


Fig. 11. (Color online) Silicon electrical potential distribution versus depth for the NH SOI devices.

junction. The e–h pairs can be easily separated at the LDD region owing to the strong depletion electric field.(33) Interestingly, β_{HI} < 1.0 for the NH SOI device at locations of −0.1–−0.3 μm, which was different from other research results.(33–37) This means that there is an extra conductive channel through which carriers flow out of the body region, escaping from flowing into the drain region. This can be explained as follows. The tunneling current source p–n junction is speculated to play a key role in reducing the parasitic β_{HI} for the NH counterpart. Figure 11 shows the further simulated silicon electrical potential of the NH SOI device with and without the recombination model. Once the ion penetrated the Si film, the Si film potential dropped from 0.45 to 0.32 V at 1 ns. In this case, the source p–n junction was still under forward bias. In the long term, the final Si potential was 0.29 V after 10 ns, which was near 0.32 V at 1.0 ns. The lack of a recombination model causes a long life τ. On the other hand, the Si film potential can be sharply reduced from 0.41 to 0.18 V with the incorporation of the recombination model. Aside from the SRH recombination mechanisms, the quantum tunneling mechanism also helps to reduce the number of e–h pairs generated by incident ions and strong field ionization. In conclusion, the NH SOI device has an excellent capacity to suppress the Si film potential instability without the need to modify the device layout.

5. Conclusions

For PD SOI MOSFETs, there is a neutron irradiation technique that increases radiation hardness and suppresses floating body effects. The hardened SOI devices are named NH devices. The NH SOI device exhibited an excellent kink effect suppression capability. However, it also suffered from a significant increase in breakdown voltage and leakage current owing to the excessive drain tunneling current. Importantly, the NH SOI devices have excellent TID and SEE hardness. The channel coupling effect after radiation in PD devices was well suppressed in the NH SOI devices because of the decreased depletion width. The weakened front–back interconnections also controlled well the abnormal steep *SS* characteristics. A very low bipolar gain (even lower than 1.0) at the source junction can be realized for drain sides. A low bipolar gain suggests that SEE can be considerably suppressed in the new structure. Therefore, one can

expect that the new structure would provide excellent experimental results aside from the aforementioned simulations, including TID and SEE. Overall, a solution for hardening PD SOI devices to make them suitable for harsh-environment applications has been demonstrated in this work.

Acknowledgments

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