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Electrostatic Discharge Power Supply Clamp Circuit with a Modified-Resistor/Capacitor Network

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The resistor/capacitor (RC)-triggered power supply clamp circuit has been widely utilized to protect CMOS integrated circuits (ICs) from damage caused by electrostatic discharge (ESD). In this work, an ESD power supply clamp circuit with a modified-RC network in a 0.18-μm CMOS process is proposed. The layout area of the novel RC network is ultrasmall compared with that of the traditional RC network in a clamp circuit. The proposed clamp circuit can keep the clamp device "on" during the ESD event, whereas it allows a turn-off mechanism with a recovery time of 70 μs under a system-level test. The clamp circuit can effectively avoid false triggering events, such as a 1.8 V/10 ns power-up event. With its high performance and low area cost, this clamp circuit can be used in the sensor IC of industry.

1. Introduction

Sensors based on CMOS technology are developing rapidly. With the scaling down of the feature size of CMOS technology, the thin gate oxide and shallow junction depth provide reliability for integrated circuit (IC) design. Electrostatic discharge (ESD) is one of the most urgent reliability issues.[1–3] Therefore, ESD has been considered as one of the most significant issues affecting the reliability of CMOS ICs. Nowadays, as part of the whole chip ESD protection, the power supply clamp circuit is indispensable to prevent damage in the internal circuit of ICs.[4,5] The main discharge device in the ESD protection circuit can be rapidly turned on to discharge the ESD charges under ESD stress.

The clamp circuit based on a MOSFET with a triggering circuit has been extensively investigated.[6–14] Its main advantages include no extra process steps, small layout area, and easy simulation by computer tools. As shown in Fig. 1, the overall structure of a classic clamp circuit consists of three parts: the clamp device, the delay element, and the detect element. The clamp device is a very large MOSFET. The detect element is usually a resistor/capacitor (RC) network; it is used to detect the ESD event and send a signal to the back-end circuit. Many types of delay element have been proposed to provide a sufficient delay time for the clamp device. However, reports of an improved RC network are few. In this paper, we present a modified-RC network to

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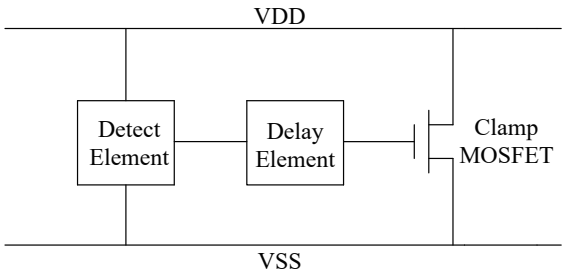

Fig. 1. Overall structure of classic clamp circuit.

reduce the large layout area consumption of the traditional RC network, and by optimizing the delay element, the clamp circuit obtains high performance.

2. Operation of Transient ESD Clamp Circuits

The classic RC-triggered clamp circuit is shown in Fig. 2. The RC network is the detect element. The rise time of an ESD event ranges from 100 ps to 60 ns, whereas that of a normal power-up event is in the order of milliseconds.[11] Therefore, in the classic clamp circuit, the RC time constant is usually set to 1 ms to distinguish the ESD event from the normal power-up event.

However, for some special applications, the fast rise time is usually shorter than a millisecond or even approaches hundreds of nanoseconds, such as "hot plug" operations or switching networks controlling the sleep power mode in low-power high-performance microprocessors.[11] Thus, the clamp circuit might be triggered under normal operating conditions, which is regarded as false triggering.

In Fig. 2, the "CLK" signal is the detect result. Since the RC network also accomplishes the delay function and the RC time constant is large enough, the "CLK" remains "1" for a long time. Thus, the clamp MOSFET can be turned on for a long time to discharge ESD energy. The two inverters are used to recover voltage. It is evident that this circuit requires a very large layout area to place the resistor and capacitor. Furthermore, the large RC constant is detrimental to the immunity to false triggering. The RC network with a large RC constant can detect a broad range of fast power-up events, so some false triggering pulses are regarded as ESD events. Then, the clamp MOSFET is turned on and the IC leaks energy.

3. Design of ESD Clamp Circuit with a Modified-RC Network

3.1 Detect element

Since the resistivity of a MOSFET-based resistor is much higher than that of a poly-Si resistor, the MOSFET is used as the resistor of the RC network in many works. In the traditional MOSFET-based RC network, a gate-grounded PMOSFET is usually used as the resistor as

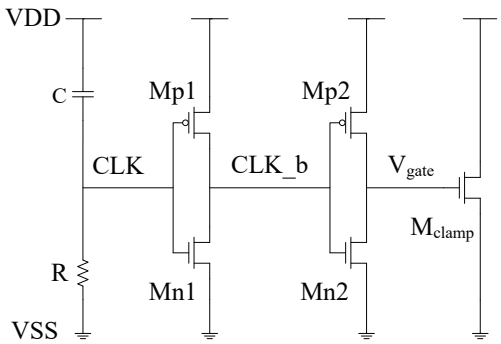

Fig. 2. Schematic of classic clamp circuit.

shown in Fig. 3(a). In such an RC network, the area of the PMOSFET is acceptable, whereas the capacitor still occupies a large area.

To further reduce the area consumption, we increase the equivalent resistance of the PMOSFET by reducing its gate-to-source voltage ($|V_{gs}|$). A modified-RC network is presented as shown in Fig. 3(b). Mp1, Mp2, and Mn1 form a biased circuit, and the RC network consists of Mp3 and C1. The biased circuit provides the signal "Bias1" for the gate of Mp3. Here, Mp1 and Mp2 are both diode-connected. Mn1 is always turned off, so there is an extremely small leakage current flowing through these three series transistors. As a result, Mp1 and Mp2 operate in the subthreshold region, so the $|V_{gs}|$ of Mp3 can be calculated as

$$\left|V_{gs}\right|_{Mp3} = VDD - Bias1 = \left|V_{gs}\right|_{Mp1} + \left|V_{gs}\right|_{Mp2} = 2\left|V_{gs}\right|_{Sub\text{-}threshold}. \quad (1)$$

Since $|V_{gs}|_{Mp1}$ and $|V_{gs}|_{Mp2}$ are both $|V_{gs}|_{Sub\text{-}threshold}$, $|V_{gs}|_{Mp3}$ is small. On the other hand, the $|V_{gs}|$ of the gate-grounded PMOSFET in the traditional MOSFET-based RC network is equal to VDD, so the equivalent resistance of the PMOSFET in the proposed RC network becomes high. Hence, the area of the capacitor in the novel proposed RC network will be sharply reduced.

It is not necessary to further reduce $|V_{gs}|_{Mp3}$. The large RC time constant is not always good, and "Bias1" should be adjusted properly. In the above design, the size of the capacitor is 2×1.5 μm^2 and the *W*/*L* ratio of Mp3 is 0.3 μm/1 μm. This means that the area of the modified-RC network is small. If $|V_{gs}|_{Mp3}$ is further reduced to a smaller value, the equivalent resistance of the RC network becomes very large and false triggering risk increases.

Note that the proposed circuit includes the transistors operating in the subthreshold region (Mp3) to implement high impedance or reduce power consumption. Such a method has been used in advanced low-power circuit design.[15,16]

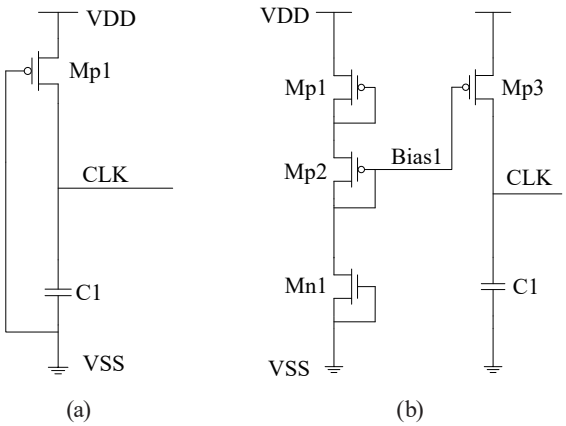

Fig. 3. Schematics of (a) traditional MOSFET-based and proposed modified-RC networks.

3.2 Delay element

The traditional RC network occupies a large layout area and makes the clamp circuits more sensitive to false triggering as mentioned in Sect. 2. The feedback technique was widely used to implement the delay element to solve this problem.[5–10] For the false triggering concern, these circuits can be turned off by different leakage currents of the transistors. The delay element based on flip-flop has a similar principle to those using the feedback technique.[11] Dual-time constant clamp circuits were also proposed to enhance the immunity to false triggering events.[12–14] The shorter and longer time constants were used to detect the ESD events and keep the clamp circuits at the ON-state, respectively.

In this study, the delay function of the proposed clamp circuit is similar to those of the circuits using the feedback technique. However, the turn-off mechanism is different. It adopts a biased pull-up MOSFET to quickly stop the "on" state of Mclamp caused by very fast power-up events. The whole schematic of the proposed clamp circuit is illustrated in Fig. 4. In this circuit, Mn3 and Mp5 consist of another bias circuit, which generates a relatively high voltage signal "Bias2". Since Mn3 is always turned off and Mp5 is diode-connected, "Bias2" is set to approximately 120 mV lower than VDD when VDD is stabilized, and Mp6 works in the subthreshold region.

3.3 Operation principle of proposed circuit

When the ESD event occurs, the RC network is triggered, and "CLK" remains at 0 at first. Mn2 is a long-length transistor, so "CLK_b" will be pulled up to a relatively high voltage by Mp4. Mn4 is fully turned on and has a stronger pulling ability than the Mp6 operating in the subthreshold region, so "Inv_in" is 0, "Vgate" is 1, and Mclamp is turned on.

Under normal operating conditions, the RC network does not respond, "CLK" is tied to VDD, "CLK_b" is pulled down to 0 by Mn2, and Mn4 is turned off. Although Mp6 operates in the sub-threshold region, "Inv_in" is pulled up to 1. Thus, "Vgate" remains at 0 and Mclamp remains at the "off" state.

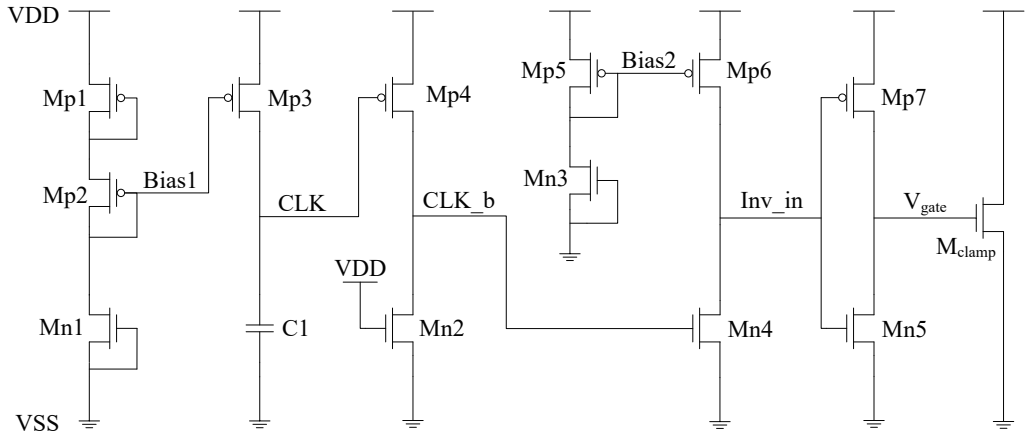

Fig. 4. Whole schematic of proposed clamp circuit.

If the clamp circuit is falsely triggered by any reason, "CLK_b" is pulled up initially, "Inv_in" is pulled down to 0, and Mclamp is turned on. Then, "CLK" gradually rises to 1 and "CLK_b" gradually goes back to 0. The equivalent resistance of Mn4 becomes larger than that of Mp6 operating in the subthreshold region and "Inv_in" is gradually pulled down by the subthreshold leakage current of Mp6; finally, "Inv_in" becomes 1 and "Vgate" is pulled down to 0.

4. Characteristic Simulation

The novel clamp circuit is designed and simulated in a 1.8 V 0.18-μm CMOS process. The width of Mclamp is set to 400 μm to meet the requirement of the 2 kV human body model (HBM). All the device sizes are listed in Table 1.

4.1 ESD voltage characteristic

A ramp from 0 to 5 V with the rise time of 10 ns is applied to VDD to simulate the ESD event. The waveform of "Vgate" is shown in Fig. 5. Mclamp remains "on" for over 10 μs under the 10 ns/5 V event, which is long enough to discharge the ESD energy. Under the low-level ESD event (50 ns/4 V), the clamp circuit is also triggered and the delay time is approximately 10 μs. Hence, the delay time is sufficient to discharge ESD energy.

4.2 Normal operating condition

Figure 6 shows the simulated result under a normal operating event. VDD rises from 0 to 1.8 V in 1 ms and "Vgate" rises to 31 mV and soon goes back to 0. The leakage current eventually remains at 8.4 nA. Hence, the clamp circuit does not turn on under normal operation.

Table 1
Device sizes of proposed circuit.

Device	Size (μm / μm)	Device	Size (μm / μm)
Mp1	0.3 / 1	Mn1	4 / 0.18
Mp2	0.3 / 1	Mn2	1 / 1
Mp3	0.3 / 1	Mn3	4 / 0.18
Mp4	4 / 0.18	Mn4	2 / 0.18
Mp5	0.3 / 0.3	Mn5	4 / 0.18
Mp6	10 / 0.18	C1(NMOS)	1.5 / 1
Mp7	20 / 0.18	Mclamp	400 / 0.18

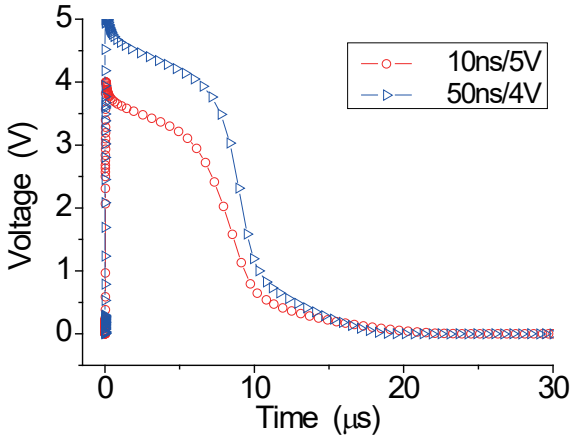

Fig. 5. (Color online) Waveform of "Vgate" under different levels of ESD event.

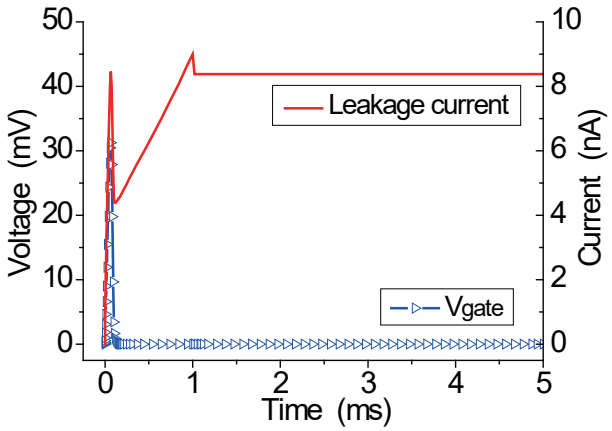

Fig. 6. (Color online) Waveform of "Vgate" and leakage current under a normal operating event.

4.3 Immunity to false triggering

To explain the excellent immunity to false triggering in some special applications, the simulation conditions are set to 10 ns/1.8 V and 10 ns/2.1 V. Figure 7 shows the waveform of "Vgate" under these conditions. Considering the power supply variation, VDD reaches 2.1 V in the simulation. Under the 10 ns/2.1 V power-up event, the clamp MOSFET is triggered for about

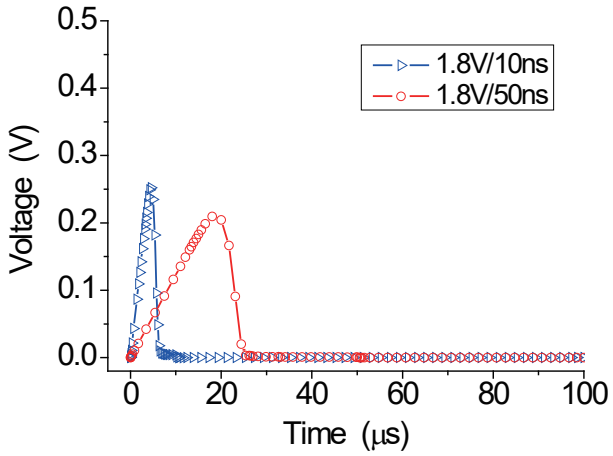

Fig. 7. (Color online) Waveform of "Vgate" under different conditions (1.8 V/10 ns and 1.8 V/50 ns).

7 μs. Compared with the circuit in Ref. 11 (~200 μs), the turn-off time is very short. Owing to the excellent immunity to false triggering, the proposed clamp circuit can avoid most false triggering events. We can see that the 10 ns/1.8 V and 50 ns/2.1 V power-up events are avoided.

4.4 Noise characteristic

The high switching rates usually cause the power supply noise, which can cause energy consumption and even trigger the clamp circuit. It is necessary to simulate the clamp circuit by adding a pseudorandom pulse. The added noise has a rate of 500 Mb/s and an amplitude of 0.6 V.[11] The noise characteristic of "Vgate" is shown in Fig. 8. It can be seen that the maximum voltage of "Vgate" is only about 60 mV and the peak width is very small. Therefore, M0 cannot be turned on and the novel clamp circuit can reject the power supply noise significantly.

4.5 Circuit-level ESD test

The circuit-level ESD test is performed to verify the effectiveness of the clamp circuit under the ESD conditions. According to the US MIL-STD-883 (method 3015.7), the HBM waveform has a rise time of 2–10 ns and a delay time of 120–180 ns. For a 2 kV ESD test, the peak current is 1.33A ± 10%. The transient current waveform used in the simulation is shown in Fig. 9.

Figure 10 shows the ESD response of VDD in the circuit-level ESD test. VDD first rises to nearly 6 V and gradually falls. Since the gate-oxide breakdown voltage of transistors in 0.18-μm CMOS technology under a 100 ns voltage pulse is around 8 V,[11] the clamp circuit passes the 2 kV HBM circuit-level test.

4.6 System-level ESD test

In recent years, the system-level ESD test has become more significant. It has been reported that some transient ESD clamp circuits have passed the circuit-level ESD specifications, but failed under the system-level test.[17–20] The failure occurs when the clamp circuit is not turned

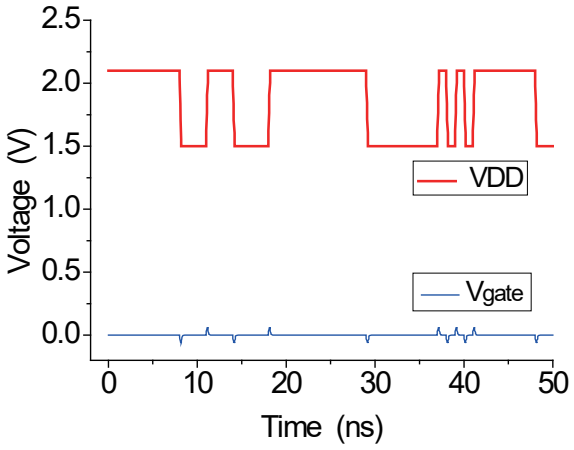

Fig. 8. (Color online) Waveform of VDD and "Vgate" under noise characteristic.

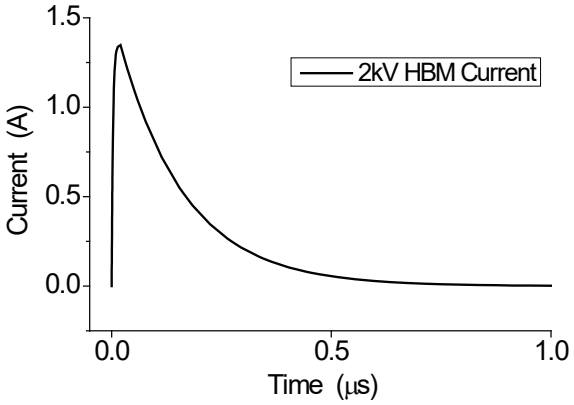

Fig. 9. Waveform of current used to simulate 2 kV HBM circuit-level test.

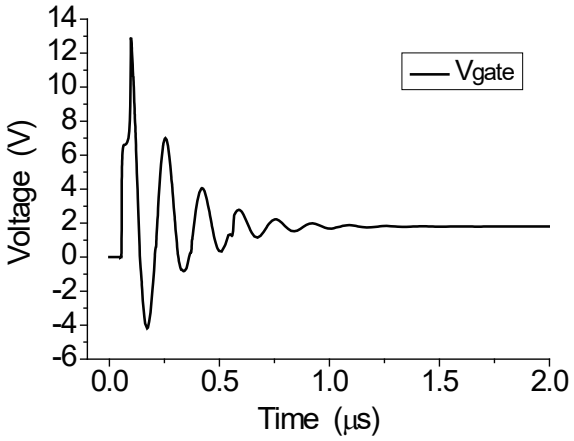

Fig. 10. Waveform of "Vgate" under system-level test in the first 2 μs.

off in time and the leakage current increases after the system-level test. Thus, the system-level ESD test is indispensable. In this test, a damped sinusoidal voltage is applied to VDD. The expression of the voltage source is shown as[11]

$$V(t) = V_0 + V_a \cdot \exp[(t_d - t)D_a] \cdot \sin[2\pi f(t - t_d)]. \quad (2)$$

In Eq. (2), $V_0 = VDD = 1.8$ V, $V_a = 14.6$ V, $t_d = 50$ ns, $D_a = 2 \times 10^7$ s^{-1}, and $f = 20$ MHz. Figure 10 shows the waveform of "Vgate" under the system-level test in the first 2 μs. It can be seen that "Vgate" initially oscillates with VDD and gradually tends to exhibit VDD in about 1 μs. Mclamp is fully turned off in 70 μs as illustrated in Fig. 11. Thus, we can conclude that the proposed clamp circuit can successfully pass the system-level test.

4.7 Temperature variation

It is necessary to consider the impact of temperature variation on the operation of the proposed power clamp. The delay time of the clamp circuit using the feedback network and similar ones vary with the temperature.[5] In this paper, 5 V/10 ns and 1.8 V/ 10 ns power-up events are applied at 125 ℃. Figure 12 shows the waveform of "Vgate" under these conditions. We can see that under the 5 V/10 ns event, "Vgate" rises to 5 V and lasts for approximately 1 μs. Under the 1.8 V/10 ns event, Mclamp is turned on for about 50 ns and soon turned off. Therefore, the clamp circuit can respond to the ESD event and avoid false triggering at high temperatures.

5. Discussion

We compared the proposed circuit with previous works. All these circuits can respond to the ESD stress and discharge ESD energy, but it is still necessary to discuss other performance characteristics.

1) Layout area. As for the RC-triggered power clamp circuits, the width of the clamp MOSFET is directly proportional to the ESD protection level. The layout area of the clamp MOSFET is determined by the design requirement. Therefore, we only compare the layout areas of control parts (detection and delay parts) of the clamp circuits. The circuit in Ref. 11 adopts a traditional RC network with a time constant of 40 ns as the detection circuit, and in turn, the control part area is mainly occupied by the resistor and capacitor. The circuit in Ref. 13 even uses a total resistance of 150 kΩ. In the proposed circuit, only a 3 μm^2 capacitor is used, whereas the capacitor area reaches around 400 μm^2 in Ref. 11. The size of the control part is only 12 × 25 μm^2 as shown in Fig. 13. Hence, the proposed circuit clearly minimizes the layout area.
2) Immunity to false triggering. The proposed circuit has good false triggering immunity. The circuits in Refs. 11 and 13 can avoid a 1.8 V/200 ns false triggering event. In comparison, the proposed circuit in this paper can avoid a 1.8 V/10 ns false triggering event; the peak value of "Vgate" is only 0.25 V, which is rapidly pulled down to 0 in around 6 ns.

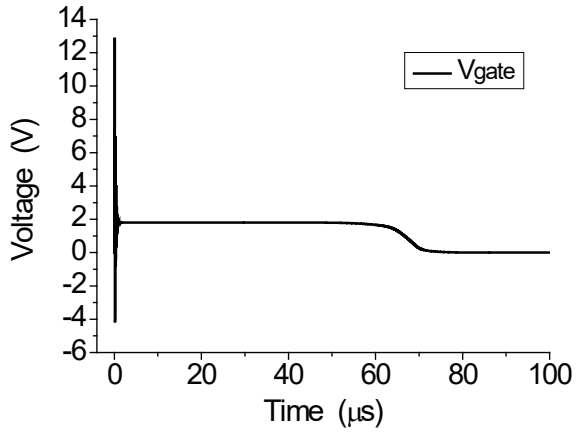

Fig. 11. Waveform of "Vgate" under system-level test in complete procedure.

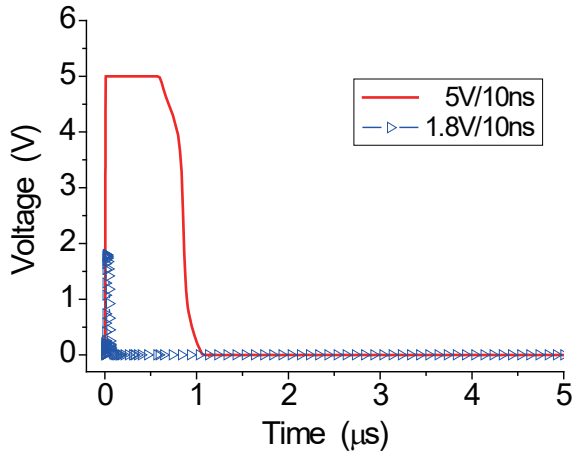

Fig. 12. (Color online) Waveform of "Vgate" under different power-up events at 125 °C.

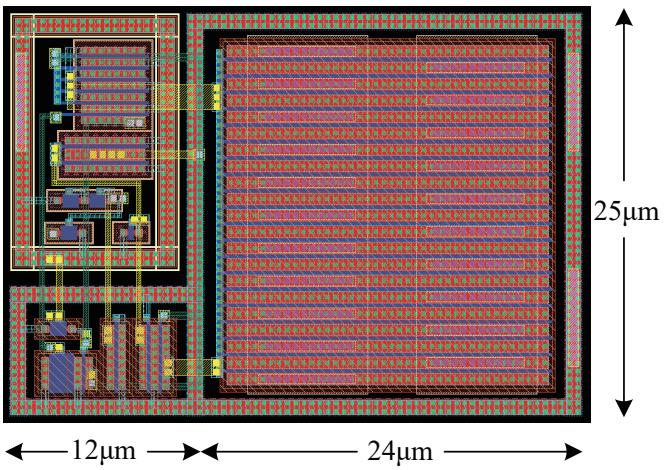

Fig. 13. (Color online) Layout of proposed circuit.

3) Recovery time. In the previous designs, when the clamp circuit is falsely triggered by any reason, the clamp device is finally turned off by the OFF-state leakage current of the MOSFET. Since the leakage current is very small, these clamp circuits need a long time to recover. As for the circuit in Ref. 11, the recovery time is around 200 μs. However, since the relatively large subthreshold leakage current is utilized, the recovery time of the proposed circuit is reduced to around 70 μs.

6. Conclusions

In this paper, a novel ESD power clamp circuit with a modified-RC network in a 0.18-μm CMOS process is proposed. The greatest advantage of this clamp circuit is the ultrasmall layout area due to the proposed modified-RC network. At the same time, it works well under both ESD event and normal operating conditions. The delay time under the ESD event is beyond 10 μs and the circuit is also immune to the fast power-up event, such as 1.8 V/10 ns. The recovery time under the system-level test is 70 μs. It is considered that the proposed clamp circuit can be widely used in the sensor IC of industry.

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