Sensors and Materials, Vol. 36, No. 5 (2024) 1797–1803
MYU Tokyo

S & M 3634

Comparative Analysis of Defect Characteristics in Silicon Carbide Wafers of Different Grades

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(Received October 27, 2023; accepted April 2, 2024)

Keywords: silicon carbide wafers, grades, defect analysis, production grade, dummy grade

In this study, two different grades of wafers, production grade and dummy grade, were employed for defect comparison. Wet etching with KOH was utilized to reveal defects on the surface of silicon carbide wafers. Optical microscopy and laser scanning confocal microscopy were employed for analysis, enabling an exploration of the performance differences between wafers of the two grades. The surface topography and etch pit profile depth were analyzed and discussed to evaluate the quality of wafers of each grade. The surface topography analysis reveals that production-grade wafers exhibit significantly fewer defects, and the types of defect differ between the two grades. Dummy-grade wafers display four defect types, micropipe (MP), threading screw dislocation (TSD), threading edge dislocation, and basal plane dislocation, whereas production-grade wafers have only two defect types, TSD and MP. Additionally, the etch pit depth serves as a criterion for classifying the four defect types. When the dimensions of surface shape and profile depth are similar, the location of the pit bottom within the profile can also be used as a judgment criterion.

1. Introduction

In recent years, the development of electric vehicle technology and the proliferation of 5G chips have led to a significant increase in the demand for semiconductor chips from major communication, electric vehicle, and aerospace companies. However, as silicon wafers are gradually encountering limitations under Moore's Law, research into new materials has been initiated worldwide, with Type III semiconductor materials emerging as a key research focus. Type III semiconductor materials encompass wide-bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN), which are characterized by their high-temperature, high-pressure, high-frequency, high-efficiency, and small size properties.[1–3] These materials are expected to become essential for manufacturing critical components in future industries.[4]

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https://doi.org/10.18494/SAM4795

ISSN 0914-4935
https://myukk.org/

Semiconductor SiC components are primarily employed in the high-power, high-frequency electronics market, including applications in electric vehicles, 5G communications, satellite communications, and solar power equipment. These components exhibit excellent material properties, such as low power consumption, high-temperature resistance, and speed, resulting in more energy-efficient chip operation. Although SiC offers numerous advantages, there are still several technical challenges in wafer production that must be addressed. SiC has over 200 crystal structure types, with the hexagonal 4H-type structure (4H-SiC) and a few other crystal structures being essential for semiconductor materials. Therefore, precise control of the silicon-to-carbon ratio, growth temperature, growth rate, gas flow, and pressure, among other parameters, is necessary; otherwise, the production of polycrystalline inclusions may lead to defective final products.[5,6]

The occurrence of common defects in SiC, such as threading screw dislocation (TSD), which can deteriorate the characteristics of wafer devices, and threading edge dislocation (TED), which has no impact on wafer devices,[7–9] emphasizes the importance of developing a classification method capable of detecting and distinguishing these dislocations from other types of defect. Sakwe *et al.* and Katsuno *et al.* employed a KOH wet etching method to expose defects on the surface of SiC wafers.[10,11] These defects were observed by optical microscopy (OM).[12] Experimental results revealed that the etch pits could be categorized into approximately four common defect types. In separate studies, Cui *et al.* and Yang *et al.* utilized laser scanning confocal microscopy (LSCM) to observe the etch pit profiles and the evolution of penetration aberrations over time for the identification of TSD and TED defects.[13,14]

In this study, two different grades of wafers, production grade and dummy grade, were utilized to compare the defects. The defects on the surface of the SiC wafers were revealed through wet etching with KOH, followed by the analysis and discussion of surface morphology and etch pit profile depth using the results of OM and LSCM. This approach was employed to investigate and assess the quality performance of wafers of different grades.

2. Experimental Procedure

Figure 1 shows the experimental setup for the molten KOH etching of SiC wafers. The physical vapor transfer (PVT) method was employed to grow 4H-SiC wafers for experimental testing. SiC wafers were cut and secured in place using a low-adhesive film, resulting in postcutting wafer sizes of approximately 5×5 mm^2. These wafers were then placed in a nickel crucible, which is inert to molten KOH. Nickel crucibles typically possess corrosion resistance, high-temperature endurance, and conductivity, making them a commonly used material in the process of chemical etching. Subsequently, 85% KOH was added, and the mixture was heated to a high temperature to liquefy the KOH. After the etching process was completed, the wafers were removed from the nickel crucible. After etching, the wafers were allowed to naturally cool to room temperature, washed with deionized water and anhydrous ethanol, and finally dried using nitrogen.

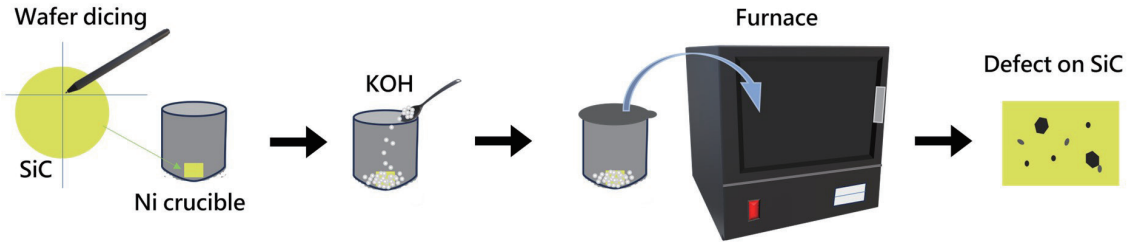


Fig. 1. (Color online) Experimental setup for molten KOH etching of SiC wafer.

The chemical mechanism of SiC etching with KOH is elaborated below.[8,15]

$$SiC + 2KOH + 2O_2 \rightarrow K_2CO_3 + SiO_2 + H_2O \quad (1)$$

2.1 Dummy-grade SiC wafer

In this study, the PVT method was employed to grow dummy-grade wafers with the following specifications: crystal orientation <100>, 4H polytype with a purity of at least 99%, a size of 6 inches, type N doping, and a thickness ranging from 325 to 375 μm.

Control of the KOH etching temperature and duration allows us to reveal subsurface defects in the wafer. The temperature was varied from 400 to 550 °C, and the initial tests involved duration control from 10 to 60 min. Ultimately, the conditions of 450 °C for 20 to 40 min were chosen to achieve the optimal defect visibility on the surface, with etching depth controlled within 10 μm.

2.2 Production-grade SiC wafer

The production-grade wafers grown by the PVT method in this study are 4-inch semi-insulating 4H-SiC substrates with a <100> crystal orientation, a polytype of 4H, and a thickness of 506 μm.

For these production-grade wafers, the initial etching temperature selected on the basis of experience was 450 °C. Subsequent process tests were conducted to analyze the etching time. It was confirmed through experiments that defects were not significantly noticeable at 10 min of etching. However, as the etching time increased, the depth of defects became more pronounced. It was determined that the conditions of 400 °C for 40 min resulted in overly dense etching and could not be used for defect determination. Therefore, the basis for defect judgment was shifted to surface morphology observation. The conditions of 450 °C for 20 min were chosen for etching because they allowed complete observation of defect morphology without causing excessive etching. The results of surface morphology observation served as the primary criterion for defect assessment.

3. Results and Discussion

The aim of the present study is to optimize KOH etching for 4H-n-SiC in order to investigate defects using a laboratory muffle furnace. The etched surface was subsequently observed by OM. Additionally, the morphology of the etched surface was examined by OM, and the cross-sectional depth of the etch pits was observed by LSCM to identify the types of defect.

3.1 Surface morphology analysis

Figure 2 displays the surface morphology of dummy-grade SiC after KOH etching, as observed by OM. The surface reveals four distinct types of defect: micropipe (MP), TSD, TED, and basal plane dislocation (BPD). Among these, MP is considered a critical defect in circuit components. It is a crystal defect within the substrate, characterized by a size of approximately 44 ± 5 μm (measured diagonally) and a hexagonal shape. Both TED and BPD are similar in size, with TED measuring 9 ± 5 μm and BPD measuring 10 ± 5 μm, but they exhibit distinct surface patterns primarily owing to differences in their Burgers vectors. In terms of morphology, TED appears nearly circular, while BPD exhibits a comet-like shape.

Figure 3 illustrates the surface morphology of production-grade SiC wafers after KOH etching, as observed by OM. Upon examining the surface morphology, it is evident that the defect density has significantly decreased, leaving only two types of defect, MP and TSD. The morphologies of these defects are more distinctly visible, with MP exhibiting a hexagonal shape and measuring approximately 55 ± 5 μm (diagonally), while TSD appears nearly circular with a size of 36 ± 5 μm.

3.2 Profile analysis

The utilization of LSCM allows us to differentiate not only the surface morphology but also the depth of the etched pits, enabling the observation of individual defects. To facilitate a

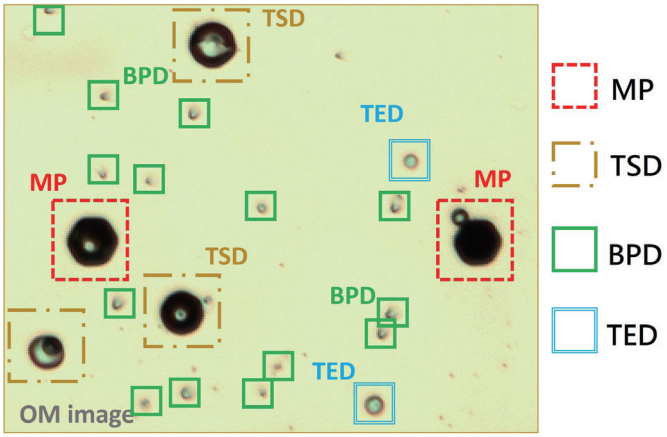


Fig. 2. (Color online) OM images of dummy-grade SiC wafers.

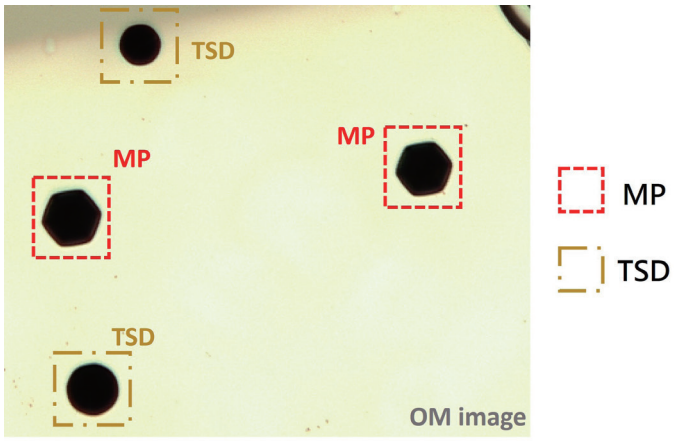


Fig. 3. (Color online) OM images of production-grade SiC wafers.

Table 1
(Color online) Different grades of SiC defect morphology and sectional views.

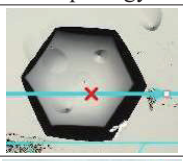
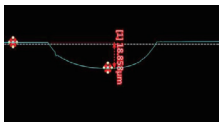
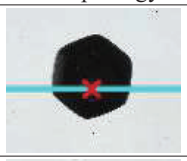
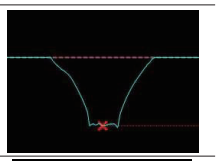
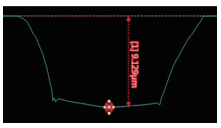
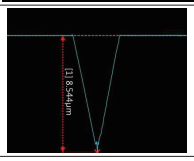
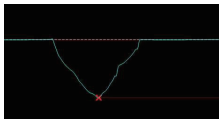
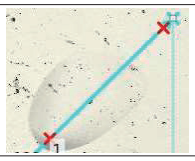
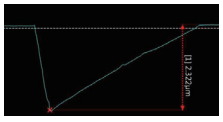
Defect type	n-type (dummy grade)		Semi-insulating (production grade)	
	Morphology	Sectional view	Morphology	Sectional view
MP				
TSD				
TED			N/A	N/A
BPD			N/A	N/A

Table 2
Defect etch pit sizes on SiC wafers of different grades.

Defect type	n-type (dummy grade)	Semi-insulating (production grade)
	Etch pits (μm)	Etch pits (μm)
MP	18.8 ± 3	30.4 ± 10
TSD	9.1 ± 3	8.5 ± 5
TED	2.7 ± 1	N/A
BPD	1.2 ± 1	N/A

Table 3
Surface morphology dimensions of defects on SiC wafers of different grades.

Defect type	n-type (dummy grade)	Semi-insulating (production grade)
	Surface morphology dimensions (μm)	Surface morphology dimensions (μm)
MP	44 ± 5	55 ± 5
TSD	35 ± 5	36 ± 5
TED	9 ± 5	N/A
BPD	10 ± 5	N/A

comparison between the two grades of wafers, the results have been compiled in Table 1. An analysis of the pit profiles provides valuable insights. Most of the pits exhibit a centrally located base, resulting in a more symmetrical surface morphology. However, BPD exhibits distinct behavior, where the pit bottom is inclined to one side, giving rise to a comet-like surface morphology. This morphology is also attributed to the formation of BPD defects in the crystal lattice.

To facilitate a more straightforward comparison of various defect types, they have been analyzed in relation to each other, as summarized in Tables 2 and 3. Table 2 clearly shows that each type of defect results in a different depth of etch pits, providing valuable insights for accurate defect identification. For instance, the etch pit depth of MP is significantly larger than those of other defect types. In Table 3, surface morphology dimensions of defects on SiC wafers of different grades are summarized.

4. Conclusions

We utilized wafers of two different grades for etching verification. From the analysis of surface morphology, it was evident that the wafers of higher grade exhibited fewer defects, and the types of defect also varied. In the dummy-grade wafers, there were four types of defect, TSD, MP, TED, and BPD, whereas the production-grade wafers showed only two types of defect, TSD and MP.

Furthermore, by examining the depth of etch pits, we established criteria for classifying the four types of defect. TSD and MP shared a common hexagonal surface morphology with sizes ranging from 30 to 50 μm. The position of the bottom of the pit is used as the criterion for determining the pit depth. When the pit depth exceeds 15.8 μm, it is determined to be MP. BPD is identified by the eccentric features at the bottom of its pits.

Acknowledgments

We wish to acknowledge the financial support of the work reported in this paper by the National Science and Technology Council (NSTC) of Taiwan under Contract Number NSTC 111-2222-E-218-004- and the Taiwan Semiconductor Research Institute (TSRI) of Taiwan under Contract Number JDP112-Y1-042. We greatly appreciate the financial assistance provided. We also extend our sincere appreciation to KEYENCE TAIWAN Co., Ltd. for generously lending us their confocal laser scanning microscope.

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