

Prediction of Electrical Characteristics of Fin Field-effect Transistor Devices Based on Simulation Using Deep Learning Method

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Nowadays, silicon-based fin field-effect transistor (FinFET) devices have become the top choice for integrated circuit designers because they can handle the majority of application scenarios. In this article, the authors propose applying deep learning models to predict the electrical characteristics of devices using their structural parameters, aiming to solve the problems of complexity, time consumption, and convergence difficulty in traditional simulations. The authors first determine the electrical characteristics of simulations on FinFET devices using technology computer-aided design (TCAD). Different deep learning models were constructed in this study to predict various electrical parameters and characteristics of integrated circuit devices based on different datasets and prediction tasks, and high levels of accuracy were achieved. For instance, the average normalized mean square error of the predicted electrical parameters of FinFET devices based on TCAD simulation was less than 1.4×10^{-5} , while the average relative errors of the predicted DC and AC characteristics of FinFET devices based on Berkeley short-channel insulated gate FET model (BSIM) simulation were 7.12×10^{-3} and 4.8×10^{-3} , respectively. These results demonstrate that the proposed deep learning models can effectively predict the electrical parameters and characteristics of integrated circuit devices, providing strong support for device design and optimization.

1. Introduction

Over the past decade, a fin field-effect transistor (FinFET) has gained more attention than a planar metal-oxide-semiconductor field-effect transistor (MOSFET) owing to its smaller short-

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channel effects.^(1,2) As the device size goes from the micron level to the nanometer level and even approaches the atomic scale, with structures reaching critical dimensions and even coherence lengths close to those of electrons, the analysis of physical properties enters the realm of quantum mechanical effects. The 3–14 nm node devices have completely different device structures and physical effects^(3,4) from traditional transistors. On one hand, traditional simulation models have biases in coefficient calibration, making it imperative to calibrate new models to achieve better simulation results. On the other hand, the physical and chemical phenomena of materials have become more complex in new processes, making accurate description and simulation difficult. In technology computer-aided design (TCAD) simulations, mesh settings are required to determine simulation accuracy. For increasingly complex device structures and smaller device sizes, sufficient mesh nodes are needed for numerical solutions, which will bring about huge computational and time costs.^(5–8)

Deep neural networks are a versatile machine learning algorithm that utilizes the sequential stacking of nonlinear processing layers to capture and model highly nonlinear data relationships. Given the remarkable success of deep learning in computer science and engineering-related fields, including computer vision, natural language processing, speech recognition, knowledge graph, and decision-making, it has also captured the attention of researchers in disciplines such as optical design, materials science, biomedical, and quantum mechanics.^(9–13) Deep learning circumvents the drawbacks of traditional iterative simulation methods and creates unprecedented opportunities in these fields. Deep neural networks avoid the interference of human factors and find the nonlinear relationship between input and output on the basis of existing data, providing an effective method for the design of device structures and complementing traditional methods based on physical calculations. Currently, deep learning has achieved certain success in fields such as predicting fully depleted silicon-on-insulator (FDSOI) devices,^(14,15) nanowire devices,⁽¹⁶⁾ and irradiation.⁽¹⁷⁾

In this paper, deep learning network structures are proposed to predict the transfer characteristic ($I_{DS}-V_{GS}$) curve and electrical parameters of FinFET devices. We first simulated the electrical characteristics of FinFET devices using TCAD and advanced design system (ADS) software, and selected different device structure parameters and electrical characteristics as input and output for the prediction model in accordance with the corresponding device's working mechanism and the selected simulation scenarios. Referring to the different simulation results, we constructed the required datasets for each prediction model and ultimately obtained a FinFET device dataset based on TCAD simulations. Using different datasets constructed for different prediction tasks and data structures, we built various deep learning models for prediction, achieving high accuracy in all cases. The research method for predicting the electrical characteristics of FinFET devices proposed in this paper does not need the professional knowledge of microelectronics and only requires the modification of the device structure to predict the corresponding electrical characteristics. This method provides a new direction for device research.

2. Experimental Methods

2.1 Device structure

In this study, we mainly use Sentaurus TCAD to establish a FinFET model to investigate the impact of different device structural parameters on the electrical characteristics of FinFET devices. The impact of process parameter fluctuations on the device's electrical performance is not within the scope of this study. Therefore, in this study, we directly construct the three-dimensional structure of the device by entering coordinate codes in the Sdevice module. Table 1 shows the modeling dimensions of the silicon-on-insulator FinFET (SOI-FinFET).

The specific doping methods and doping concentrations of each region of the FinFET are shown in Fig. 1. The silicon substrate, fish fin area, source region, and drain region are first

Table 1
Modeling dimensions of the SOI-FinFET.

Area name	X-axis coordinates	Y-axis coordinates	Z-axis coordinates
Silicon substrate (Sub)	(-0.3, 0.3)	(-0.35, 0.35)	(0.14, 0.37)
Buried oxygen layer (Box)	(-0.3, 0.3)	(-0.35, 0.35)	(0.04, 0.14)
Polysilicon gate (Poly)	(-0.3, 0.3)	(-0.5, 0.5)	(-0.1, 0.04)
Gate oxide layer (Gox)	(-0.033, 0.033)	(-0.5, 0.5)	(-0.002, 0.04)
Fish fin area (Fin)	(-0.015, 0.015)	(-0.15, 0.15)	(0, 0.04)
Source region (S)	(-0.3, 0.3)	(-0.3, -0.15)	(0, 0.04)
Drain region (D)	(-0.3, 0.3)	(0.15, 0.3)	(0, 0.04)

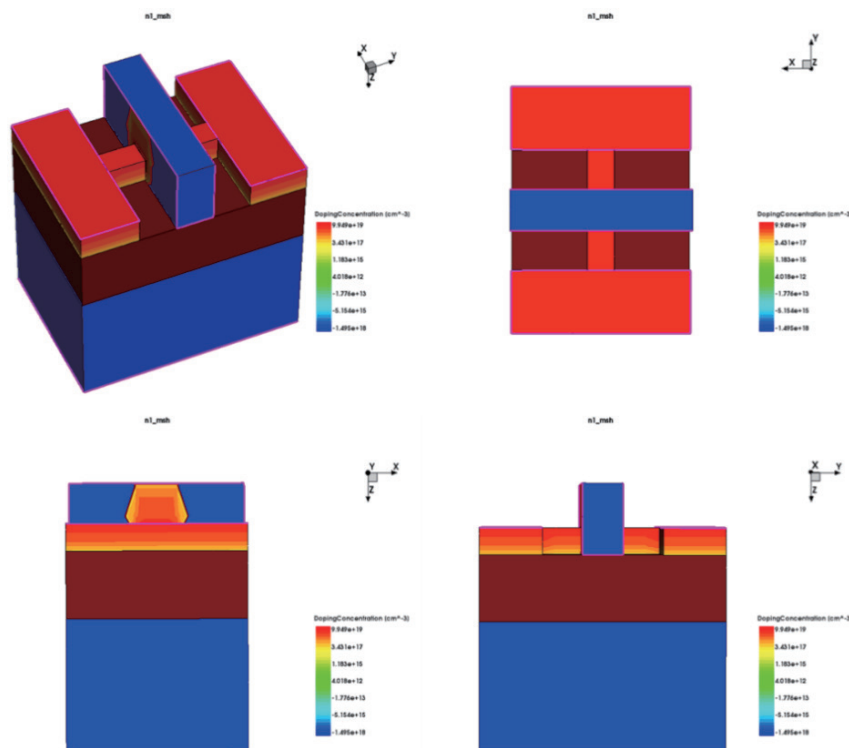


Fig. 1. (Color online) 3D schematic diagram of SOI-FinFET doping model.

doped with boron atoms in a uniform doping manner, with doping concentrations of $1.0 \times 10^{18} \text{ cm}^{-3}$ for the silicon substrate and $1.0 \times 10^{16} \text{ cm}^{-3}$ for the fishbone, source, and drain regions. Then, arsenic atoms are doped into the source, drain, source extension, drain extension, and channel regions by a Gaussian doping method. The maximum doping concentration of the channel region is $5.0 \times 10^{17} \text{ cm}^{-3}$, and that of the other four regions is $5.0 \times 10^{19} \text{ cm}^{-3}$.

2.2 Simulation of device electrical characteristics

After constructing the complete FinFET device model, the Sdevice module is used to simulate the DC and AC characteristics of the device. Figure 2 shows the transfer characteristics of the FinFET device. As shown in Fig. 2, the conductivity current of the FinFET device with a gate length of 90 nm is approximately $4 \times 10^{-5} \text{ A}$ at room temperature (300 K). The output characteristic curves of the device under different gate voltages are shown in Fig. 3.

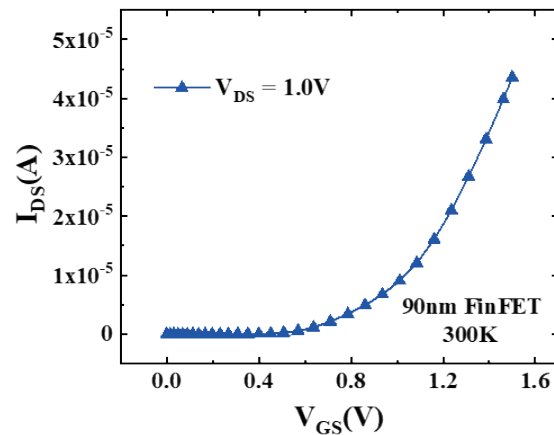


Fig. 2. (Color online) Transfer characteristic curve of SOI-FinFET.

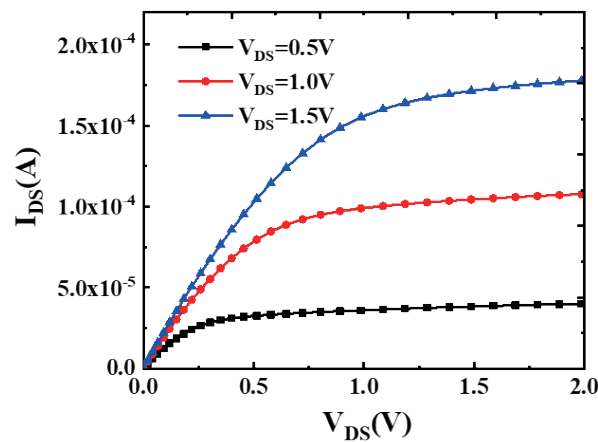


Fig. 3. (Color online) Output characteristic curves under different gate voltages.

3. Dataset Construction and Data Preprocessing

3.1 Selection of eigenvalues

In this article, TCAD simulation is used to predict the electrical characteristics of SOI-FinFET devices, so it is crucial to select the appropriate device structural parameters as inputs to predict the desired device electrical parameters for the subsequent network model construction and training. According to the working principle and device characteristics of the SOI-FinFET, it is known that gate length, fin width, fin height, and gate oxide layer thickness have a significant impact on the electrical characteristics of FinFET devices. Therefore, we initially selected the above four device structural parameters as input features. To intuitively feel the impact of the above four device structural parameters on the electrical characteristics, we here use the method of controlling variables to simulate the electrical characteristics of the four device structural parameters. As shown in Fig. 4, the gate length, fin width, fin height, and gate oxide layer thickness have a significant impact on the source–drain current I_{DS} of the device. The source–drain current of the device increases with increasing fin width, fin height, and gate oxide layer thickness, and decreases with increasing gate length. This is in line with the working principle of FinFET devices.

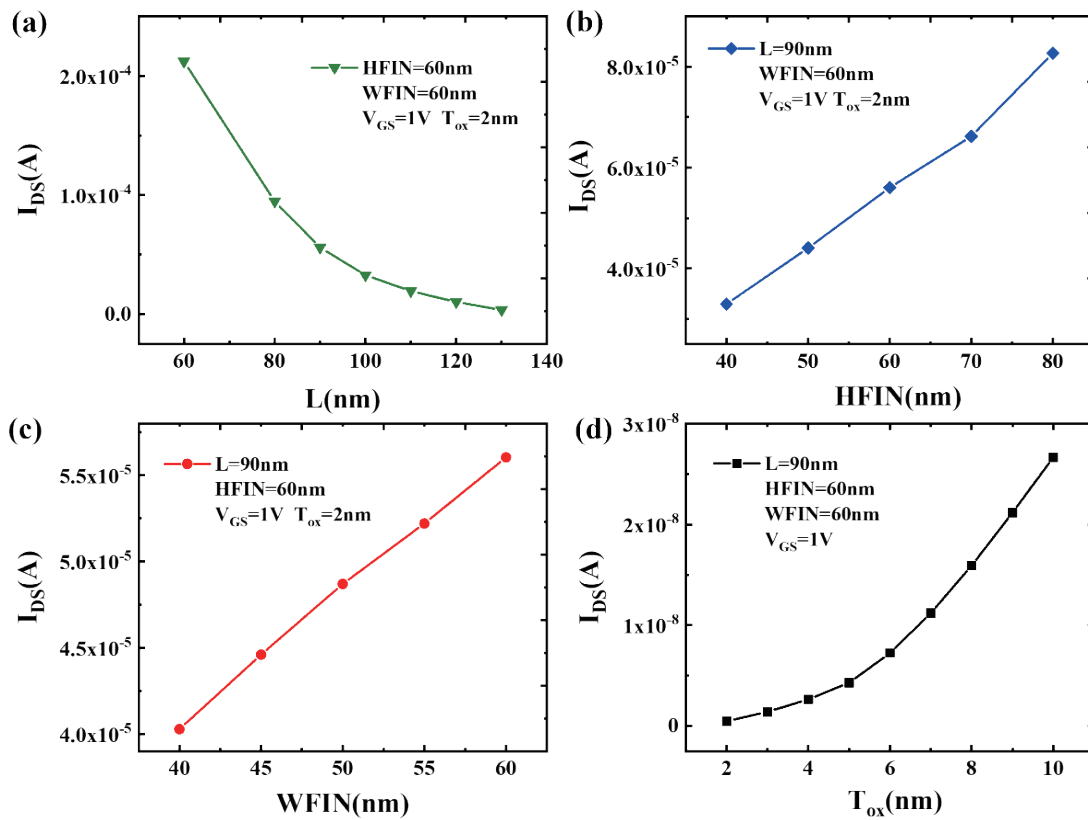


Fig. 4. (Color online) Changes in leakage current with (a) L , (b) H_{FIN} , (c) W_{FIN} , and (d) T_{ox} .

Figure 4 shows that the four device structural parameters, namely, gate length, fin width, fin height, and gate oxide layer thickness, have a significant impact on threshold voltage and sub-threshold swing, which are two important electrical characteristic parameters of the device. Therefore, it is reasonable to select them as input for the network; this is also in line with the working mechanism of SOI-FinFET devices.

3.2 Construction of datasets

After selecting the input and output feature variables for subsequent deep learning model training, the necessary simulation nodes are constructed using the Sentaurus TCAD simulation software; each node represents a set of device parameters simulated and calculated for a set of output electrical parameters. In this section, device structural parameters are initially configured in the order of gate length, fin width, fin height, and gate oxide layer thickness, where gate length L (unit: μm) increases from 0.09 to 0.14 incrementally by 0.005 in six steps, fin width W_{FIN} (unit: μm) increases from 0.04 to 0.06 incrementally by 0.005 in five steps, fin height H_{FIN} (unit: μm) increases from 0.04 to 0.06 incrementally by 0.005 in five steps, and gate oxide layer thickness T_{OX} (unit: μm) increases from 0.002 to 0.01 incrementally by 0.001 in nine steps. The five electrical parameters are extracted from the simulation results as output feature values using the previously described formulas.

A total of 1350 sample data points were simulated in this modeling process, and after eliminating samples with data abnormalities, the dataset contains 1315 sample data points, each of which includes four device structural parameters and five device electrical parameters. The magnitude of the data fluctuations is considerable. It is difficult to train a deep learning model that converges by directly feeding such data into the network. The input feature variables are subjected to matrix multiplication with the initial weights during forward propagation after being fed into the neural network. Then, the predicted output is compared with the true output, and finally, the loss is backpropagated to update the network weights by iterating the training process.

4. Prediction Model and Results

4.1 Prediction model

After multiple iterations of training, the network structure used for transfer characteristic curve prediction is shown in Fig. 5. The input consists of the four physical parameters of the FinFET device and the output consists of the points on the corresponding $I_{DS}-V_{GS}$ curve. In this model, the multi-layer perceptron (MLP) module has hidden the first convolutional layer of the original version and directly uses two 1×1 convolutional layers. This is a special optimization performed on the basis of the small input feature size of the dataset used in this article. Adding a max pooling layer after the first MLPConv1 can significantly reduce the total number of parameters in the deep learning model.

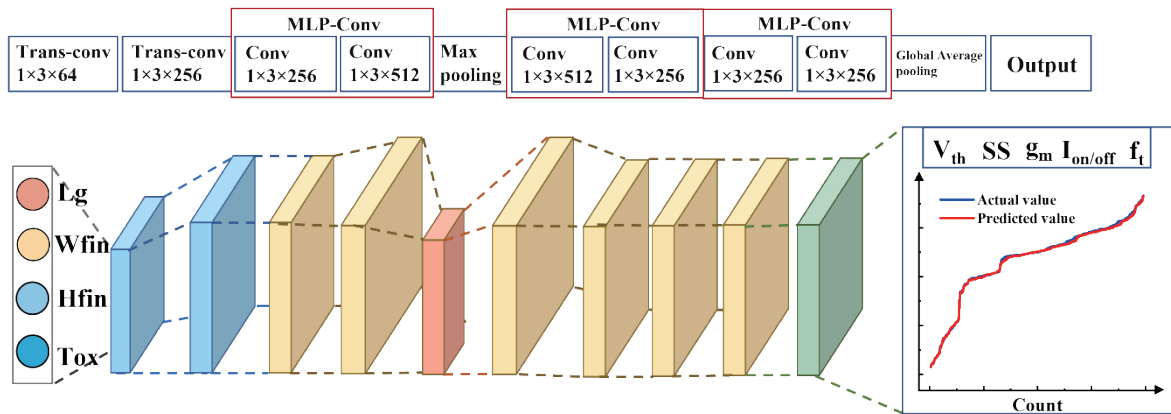


Fig. 5. (Color online) Structure diagram of deep learning model.

In this article, the dataset containing 1315 samples is divided into a training set and a test set in an 8:2 ratio. The training set includes 1052 samples and the test set includes 263 samples. The prediction input data for the experiment is randomly selected from the test set, with 198 samples in the prediction dataset. The dataset split is fixed and will not be changed. First, the training set is fed into the experimental model for iteration and weight correction. Then, the model training mode is turned off to stop updating the model weights, and the test set is fed into the experimental model to measure the quality of the model. During the training process, it is necessary to determine whether the training is converging and stop it in time according to the changes in training and test losses. In this article, the third-party monitoring library, Wandb (Weights & Biases), is introduced to dynamically monitor the training process by uploading the training and test losses of each epoch, thus enabling training to be stopped in time.

4.2 Results

After the multiple training iterations and modification of hyperparameters, the well-trained deep learning model is used to predict the electrical parameters of the previously determined prediction dataset. To easily compare the model-predicted and true label values, we first pair the predicted and true label values, and then sort the paired data in ascending order of the predicted values. Finally, the paired data are plotted as a line chart, and the predicted results are shown in Fig. 6. This method can clearly show the difference between the predicted and true label values, which aids in the evaluation of the prediction performance of the deep learning model.

In Fig. 7, the mean square error (MSE) losses of threshold voltage, subthreshold swing, transconductance, current ON/OFF ratio, and cut-off frequency are 6.51×10^{-5} , 5.42×10^{-5} , 9.76×10^{-3} , 2.76×10^{-4} , and 3.44×10^{-3} , respectively. The total MSE loss of the model prediction is 2.72×10^{-3} .

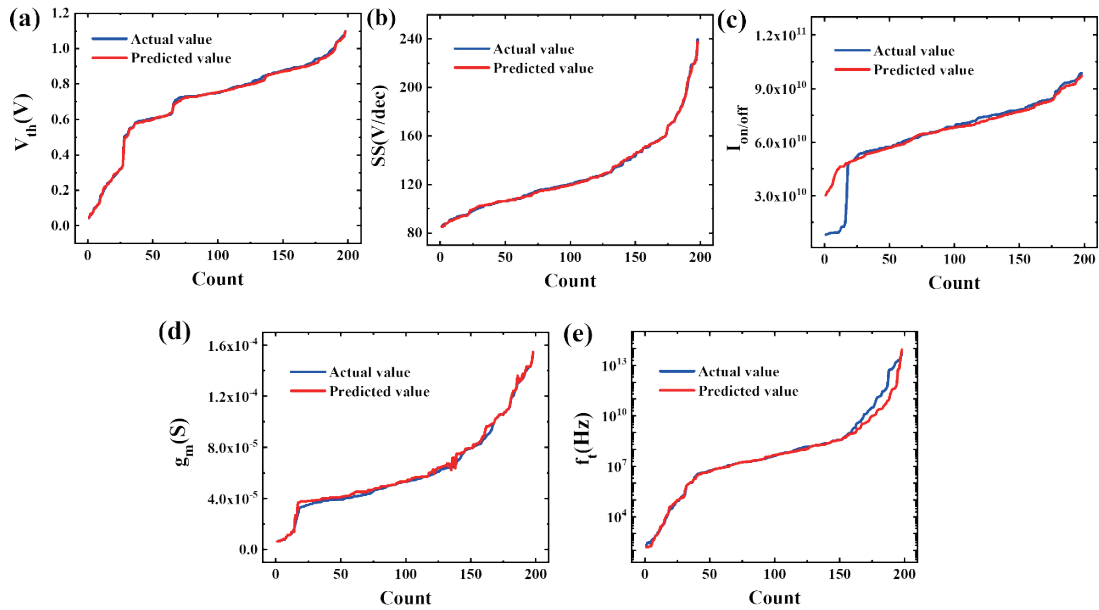


Fig. 6. (Color online) Model output diagram.

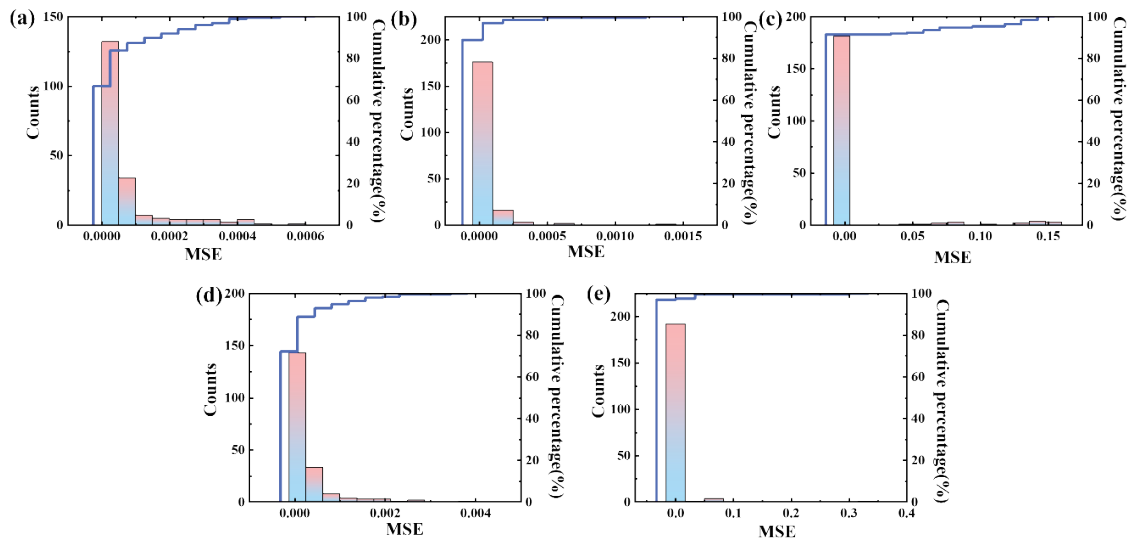


Fig. 7. (Color online) Prediction error statistics.

5. Conclusions

We mainly predicted the electrical characteristics of FinFET devices. We selected the widely used FinFET devices for simulation and constructed deep learning models to predict the electrical characteristics of FinFET and HEMT devices. Referring to the simulated datasets, we proposed a prediction method based on deep learning models to accelerate device simulation. This method provides a new paradigm for the design and modeling of FinFET devices, and establishes a new link between manufacturing factories and circuit and device designers.

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References

- 1 D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu: IEEE Trans. Electron Devices **47** (2000) 2320. <https://doi.org/10.1109/16.887014>
- 2 S. M. Jagtap and V. J. Gond: Int. J. Natural Computing Research **10** (2021) 12. <https://doi.org/10.4018/IJNCR.2021070102>
- 3 Y. Liu, T. Matsukawa, K. Endo, S. Ouchi, K. Sakamoto, J. Tsukada, Y. Ishikawa, H. Yamauchi, and M. Masahara: Int. Conf. Solid State Devices & Materials (2009) 1044. <https://doi.org/10.7567/SSDM.2009.C-7-3>
- 4 W.-T. Huang and Y. Li: Nanoscale Res. Lett. **10** (2015). <https://doi.org/10.1186/s11671-015-0739-0>
- 5 T. Ikegami, K. Fukuda, J. Hattori, H. Asai, and H. Ota: J. Comput. Electron. **18** (2019) 534. <https://doi.org/10.1007/s10825-019-01313-7>
- 6 A. Anam, S. I. Amin, and D. Prasad: IEEE Trans. Nano **23** (2024) 584. <https://doi.org/10.1109/TNANO.2024.3437669>
- 7 J. Jena, T. P. Dash, E. Mohapatra, S. Das, and J. Nanda: Int. J. High Speed Electron. Syst. **30** (2021). <https://doi.org/10.1142/S012915642140005X>
- 8 D. Li, T. Liu, Z. Wu, C. Cai, P. Zhao, Z. He, and J. Liu: Microelectron. Reliab. **114** (2020) 113901. <https://doi.org/10.1016/j.microrel.2020.113901>
- 9 I. Malkiel, M. Mrejen, A. Nagler, U. Arieli, L. Wolf, and H. Suchowski: Light Sci. Appl. **7** (2018) 60. <https://doi.org/10.1038/s41377-018-0060-7>
- 10 T. Asano and S. Noda: Opt. Express. **26** (2018) 32704. <https://doi.org/10.1364/OE.26.032704>
- 11 Z. Liu, D. Zhu, S. P. Rodrigues, K.-T. Lee, and W. Cai: Nano Lett. **18** (2018) 6570. <https://doi.org/10.1021/acs.nanolett.8b03171>
- 12 B. Sanchez-Lengeling and A. Aspuru-Guzik: Science **361** (2018) 360. <https://doi.org/10.1126/science.aat2663>
- 13 J. Gong, K. Xu, Z. Ma, Z. J. Lu, and Q. C. Zhang: Nat. Mach. Intell. **3** (2021) 995. <https://doi.org/10.1038/s42256-021-00412-0>
- 14 R. Zhao, S. Wang, X. Duan, C. Liu, L. Ma, S. Chen, and H. Liu: Nanotechnology **33** (2022) 335203. <https://doi.org/10.1088/1361-6528/ac6c95>
- 15 R. Zhao, S. Wang, X. Duan, X. Cao, L. Ma, S. Chen, H. Liu, Y. Chen, H. Zhang, and Y. Zhao: Nanotechnology **33** (2022) 505204. <https://doi.org/10.1088/1361-6528/ac9287>
- 16 R. Butola, Y. Li, and S. R. Kola: IEEE Access **10** (2022) 71356. <https://doi.org/10.1109/ACCESS.2022.3188690>
- 17 X. Zhang, S. Chen, B. Liu, X. Cao, D. Chen, L. Ma, and S. Wang: Adv. Theor. Simul. **6** (2023) 2200692. <https://doi.org/10.1002/adts.202200692>

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