Sensors and Materials, Vol. 37, No. 3 (2025) 911–920
MYU Tokyo

S & M 3965

Impact of Structural Changes in the Chip Carrier on the Heat Dissipation Performance of Power Transistors

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(Received January 27, 2025; accepted February 25, 2025)

Keywords: structural change, chip carrier area, heat dissipation performance, power transistor, heat transfer coefficient, power dissipation

In this study, we primarily employed COMSOL, a finite element method analysis software program, to investigate the heat dissipation of power transistors, with the TO-220 package design from Onsemi serving as a reference. The focus was on analyzing the structural parameters of the chip carrier and their impact on the thermal management of power transistors' packaging. By varying the structural parameters of the chip carrier within the packaging area, including its length, thickness, and height, we examined how these changes affect heat dissipation. The results of the analyses indicated that the presence of a chip carrier, as compared with the unsealed model, led to a reduction in maximum temperature by 15 °C. The simulation results demonstrate the importance of the chip carrier's design in enhancing thermal performance. The ultimate goal of this research was to modify the packaging model in such a way that the maximum temperature of the power transistor packaging was maintained below 175 °C. This temperature threshold is critical for ensuring the reliable operation and longevity of power transistors in high-performance applications. By optimizing the packaging design and improving heat dissipation, in this study, we contributed to the advancement of more efficient and durable power transistor solutions for next-generation electronic devices and systems.

1. Introduction

In Internet of Things (IoT) devices, the heat dissipation of power transistors becomes particularly crucial, as these devices often need to operate for extended periods in small, compact environments. Improper heat management can directly impact the stability, performance, and lifespan of the devices.[1–3] With the widespread adoption of IoT applications,

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https://doi.org/10.18494/SAM5578

ISSN 0914-4935
https://myukk.org/

the demand for higher performance, lower power consumption, and reliable long-term operation is continuously increasing. As a result, heat dissipation management for power transistors has become an essential part of the design process. In the context of IoT, the heat dissipation of power transistors plays a crucial role in maintaining the overall functionality and performance of devices. Power transistors generate heat during operation, particularly when subjected to high loads or switching frequencies. If the heat dissipation is inadequate, it can lead to overheating, which may result in transistor failure or a decrease in performance. Effective heat management also improves energy efficiency by ensuring that the transistors operate at lower temperatures, minimizing energy loss and reducing unnecessary waste.

Moreover, the lifespan of components is directly affected by their operating temperature, with excessive heat accelerating the aging process and shortening their service life. Proper heat dissipation helps maintain a stable operating environment, extending the overall longevity of IoT devices. As IoT devices become increasingly compact, the challenge of heat dissipation intensifies. With less space available for cooling, designers are required to use advanced technologies such as heat pipes, heat sinks, and miniature fans to ensure that the temperature of power transistors is effectively controlled without compromising the device's size. Additionally, the importance of managing heat extends to preventing system failures. Many IoT devices, such as smart home devices and wearables, need to operate continuously for long periods. Poor heat dissipation can cause overheating, which can disrupt connectivity and communication, ultimately affecting the stability of the entire IoT system.

Nowadays, there is a growing demand for devices to have more functions, which has led to the need for smaller and more efficient designs. The number of electronic components (such as power transistors) can be increased within the same area, allowing chips to perform more computations and thereby enhance performance. As a result, packaging technology for power transistors must also continue to advance. The development of packaging technology primarily addresses the technical need for power transistors to generate significant heat during operation. If this heat is not effectively dissipated, it can cause the components to overheat, negatively affecting their performance and lifespan, and potentially leading to failure. To ensure the stable operation of power transistors, efficient heat dissipation is crucial. Heat sinks are key components that transfer heat from the package to the surrounding environment. The thermal management design of power semiconductors is crucial for ensuring their proper operation, enhancing performance, and extending their lifespan. By ensuring component stability and reliability, the effective heat dissipation management of power transistors can maximize the performance of power devices.

Common methods for cooling power transistors include the use of heatsinks with suitable heat dissipation materials[4] and using fans[5] or liquid cooling systems[6] to efficiently transfer heat from the heat source to the dissipation area. However, it is standard practice to include a heatsink for most power devices. Research focusing solely on modifying heatsink structural parameters to meet the thermal requirements of power semiconductors—without incorporating additional structures or materials such as fan cooling and liquid cooling systems, or heat pipes—is relatively scarce. In this study, therefore, a simulation method was utilized to alter heatsink structural parameters in order to identify the optimal heat dissipation model. Proper packaging

size and shape design help optimize thermal performance, ensuring that heat is evenly distributed and rapidly conducted to the exterior of the package.[7] In this project, we primarily used COMSOL simulation software for modeling.[8,9] By analyzing a large number of different models, the goal is to assist future researchers in designing power transistor heat dissipation structures. In this paper, we aimed to provide a reference, allowing them to directly select the optimal parameters, significantly reducing production costs.

2. Simulation Parameters

The TO-220 package design from Onsemi was used as a reference for our analyses of the heat dissipation of power transistors. In the initial phase, we compared the temperature variations between two different scenarios, one where the device was packaged and the other where it was not. This comparison of two different package conditions would help us understand the impact of packaging on thermal performance. The detailed structural diagram for the simulation of the power transistor package is provided in Figs. 1(a) and 1(b), which illustrate the layouts of with and without package (chip carrier). In the following steps, we explored how adjustments to these chip carrier parameters affected the thermal behavior of the component, specifically its temperature characteristics under different conditions. In this investigation, we aimed to provide a deeper understanding of how the chip carrier structure affects heat dissipation and the overall thermal management of power devices.

The motivation for the change was to find whether the structure of the chip carrier had reached its optimal design. To achieve this, we scaled up the chip carrier structure to investigate whether it could further reduce the temperature of the power transistor packaging compared with the original design. The structural parameters of the chip carrier were length, thickness, and height. Initially, we analyzed one of these parameters, including the variations in length (Fig. 2), thickness (not shown here), and height (Fig. 3). Afterward, we simultaneously varied all three parameters, optimizing them individually. Finally, we compared the results obtained using

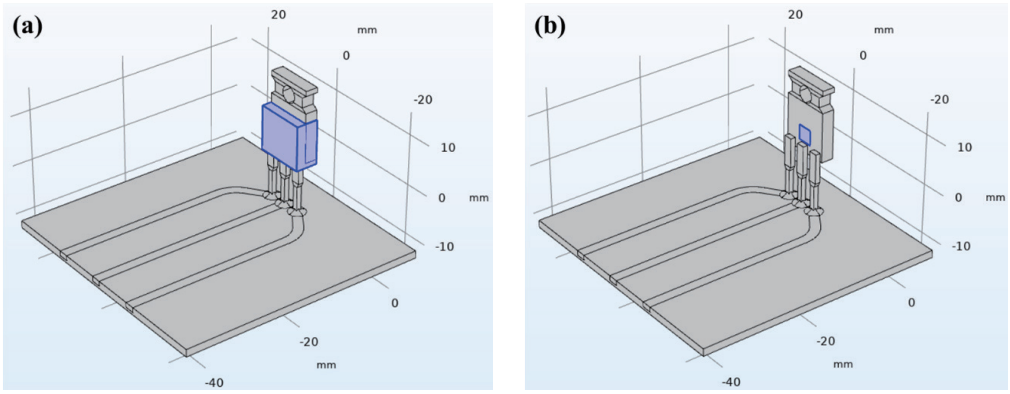

Fig. 1. (Color online) Complete structural model of the power transistor: (a) with chip carrier (indicated by blue markings) and (b) without chip carrier.

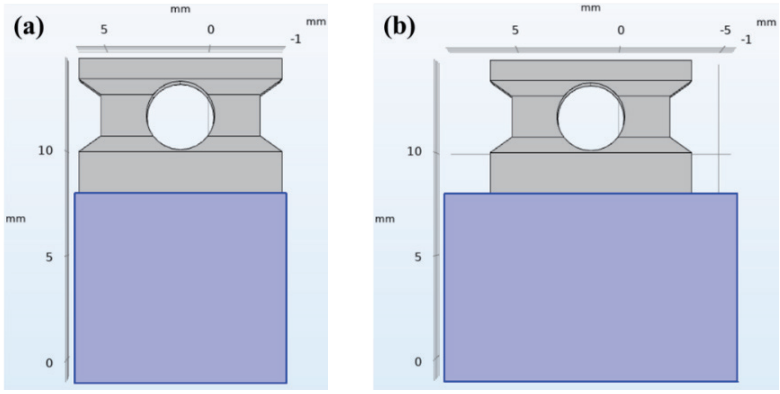

Fig. 2. (Color online) Length variation diagram: (a) original structure length (10 mm) and (b) maximum length (14 mm).

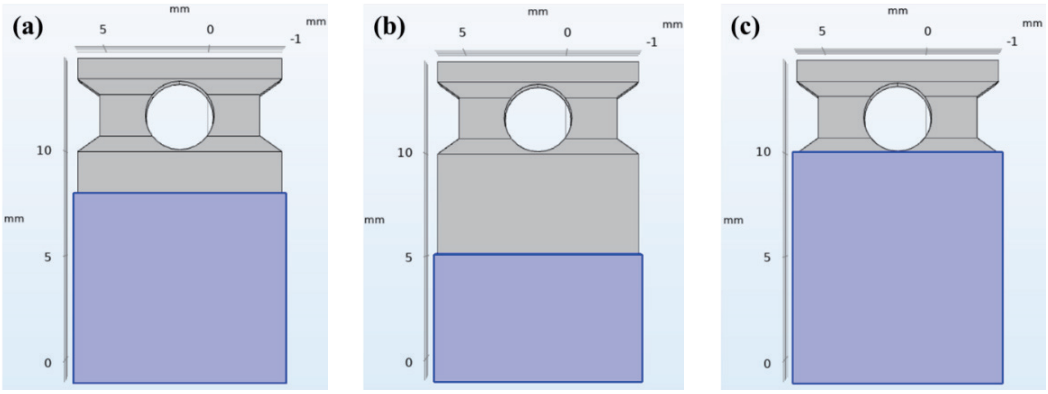

Fig. 3. (Color online) Height variation diagram: (a) original structure height (9 mm), (b) minimum height (6.1 mm), and (c) maximum height (11 mm).

the optimal parameters with the original structure to assess the impact on heat dissipation. This comprehensive approach allowed us to evaluate the effectiveness of structural modifications and their potential to improve thermal performance. The mesh data we set included a total of 112129 finite elements, with a minimum element quality of 0.06506, an average element quality of 0.64, and an element volume ratio of 1.843×10^{-5}.

3. Simulation Results and Discussion

To evaluate the impact of packaging on the thermal performance, we compared the increases in the temperature of a power transistor in both unencapsulated and encapsulated states. As shown in Fig. 4, under an ambient temperature of 25 °C, with a heat transfer coefficient (HTC) of 5 W/(m^2·K) and a power dissipation (PD) of 4 W, the highest temperature of the unencapsulated model increased to 185.2 °C, while the highest temperature of the encapsulated model increased to 170 °C. On the basis of our simulation results, we can conclude that, with packaging, the

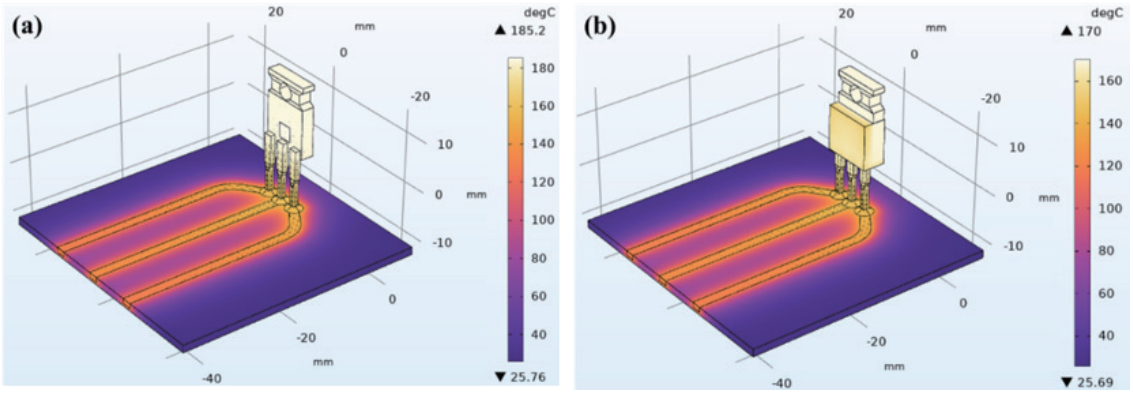

Fig. 4. (Color online) Comparison of packaging models: (a) unencapsulated and (b) encapsulated.

maximum temperature decreased by at least 15 °C. This result demonstrates that our simulated packaging model significantly contributes to improving thermal performance. Therefore, we can further modify the packaging model in subsequent studies to explore whether it has reached the optimal design for heat dissipation.

Next, we simulated the effects of the HTC and PD. Once we set the standard parameters for these two factors, we then compared the real impact of different packaging models on heat dissipation performance. The convective environment had a significant effect on heat dissipation, so we simulated both natural and forced convection conditions at an ambient temperature of 25 °C. In natural convection, the HTC was set to 5 W/(m^2·K), whereas in forced convection, it was set between 25 and 100 W/(m^2·K). As shown in Fig. 5, we simulated PD values ranging from 1 to 16 W to determine how much the highest temperature of the power transistor packaging increased. For an HTC of 5 W/(m^2·K) and a PD of 4 W, the highest temperature increased from 66.13 to 199.7 °C. With an HTC of 25 W/(m^2·K) and a PD of 8 W, the highest temperature increased from 46.31 to 186.5 °C. When the HTC was 50 W/(m^2·K) and the PD was 11 W, the highest temperature increased from 39.79 to 183.1 °C. At an HTC of 100 W/(m^2·K) and a PD of 17 W, the highest temperature increased from 34.94 to 182.7 °C. These results showed that increasing the HTC significantly improves the PD capability of the packaged power transistor. However, since the maximum operating temperature of the TO-220 model we are using is 175 °C, we set the HTC to 100 W/(m^2·K) and the PD to 15.5 W. Under these conditions, the highest temperature is 177.9 °C. Our goal is to modify the packaging model under these conditions to reduce the highest temperature of the power transistor packaging to below 175 °C.

The original length of the TO-220 chip carrier was 10 mm, as shown in Fig. 6(a). When the packaging length increased from 10 to 14 mm and the thickness and height of the chip carrier were 4.5 and 9 mm, respectively, the maximum temperature decreased from 177.9 to 173.7 °C, and the minimum temperature dropped from 88.8 to 68.08 °C. By altering the chip carrier length, the maximum temperature was reduced by 4.2 °C, while the minimum temperature decreased by 20.72 °C. The primary reason for the reduction in maximum temperature is that as the length of the chip carrier increases, the larger packaging space helps to lower the internal heat flux, as seen in Fig. 6(b). During the simulation, certain areas are shown to have high heat

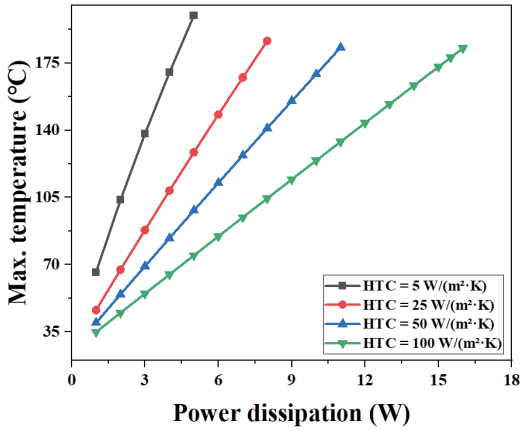

Fig. 5. (Color online) Variation of maximum temperature with PD at different HTCs.

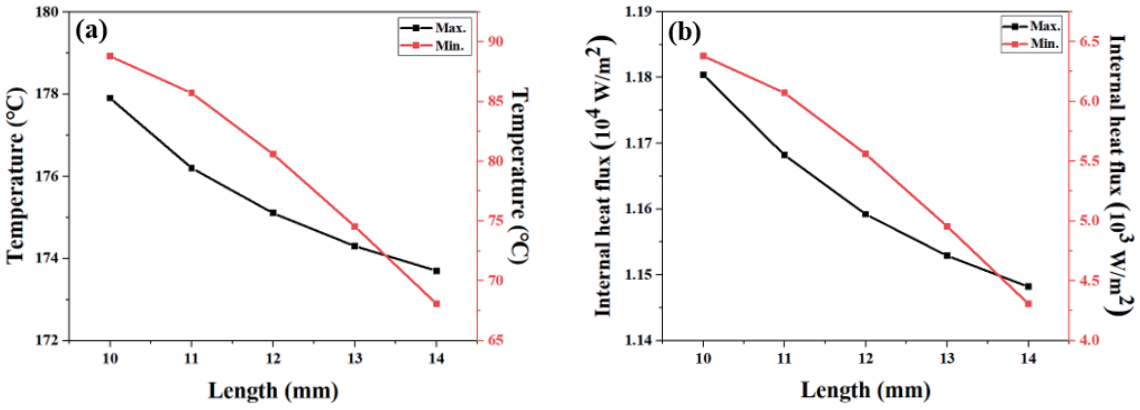

Fig. 6. (Color online) (a) Temperature and (b) internal heat flux variations with chip carrier length.

concentrations, indicating that heat is flowing from high-temperature regions to low-temperature regions. However, simply increasing the length of the chip carrier does not continuously decrease the temperature. When the length of the chip carrier reaches 13 mm, the decrease in maximum temperature begins to level off. This trend corresponds to the decrease in maximum internal heat flux, as shown in Fig. 6(b). Therefore, we have chosen to increase the chip carrier length to a maximum of 14 mm.

A more significant drop in minimum temperature occurs because the position in the chip carrier is more external. Compared with the original model, the heat transmitted from the center of the package (where the chip area is located) to the external areas is considerably reduced. Since the benefit of further decreasing the maximum temperature is marginal when the chip carrier length reaches 14 mm, the optimal length of the chip carrier is set to 13 mm, at which point the maximum temperature is 174.3 °C. The relationship between the chip carrier length and the temperature distribution indicates that increasing the chip carrier length effectively reduces both the maximum and minimum temperatures, with the greatest benefit achieved by extending the length to up to 13 mm. The reduction in maximum temperature is attributed to the

increased space for heat dissipation, which lowers the internal heat flux. However, beyond 13 mm, the benefits in terms of maximum temperature reduction are minimal. Therefore, setting the chip carrier length at 13 mm strikes an optimal balance between temperature reduction and package size. This approach enhances thermal management without unnecessarily increasing the package size, making it a practical solution for improving device performance and reliability.

The temperature distributions of the TO-220 chip with different chip carrier thicknesses are shown in Fig. 7, with the length and height of the chip carrier being 13 and 9 mm, respectively. The original packaging thickness of the TO-220 chip carrier was 4.5 mm, as shown in Fig. 7(a). As the packaging thickness increased from 3.7 to 9 mm, as shown in Figs. 7(b) and 7(c) and in Fig. 8(a), the maximum temperature decreased from 178.8 to 176.7 ℃. The intermediate temperature dropped from 148.6 to 65.9 ℃, and the minimum temperature decreased from 112.4 to 42.4 ℃. By changing the thickness of the chip carrier, the maximum temperature decreased by 2.1 ℃, the intermediate temperature decreased by 82.7℃, and the minimum temperature decreased by 70 ℃. The primary reason for the decrease in maximum temperature is that, as the chip carrier thickness increases, the larger packaging space helps reduce the internal heat flux. Similarly, the temperature distribution in the simulation results shows that the negative sign indicates the flow of heat from high-temperature areas to low-temperature areas. However, increasing the chip carrier thickness does not always lead to continuous temperature reduction. As shown in Fig. 8(a), when the chip carrier thickness reaches 8 mm, the trend of maximum temperature reduction begins to level off, which corresponds to the trend of decreasing internal

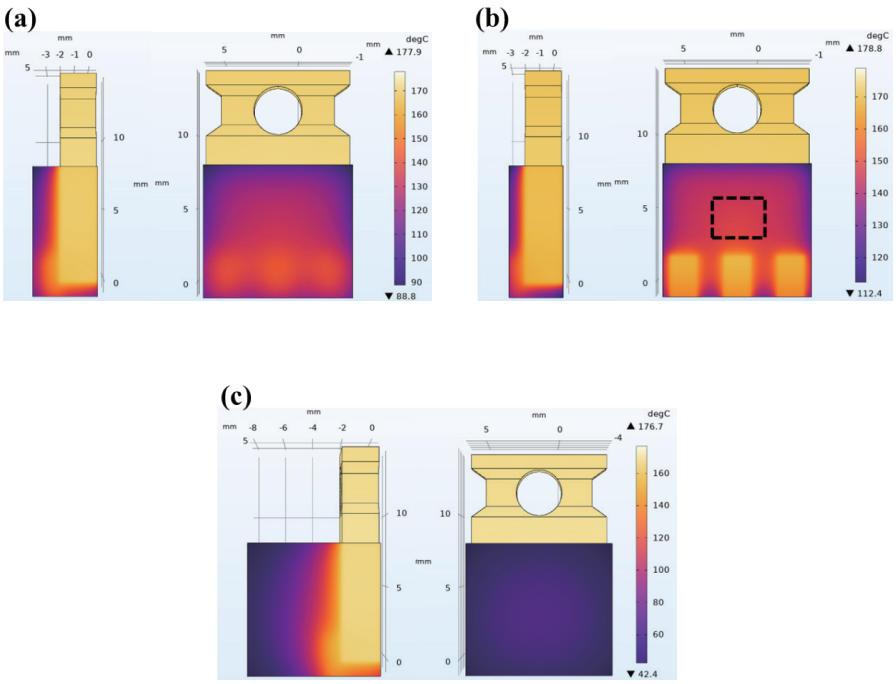

Fig. 7. (Color online) Temperature variation with different chip carrier thicknesses: (a) original thickness (4.5 mm), (b) minimum thickness (3.7 mm), and (c) maximum thickness (9 mm).

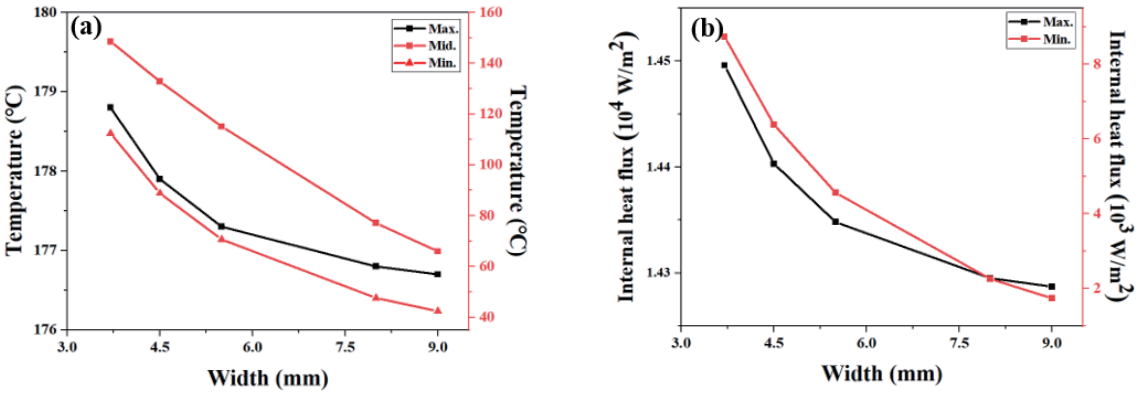

Fig. 8. (Color online) (a) Temperature and (b) internal heat flux variations with chip carrier thickness.

heat flux, as shown in Fig. 8(b). Therefore, we limit the chip carrier thickness to a maximum of 9 mm.

The more significant temperature reductions at the intermediate and minimum temperatures are due to their locations being farther out from the core of the packaging model. As heat is transmitted from the central chip region to these outer areas, the temperature naturally decreases more significantly. Compared with altering the chip carrier's length and height, changing the thickness has a more notable effect on the thermal performance. Since the reduction in maximum temperature becomes marginal when the chip carrier thickness reaches 9 mm, we determined that the optimal chip carrier thickness is 5.5 mm, where the maximum temperature is 177.3 °C. This analysis result emphasizes that optimizing the chip carrier thickness is an effective way of improving the thermal performance of the packaging. However, there is a diminishing return as the chip carrier thickness increases beyond a certain point. Therefore, choosing an optimal chip carrier thickness—rather than simply increasing it as much as possible—is crucial for achieving a balance between effective thermal management and design constraints.

The original height of the TO-220 chip carrier was 9 mm. As the package height increased from 6.1 to 11 mm, while the length and thickness of the chip carrier were 13 and 5.5 mm, respectively, the maximum temperature decreased from 178.5 to 177.4 °C and the minimum temperature decreased from 90.13 to 88.36 °C. By changing the height of the chip carrier, the maximum temperature dropped by 1.1 °C and the minimum temperature dropped by 1.77 °C, as shown in Fig. 9(a). The main reason for the reduction in maximum temperature is that as the chip carrier height increases, the larger packaging space reduces the internal heat flux, as illustrated in Fig. 4. On the other hand, the minimum temperature does not decrease significantly because the modified area still contacts the metal backplate. Therefore, the temperature transmitted from the central chip region of the package model does not experience a substantial drop. The temperature change in the chip carrier also correlates with changes in maximum internal heat flux, as shown in Fig. 9(b). Although changing the height has a smaller effect on the maximum temperature, increasing the height by 1 mm results in a 0.2 °C decrease in maximum temperature. Owing to the structural limitations of the TO-220 chip, the maximum height that we can have is 11 mm. Therefore, we set the optimal height of the chip carrier at 11 mm, at which point the maximum temperature reaches 177.4 °C.

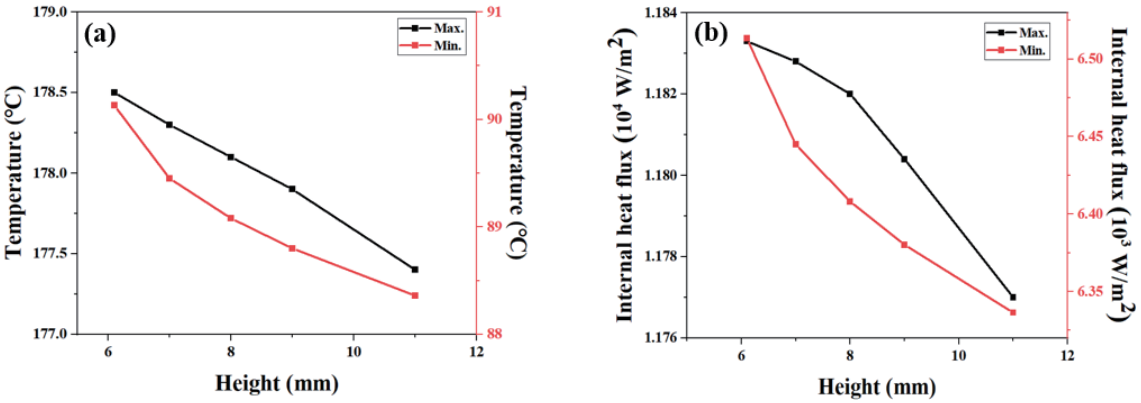

Fig. 9. (Color online) (a) Temperature variation and (b) internal heat flux variation with chip carrier height.

The height variation in the TO-220 chip carrier significantly affects the temperature distribution within the package. By increasing the height, we introduce a larger volume for heat dissipation, which directly impacts the thermal efficiency of the system. However, the benefits in terms of maximum temperature reduction become marginal beyond a certain height increase. One notable observation is that the minimum temperature sees a smaller reduction, which can be attributed to the fact that the contact with the metal backplate still channels some heat away, limiting the cooling effect in the lower regions. The result suggests that while height adjustments can optimize heat management to a certain extent, other factors such as material conductivity and backplate efficiency should also be considered to achieve more substantial temperature reductions in both maximum and minimum regions. In practice, given the constraints of the TO-220's design, the optimal height of 11 mm provides a balanced solution, reducing the maximum temperature to a safe operating level while ensuring that the chip remains within operational thresholds. This approach underscores the importance of considering both the thermal and physical design limitations when optimizing electronic component performance.

4. Conclusions

As the packaging length increased from 10 to 14 mm, with the thickness and height of the chip carrier fixed at 4.5 mm and 9 mm, respectively, the maximum temperature decreased from 177.9 to 173.7 °C, while the minimum temperature dropped from 88.8 to 68.08 °C. The optimal length was determined to be 13 mm. When the length and height of the chip carrier were set at 13 and 9 mm, respectively, and the packaging thickness was increased from 3.7 to 9 mm, the maximum temperature decreased from 178.8 to 176.7 °C. The intermediate temperature dropped from 148.6 to 65.9 °C, and the optimal thickness was found to be 5.5 mm. As the chip carrier height increased from 6.1 to 11 mm, with the length and thickness fixed at 13 and 5.5 mm, respectively, the maximum temperature decreased from 178.5 to 177.4 °C and the minimum temperature decreased from 90.13 to 88.36 °C. By changing the height of the chip carrier, the maximum temperature dropped by 1.1 °C and the minimum temperature decreased by 1.77 °C. The research model presented in this paper can serve as a valuable reference for the design of

power transistor packaging in future 5G and IoT applications. This model offers insights that can guide engineers and designers in optimizing packaging solutions, ensuring that they meet the performance, efficiency, and reliability requirements necessary for these advanced technologies.

Acknowledgments

This research was supported by "Guangdong Science and Technology Program", "Lagrangian Coherent Structure Analysis of Heat Sink for Heat Transfer Performance with Piezoelectric Fan. (No. 2024A0505050022)", Summit-Tech Resource Corp., and by projects under Nos. NSTC 113-2622-E-390-001 and NSTC 113-2221-E-390-011. We would also like to thank Pitotech Co., Ltd. for their help in the use of COMSOL Multiphysics® software.

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