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Analyzing Noise Margin Degradation in Subthreshold Nanosheet Transistor Logic Gates: An Interface Quasi-Fermi Potential Model for Interface-trapped Charge Effects

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On the basis of the continuity of subthreshold current at the interface of trapped charges in the channel between fresh and damaged regions, a new interface quasi-Fermi potential (IQFP) model for the nanosheet FET with interface-trapped charges (ITCs) is developed. With the IQFP, the subthreshold current degraded by the ITCs for both N-FET and P-FET can be completely developed. We found that the IQFP can be strongly affected by both the distribution and polarity of the ITCs. Owing to the distribution of positive/negative ITCs near the drain side for N-FET/P-FET, the decreased threshold voltage will cause noise margin (NM) degradation. In contrast, the threshold voltage will be increased by the distribution of negative/positive ITCs near the source side for N-FET/P-FET, which resists the degradation of the NM. The NM caused by the balanced transistor strength between P-FET and N-FET can be monitored using the IQFP. This model can also be extended to other multi-channel-potential FETs comprising the subthreshold logic gate.

1. Introduction

Multiple-gate (MG) FETs[1–3] have attracted considerable attention due to their inherent robustness against short-channel effects (SCEs) when the gate length is scaled down to the nanometer regime. Among MG FETs, the nanosheet (NS) FET[4–15] with full gate coverage will provide the best short-channel behavior in comparison with other MG FETs. Aside from the best immunity to SCEs, the NS FET with multiple channels can provide sufficient driving current to pull-up the subsequent circuits with large fan-outs. The channel potentials for the device can be split into different regions corresponding to the different boundary conditions caused by interface-trapped charges (ITCs). For instance, the positive/negative ITC spread near the drain side for N-FET/P-FET will split the channel potential into two regions. One region near the source side will provide the low/high minimum channel potential and the other region near the

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drain side for N-FET/P-FET will provide the high/low minimum channel potential. Owing to the different profiles of channel potential between the source and the drain, the interface quasi-Fermi potential (IQFP) is necessary to calculate the subthreshold current in the entire channel region. Up to now, there are no studies on how the IQFP is related to the subthreshold current for devices with different profiles of channel potentials. As for the single-channel potential device, the IQFP is equal to the drain voltage. The IQFP is the function of device parameters such as oxide thickness, silicon thickness, doping density, and gate work function. This is the first time that the IQFP is derived from the continuity of the subthreshold current based on a quasi-3D scaling equation. With the IQFP, the noise margin (NM) for the subthreshold logic gate of the inverter composed of the NS FET can be theoretically and thoroughly evaluated.

2. Model Description

2.1 Quasi-3D scaling equation for NS FET with ITC

As shown in Fig. 1, the channel potential distribution for the NS FET working in the subthreshold region can be split into two regions. Region 1 of the fresh zone illustrates the channel potential without the ITC. Region 2 of the damaged zone exhibits the channel potential

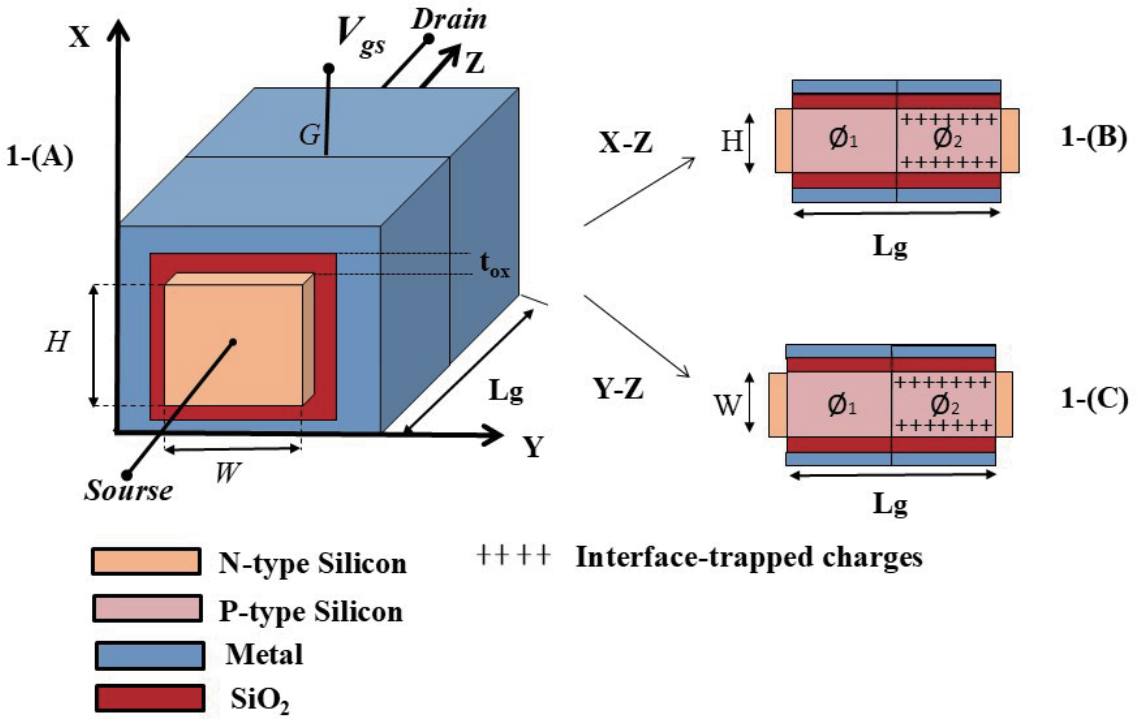

Fig. 1. (Color online) 1-(A) 3-D NS MOSFET schematic with ITCs. 1-(B) 2-D NS MOSFET with the *x*-*z* cut-plane that shows the two-region channel potential with the scaling length of λ_H. 1-(C) 2-D NS MOSFET with the *y*-*z* cut-plane that shows the two-region channel potential with the scaling length of λ_W. ITCs are assumed to be distributed near the drain side, as shown in 1-(B) and 1-(C).

with the ITC. On the basis of the quasi-3D scaling equation,[16–19] the central channel potential with the central conduction mode in two regions (i = 1, 2) can be expressed as

$$\frac{d^2\Phi_{Ci}(z)}{dz^2}+\frac{\Phi_{Ci}(z)-\phi_{CLi}}{\lambda^2}=0,\quad i=1,2 \tag{1}$$

with

$$\phi_{CLi}=V_{gs}-V_{fbi}-\frac{qN_{ai}\lambda^2}{\varepsilon_{si}},\lambda=\frac{1}{\lambda_{QG}{}^2}=\frac{1}{\lambda_H{}^2}+\frac{1}{\lambda_W{}^2},\quad i=1,2 \tag{2}$$

$$V_{fbi}=\Phi_m-\Phi_s-\frac{qN_{fi}}{C_{ox}},\ i=1,2 \tag{3}$$

where ϕ_{CLi} is the long-channel central potential defined by Eq. (2). The scaling length in Eq. (1) can be expressed by Eq. (2). l_W and λ_H are the quasi-2D scaling lengths in the x-z and y-z cut-planes, respectively. The flat-band voltage V_{fbi} in Eq. (3) is the work-function difference between the gate and the silicon body (i.e., V_{fbi} =F_{mi} − F_{si} − qN_f/C_{ox}). The ITC can induce the flat-band voltage shift qN_f/C_{ox}, where N_f is the surface density of ITC and C_{ox} is the capacitance per unit area for the gate oxide.

2.2 IQFP model

According to our previous work,[16] the subthreshold currents of the NS FET in the channel regions 1 and 2 can be expressed as

$$I_{subi}=I_{oi}\left(e^{-V_{i1}/V_T}-e^{-V_{i2}/V_T}\right)e^{\Phi_{C,mini}/V_T},\quad i=1,2 \tag{4a}$$

with

$$I_{oi}=\frac{\pi\mu_n n_i{}^2kT}{a_ib_iN_aL_i}\left[\mathrm{erf}\left(a_i\frac{H}{2}\right)\right]\left[\mathrm{erf}\left(b_i\frac{W}{2}\right)\right],\ i=1,2 \tag{4b}$$

where the IQFP of V_{IQFP} in the channel regions 1 and 2 can be expressed as

$$V_{i1}\big|_{i=1}=0,V_{i2}\big|_{i=1}=V_{IQFP},V_{i1}\big|_{i=2}=V_{IQFP},V_{i2}\big|_{i=2}=V_{ds},L_2=L_g-L_1. \tag{5}$$

The parameters (a_1, b_1, a_2, b_2) shown in Eq. (4b) can be the same as those in our previous paper.[16] Owing to the continuity of the subthreshold current in regions 1 and 2 (i.e., I_{sub1}=I_{sub2}), the equation regarding the IQFP of V_{IQFP} shown in Eq. (5) can be expressed as

$$\frac{1-e^{\frac{-V_{IQFP}}{V_T}}}{e^{\frac{-V_{IQFP}}{V_T}}-e^{\frac{-V_{ds}}{V_T}}}=\frac{a_1b_1L_1e^{\frac{\Phi_{Cmin2}}{V_T}}\operatorname{erf}\left(a_2\frac{H}{2}\right)\operatorname{erf}\left(b_2\frac{W}{2}\right)}{a_2b_2L_2e^{\frac{\Phi_{Cmin1}}{V_T}}\operatorname{erf}\left(a_1\frac{H}{2}\right)\operatorname{erf}\left(b_1\frac{W}{2}\right)}. \tag{6}$$

After the calculation of Eq. (6), the IQFP of V_{IQFP} on the left-hand side of Eq. (6) can be obtained as

$$V_{IQFP}=V_T\times\ln\left(\frac{1+\gamma}{\gamma+e^{\frac{-V_{ds}}{V_T}}}\right) \tag{7}$$

with

$$\gamma=\frac{a_2b_2(L-L_1)e^{\frac{\Phi_{Cmin1}}{V_T}}\operatorname{erf}\left(a_1\frac{H}{2}\right)\operatorname{erf}\left(b_1\frac{W}{2}\right)}{a_1b_1L_1e^{\frac{\Phi_{Cmin2}}{V_T}}\operatorname{erf}\left(a_2\frac{H}{2}\right)\operatorname{erf}\left(b_2\frac{W}{2}\right)}. \tag{8}$$

By substituting Eqs. (7) and (8) into Eq. (4a), the subthreshold current for the NS FET in the channel region can be obtained. Any one of the subthreshold currents in regions 1 and 2 can stand for the subthreshold current of the entire device. The subthreshold current in region 1 is selected to demonstrate the subthreshold current for the NS FET. This leads to the following Eqs. (9a) and (9b).

$$I_{sub1}=I_{o1}\left(1-e^{-V_{IQFP}/V_T}\right)e^{\Phi_{C,min1}/V_T} \tag{9a}$$

$$I_{o1}=\frac{\pi\mu_n{n_i}^2kT}{a_1b_1N_aL_i}\left[\operatorname{erf}(a_1\frac{H}{2})\right]\left[\operatorname{erf}(b_1\frac{W}{2})\right] \tag{9b}$$

2.3 NM of NS FET with ITC

According to our previous paper,[16] the NM of the inverter with ITCs can be expressed as

$$NM=\begin{cases}NM_H=\dfrac{V_{dd}}{2}-\dfrac{\eta V_T}{2}-\dfrac{\eta V_T}{2}\left(\ln\dfrac{\beta_p}{\beta_n}+\ln\dfrac{2}{\eta}\right),\\ NM_L=\dfrac{V_{dd}}{2}-\dfrac{\eta V_T}{2}-\dfrac{\eta V_T}{2}\left(\ln\dfrac{\beta_n}{\beta_p}+\ln\dfrac{2}{\eta}\right),\end{cases} \tag{10}$$

where b_n and b_p are the transistor strengths for N-FET and P-FET, respectively, and η is the inverse of the subthreshold slope. NM_L and NM_H are NMs for the low- and high-level inputs, respectively. NM can be chosen as the minimum value between NM_L and NM_H. The transistor strength in Eq. (10) can be derived from Eq. (9) by linearizing $F_{c,min1}$ to the gate voltage. This leads to

$$I_{sub1} = I_{o1}\left(1-e^{-V_{IQFP}/V_T}\right)e^{2\Phi_B/V_T}e^{\left(V_{gs}-V_{th}\right)/\eta V_T} = \beta_n e^{V_{gs}/\eta V_T} \tag{11a}$$

with

$$\beta_n = I_{o1}\left(1-e^{-V_{IQFP}/V_T}\right)e^{2\Phi_B/V_T}e^{-V_{th}/\eta V_T}, \tag{11b}$$

where V_{TH} and Φ_B are the threshold and bulk voltages, respectively. b_n is the transistor strength for N-FET. The transistor strength for P-FET (i.e., b_p) can also be obtained by changing the polarity of doping density and applied voltages. Owing to the unbalanced transistor strength (i.e., $b_n \neq b_p$) caused by the ITC, the NM degradation can be monitored using the location, density, and polarity of the ITC.

3. Results and Discussion

A 3-D device simulator is used to validate the model.[20] Unless otherwise stated, the NS FET with the square shape of silicon for both P-FET and N-FET is assumed (i.e., $T_{si} = H = W$). Figure 2 shows the IQFP versus the channel length for different densities of positive ITCs near the drain side of N-FET. It indicates that as the channel length is decreased, the IQFP will be increased owing to SCEs, which brings about the increased subthreshold current. The higher positive ITC will induce the larger IQFP due to the threshold voltage decreased by SCEs. The

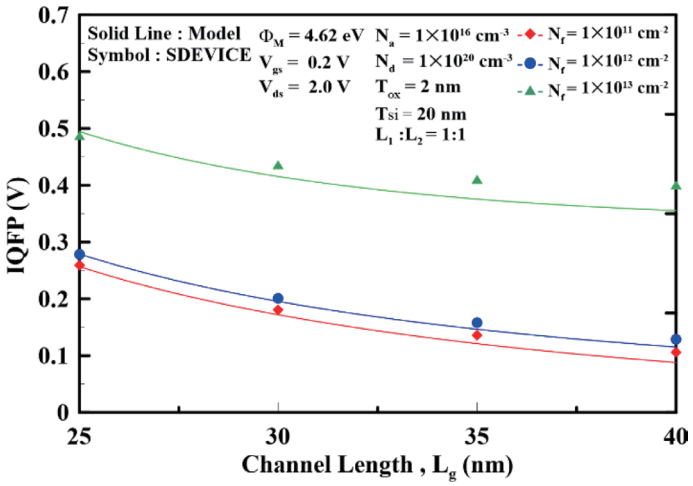

Fig. 2. (Color online) IQFP versus channel length for different densities of ITCs distributed near the drain side. The positive charge density and N-FET are assumed.

low positive ITC can follow the low subthreshold current near the drain side. Figure 3 shows the IQFP versus the channel length for different densities of negative ITCs near the drain side of P-FET. Similar results, as shown in Fig. 2, can be seen except for the polarity of the IQFP. The high subthreshold current induced by the low IQFP can be obtained by the high negative ITC distributed near the drain side of P-FET. From Figs. 2 and 3, it can be inferred that the negative/positive ITCs distributed near the source side of N-FET/P-FET will exhibit the low IQFP that results in the low subthreshold current. To monitor the *NM* degradation by the ITC, Fig. 4 shows *NM* versus the channel length for different densities of negative ITCs distributed near the source side of N-FET and the drain side of P-FET. It can be seen that the high negative ITC will keep

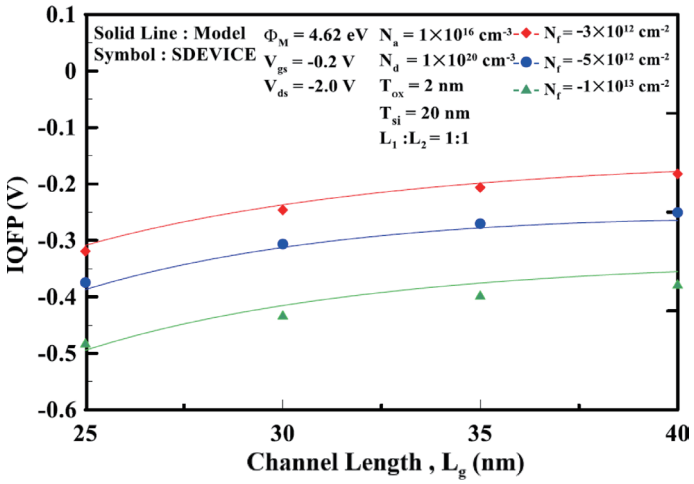

Fig. 3. (Color online) IQFP versus channel length for different densities of ITCs distributed near the drain side. The negative charge density and P-FET are assumed.

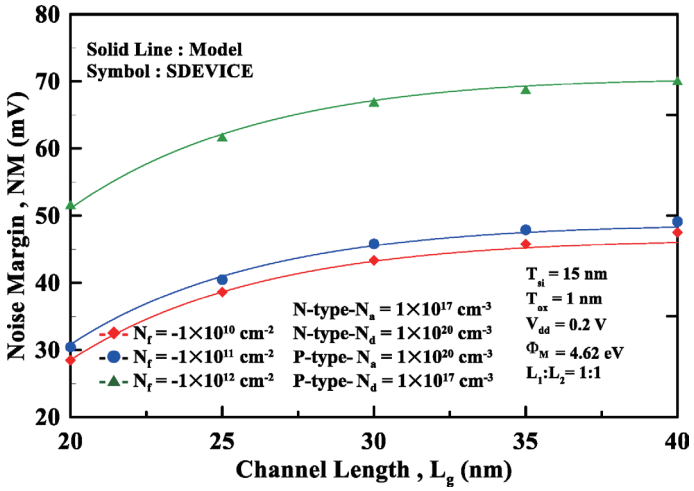

Fig. 4. (Color online) NM versus channel length for different densities of negative ITCs distributed near the source side of N-FET and the drain side of P-FET.

the high *NM*. In contrast, the low negative ITC will result in the low *NM* because strong SCEs that bring about the large imbalance of transistor strength between N-FET and P-FET are encountered. Figure 5 shows NM versus the channel length for different densities of positive ITCs distributed near the drain side of N-FET and the source side of P-FET. Unlike that shown in Fig. 4, the low positive ITC that effectively resists SCEs will result in the high *NM*. Figure 6 shows *NM* versus the channel length for damaged/fresh P-FET and N-FET. It indicates that NM for the fresh P-FET/N-FET will lie in between P-FET and N-FET with the positive and negative ITCs, respectively.

Note that the negative/positive ITCs will exhibit the highest/lowest *NMs* among the three cases. Although quantum confinement effects are not considered in this paper, if the quantum

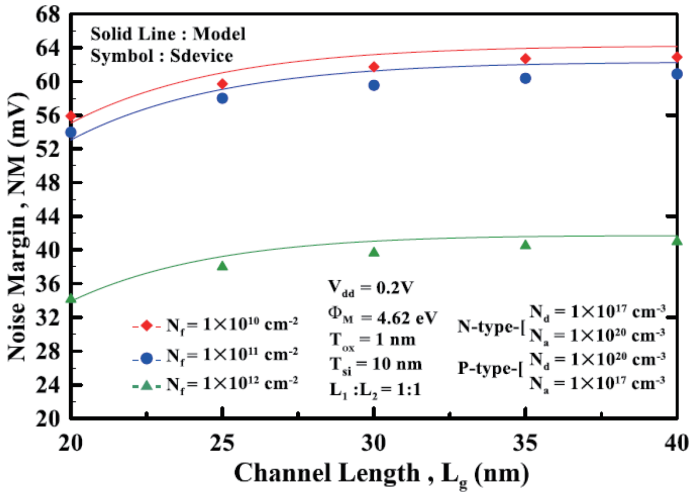

Fig. 5. (Color online) NM versus channel length for different densities of positive ITCs distributed near the drain side of N-FET and the source side of P-FET.

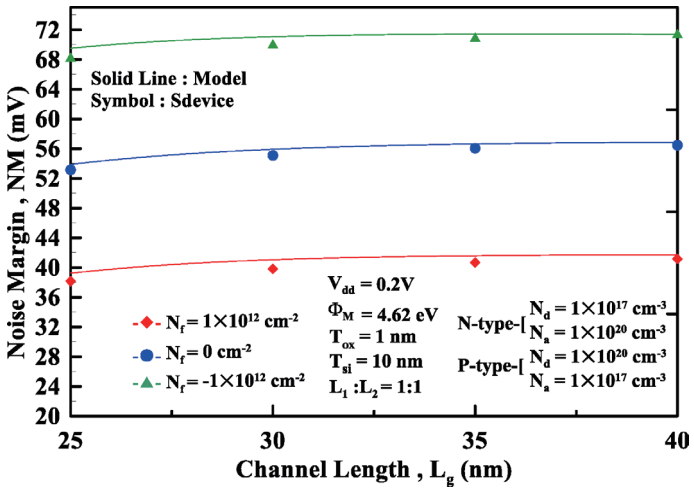

Fig. 6. (Color online) NM versus channel length for damaged/fresh P-FET and N-FET.

confinement effect is taken into account, its impact on the drive currents of P-FET and N-FET is basically the same, so the NM shown in Figs. 4–6 will not change.

4. Conclusions

We developed a novel IQFP model that establishes a unified framework for both subthreshold current calculation in multichannel devices and NM degradation analysis in logic gates under ITC effects. The IQFP formalism rigorously derived from quasi-3D scaling equations resolves current continuity challenges in two-channel potential devices by simultaneously addressing multi-region electrostatic coupling and quantum confinement effects. Beyond its immediate application in dual-channel systems, the model demonstrates extensibility to multi-channel architectures through the strategic development of multiple IQFPs at distinct channel interfaces, enabling the precise characterization of cross-sectional potential distributions in advanced NS transistors. Our analysis reveals fundamental ITC-NM degradation mechanisms: drain-side positive/negative ITCs in N-FETs/P-FETs reduce the threshold voltage to accelerate *NM* collapse, whereas source-side polarity-reversed ITCs enhance noise immunity through threshold voltage elevation. By correlating IQFP variations with transistor strength imbalance ($\beta n/\beta p$ ratio), we established a universal *NM* prediction framework validated across 15–50 nm channel lengths through 3D device simulations. This capability provides critical design guidelines for radiation-hardened circuits, including layout optimization to suppress drain-side charge accumulation ($<1 \times 10^{12}$ cm^{-2} ITC tolerance) and adaptive biasing strategies for threshold voltage compensation. The model's modular architecture bridges quantum device physics with circuit reliability engineering, offering scalability to gate-all-around nanowires and stacked NSs through generalized boundary condition formulations. Its compatibility with high-κ dielectric interface optimization and machine-learning-assisted 3-D device simulator parameter extraction positions it as an essential co-design tool for next-generation IoT and biomedical electronics demanding sub-100 nW operation.

References

1 Y. K. Lin, H. Agarwal, P. Kushwaha, M. Y. Kao, Y. H. Liao, K. Chatterjee, S. Salahuddin, and C. Hu: IEEE Trans. Electron Devices **66** (2019) 2023. https://doi.org/10.1109/ted.2019.2899810
2 G. Segev, I. Amit, A. Godkin, A. Henning, and Y. Rosenwaks: IEEE Electron Device Lett. **36** (2015) 651. https://doi.org/10.1109/led.2015.2434793
3 M.Gupta and A. Kranti: IEEE Trans. Electron Devices **66** (2019) 2704. https://doi.org/10.1109/ted.2019.2912209.
4 P. Y. Kuo, Z. H. Li, C. M. Chang, and P. T. Liu: IEEE Trans. Electron Devices **69** (2022) 4791. https://doi.org/10.1109/ted.2022.3188587
5 N. Choudhury and S. Mahapatra: IEEE Trans. Electron Devices **69** (2022) 3535. https://doi.org/10.1109/ted.2022.3172055
6 H. Wong and K. Kakushima: Nanomaterials **13** (2023) 411. https://doi.org/10.3390/nano13030411
7 S. Hong, M. Wu, Y. Hong, Y. Jeong, G Jung, W. Shin, J. Park, D. Kim, D. Jang, and J.-H. Lee: Sens. Actuators, B **330** (2021) 129240. https://doi.org/10.1016/j.snb.2020.129240
8 J. Zhang, L. Liu, Y. Yang, Q. Huang, D. Li, and D Zeng: Phys. Chem. Chem. Phys. **29** (2021) 15420. https://doi.org/10.1039/D1CP01890F
9 G. Jung, S. Hong, W. Shin, Y. Jeong, J. Park, D. Kim, and J.-H. Lee: Sens. Actuators, B **369** (2022) 132257. https://doi.org/10.1016/j.snb.2022.132257

10 W. Shin, Y. Jeong, S. Hong, G. Jung, J. Park, D. Kim, B.-G. Park, J.-H. Lee: Sens. Actuators, B **367** (2022) 132052. https://doi.org/10.1016/j.snb.2022.132052
11 C. Liu, B. Zhang, W. Chen, W. Liu, and S. Zhang: TrAC, Trends Anal. Chem. **143** (2021) 116334. https://doi.org/10.1016/j.trac.2021.116334
12 J. Wang, S. Xu, C. Zhang, A. Yin, M. Sun, H. Yang, C. Hu, H. Liu: InfoMat **5** (2023) e12376. https://doi.org/10.1002/inf2.12376
13 M.Sagarika and J. Zhang: Electronics 11.**21** (2022) 3589. https://doi.org/10.3390/electronics11213589.
14 A. S. Kumar, V. B. Sreenivasulu, M. Deekshana, G. Shanthi, and K. S. Rao: Integrated Devices for Artificial Intelligence and VLSI, B. Raj, S. L. Tripathi, T. Chaudhary, K. S. Rao, M. Singh, Eds. (Scrivener Publishing 2024), pp. 25–47. https://doi.org/10.1002/9781394205158.ch2
15 J. Ajayan, D. Nirmal, S. Tayal, S. Bhattacharya, L. Arivazhagan, A. S. A Fletcher, P. Murugapandiyan, and D. Ajitha: Microelectron. J. **114** (2021) 105141. https://doi.org/10.1016/j.mejo.2021.105141
16 T. K. Chiang: IEEE Trans. Electron Devices **63** (2016) 3354. https://doi.org/10.1109/TED.2016.2581826
17 T. K. Chiang: IEEE Trans. Nanotechnology **16** (2017) 16. https://doi.org/10.1109/TNANO.2016.2622246
18 T. K. Chiang: IEEE Trans. Electron Devices **65** (2018) 4535. https://doi.org/10.1109/TED.2018.2866372
19 T. K. Chiang: IEEE Trans. Electron Devices **68** (2021) 5330. https://doi.org/10.1109/ted.2021.3107817
20 SDEVICE: 3-D device simulator, Sentaurus, Synopsis 2000.

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