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48×32 Element Thermoelectric Infrared Focal Plane Array with Precisely Patterned Au-Black Absorber

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This paper presents a 48×32 element thermoelectric infrared focal plane array that provides high responsivity and potential for low cost . The device has a responsivity of 2100 V/W and a time constant of 25 ms. The overall chip size is 10.5 mm×7.4 mm with a 9.12 mm×6.08 mm imaging area. Each detector consists of six pairs of p-n polysilicon thermocouples, and has external dimensions of 190 μm×190 μm. The processes for obtaining a precisely patterned Au-black infrared absorbing layer and reducing the thermal stress of the Si_3N_4 layer deposited by LP-CVD achieve both high responsivity and an excellent time constant. This performance is suitable for automotive applications.

1. Introduction

The cooled infrared detectors that have been used in the past are not suitable for vehicles, largely because of their high price and the limited lifetime of the cooling system. As a result of advances in semiconductor technology, thermal infrared detectors have been developed in recent years that make use of a phase transition to achieve exceptionally high performance.[1, 2] These thermal infrared detectors have now advanced to the point where their performance is nearly comparable to that of their cooled counterparts. Examples of proposed applications to vehicles can be seen in the Advanced Safety Vehicle (ASV) Project in Japan[3] and night vision systems. However, there are various

factors that make it difficult to achieve low-cost uncooled detectors. For instance, infrared detectors that make use of a phase transition require precise temperature adjustments in the vicinity of the phase transition temperature, which necessitates the use of an add-on device such as a Peltier thermoelectric cooler. Another reason is that a pyroelectric sensor invariably has to be fabricated with a hybrid construction. Further cost reductions are necessary if thermal infrared sensors are to find widespread use in mass-produced vehicles. Toward this end, it is necessary to achieve a monolithic focal plane array (FPA) that will reduce the number of operations in the device fabrication process as much as possible, while still ensuring compatibility with the widely used CMOS process.

Among different types of thermal infrared sensors,[4–10] the thermopile[4,6,8] is the most promising infrared FPA for automotive use because of its potential for low cost and the fact that its electromotive force allows easy design of a latter-stage amplifier circuit. The performance of thermopiles is not necessarily sufficient for applications in vehicles at present, and further improvement will require better thermal isolation of the hot and cold junctions, a higher fill factor and higher infrared absorptivity.

Although gold black is known as an material that provides high absorptivity, a key factor in improving its sensitivity further is the Au-black layer fabrication technique. Since a Au-black layer is formed by depositing fleecy Au particles under a chamber pressure of several hundred Pa, patterning cannot be accomplished by an ordinary photoresist coating. Accordingly, Au-black layers have traditionally been fabricated by full-surface vapor deposition[10] or by selective vapor deposition using a shadow mask. The former technique is not a desirable approach because it results in degraded sensitivity because of the deposition of Au black even in the vicinity of the cold junctions where desired. Not only that, it also interferes with outside electrical contact. With the latter technique, the Au-black layer is formed under a chamber pressure of several hundred Pa with a vacuum deposition technique, resulting in a short mean free path for the deposited material. Because the material also penetrates around to the other side of the shadow mask, rapid formation of the interface is impossible. It is also difficult to align the shadow mask accurately. These factors have prevented the precise patterning of Au-black layers.

Several approaches have been taken in an effort to overcome these problems, including the use of NiCr[11] or another material[12] as the infrared absorbing layer in place of Au black or the use of a multiple reflection technique[9] to increase effective absorptivity. However, these approaches also have their problems. In the former case, substitute materials generally provide lower absorptivity than Au-black layers. One drawback of the latter approach is that increasing the level of absorptivity heightens the wavelength sensitivity. Consequently, developing a process for fabricating a more precisely patterned Au-black layer[13] is a key factor in improving the sensitivity of thermal infrared sensors.

Long narrow beams supporting the absorber are necessary to improve thermal isolation between hot and cold junctions. These beams tend to be influenced by the internal stress of the thin films of which they are composed. Moreover, to improve the fill factor, an asymmetric sensor layout pattern using curved beams is needed, making the beams more susceptible to the influence of internal stress. We adopted a Si^+ ion implantation technique to control the mechanical properties of the Si_3N_4 layer.

This paper first presents the structure of a thermoelectric infrared FPA that reconciles thermopile responsivity with the time constant. It then describes the fabrication process, which features control of the mechanical properties of the Si_3N_4 layer by an ion implantation technique and a precisely patterned Au-black layer fabricated by the lift-off technique. Finally it describes measured performance data of the thermoelectric infrared FPA.

2. Structure of the Device

Thermopile responsivity R and the time constant τ are given by

$$R = n \cdot \alpha \cdot R_{th} \cdot \eta \quad (1)$$

$$\tau \propto C_{th} \cdot R_{th}, \quad (2)$$

where n is the number of thermocouple pairs, α is the Seebeck coefficient, R_{th} is the thermal resistance between the hot and cold junctions, η is infrared radiation absorptivity and C_{th} is the thermal capacitance of the thermopiles.

Accordingly, to improve responsivity while holding down the resultant increase in the time constant, it is necessary to reduce the thermal capacitance without changing the thermal resistance.

Thermal resistance R_{th} is determined by the ratio of the length of the heat conduction path to the cross-sectional area of the thermopiles and membrane. The cross-sectional area of the thermopiles is determined by the pitch of the polysilicon of which they are composed and the thickness of the material composing the membrane. This means that it is necessary to reduce the pitch of the sensor and the thickness of the constituent materials to improve responsivity. These requirements can easily be met with the CMOS process.

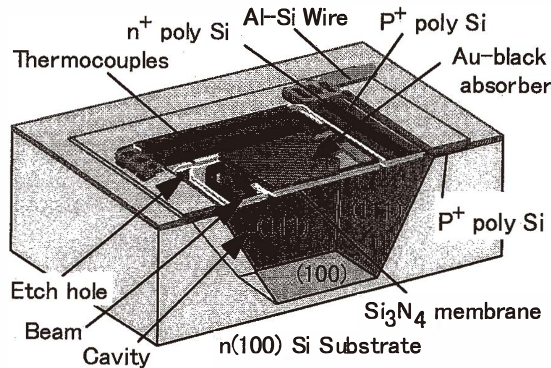

Fig. 1. Cross section of thermoelectric IR detector.

The cross-sectional structure of the prototype sensor is shown in Fig. 1, and a scanning electron microscope (SEM) micrograph of the sensor is shown in Fig. 2. The prototype sensor has six pairs of thermocouples consisting of alternating areas of p-type and n-type polysilicon connected in series on the Al–Si wiring layer. The p-type polysilicon was doped with a boron dose of 1×10^{16} cm^{-2}, and the n-type polysilicon was doped with a phosphorus dose of 1×10^{16} cm^{-2}. The Seebeck coefficient was 0.24 mV/K for the p-type polysilicon and 0.24 mV/K for the n-type polysilicon.

The sensing area was thermally isolated from the Si substrate and supported by four curved beams having a length of 119 μm. The layer structure of the membrane from bottom to top consisted of a Si_3N_4 layer, thermopiles, first isolation layer, first Al - Si wiring layer, second isolation layer, amorphous Si (a-Si) layer, and the Au-black layer. The hot junctions of each thermocouple were positioned near the edge of the IR absorber and the cold junctions were located on the Si substrate. The thickness of each layer is given in Table 1.

The dimensions of the device are as follows: the total area of the device is 190 μm$\times$190 μm, the Au-black absorber measures 116 μm$\times$116 μm, and the thermopiles have a length of 119 μm, a width of 0.8 μm, and a pitch of 3 μm. The internal resistance of the device is 116 kΩ.

3. Fabrication Process

The prototype array was produced in a fabrication process consisting of the ordinary CMOS process and special processes. The sequence of steps in the sensor fabrication process is shown in Fig. 3.

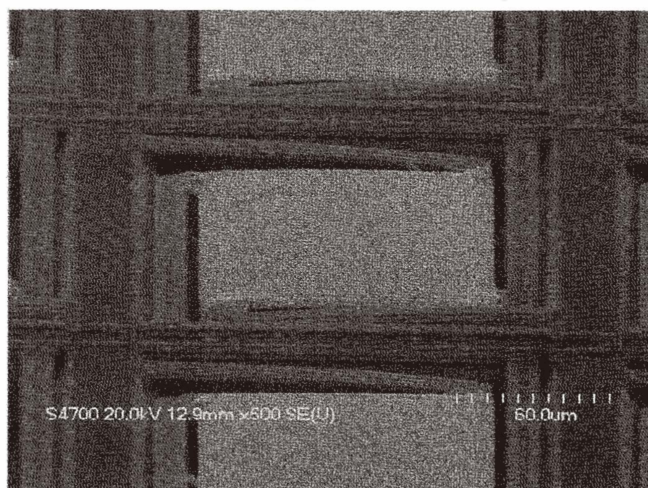

Fig. 2. SEM micrograph of a sensor.

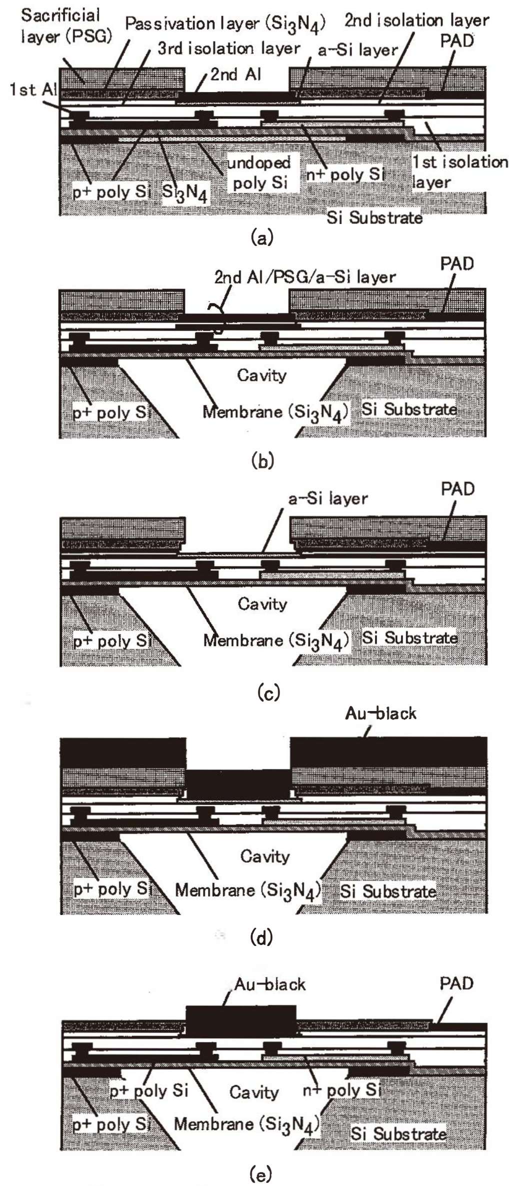

Fig. 3. Fabrication process ((a) PSG sacrificial layer formation, (b) Micromachining, (c) Removal of 2nd Al and PSG, (d) Au-black deposition, (e) Lift-off).

Table 1
Materials and thickness of each layer.

Layers	Materials	Thickness (nm)
Sacrificial layer	Poly Si	350
Membrane	SiN by LPCVD	100
Thermopiles	Poly Si	350
1st isolation layer	BPSG	600
1st wiring layer	Al-Si	700
2nd isolation layer	P-TEOS	600
Au-black underlay	Amorphous Si	100
3rd isolation layer	PSG	300
2nd wiring layer	Al-Si	800
Passivation layer	SiN by PECVD	300
Sacrificial layer	PSG	2000

3.1 *Control of residual stress of SiN layer*

Because the deposition temperature of the Si_3N_4 layer is 780°C and higher than that of any other layer making up the device, very large internal stress arises in this layer. Several techniques have been reported for reducing the internal stress of the Si_3N_4 layer, such as controlling the deposition conditions or using a phosphorus or boron ion implantation method[14,15]. However, there are no reports concerning internal stress changes with a silicon ion implantation method or as a function of insulation resistance of the Si_3N_4 layer. Therefore, we investigated the influence of a silicon ion implantation method, the later thermal treatment process and the insulation resistance.

Measurement was made of the warpage of the Si substrate following deposition of the Si_3N_4 layer on one side. The internal stress σ of the Si_3N_4 layer was calculated from the measured warpage using eqs. (3) and (4).

$$R_m = R_b \cdot R_a / (R_b - R_a) \tag{3}$$

$$\sigma = (E \cdot h^2)/[6(1-\nu) \cdot R_m \cdot t], \tag{4}$$

where R_a is the radius of the Si substrate before deposition, R_b is the radius of the Si substrate after deposition, E is Young's modulus, h is the substrate thickness, ν is Poisson's ratio, and t is the thickness of the deposited layer.

To reduce the residual stress level of the Si_3N_4 layer, we employed a Si^+ ion implantation technique. The measured results in Fig. 4 indicate that the Si_3N_4 layer without Si^+ ion implantation had very large residual stress of $\sigma = 1.54$ GPa after thermal treatment at 950°C for 30 min., but the Si_3N_4 layer implanted with a Si^+ ion dose of 1×10^{16} cm^{-2} and an ion energy of 150 keV had small residual stress of $\sigma = 0.55$ GPa after thermal treatment.

The electrical resistance of an ion-implanted Si_3N_4 layer was also measured. The results indicate that this ion implantation technique had no effect on the resistance of the layer. Therefore, taking these results into consideration, we fabricated a prototype sensor having a Si_3N_4 layer implanted with a Si^+ ion dose of 1×10^{16} cm^{-2}.

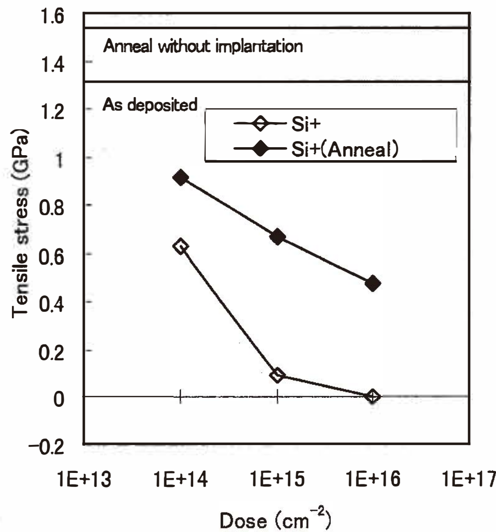

Fig. 4. Internal stress of SiN layer versus Si^+ ion dose.

3.2 *Micromachining*

To fabricate the membrane structure, it was necessary to under-etch the substrate below the membrane. This was accomplished using a sacrificial layer of polysilicon.(16) Hydrazine, which has good resistivity to SiO_2, was used to etch the p-type (100) Si substrate at an etchant temperature of 80°C for 90 min. Furthermore, to prevent a level difference from occurring in the polysilicon thermocouples and Si_3N_4 layer in the vicinity of the cold junctions, the polysilicon sacrificial layer below these junctions was doped with a high concentration of boron to inhibit the progress of etching. The layer was doped with a boron dose of 1×10^{16} cm^{-2} by ion implantation and annealed in a N_2 atmosphere at 950°C for 20 min., which worked to reduce the etching rate to 1/20 of the undoped rate. This process step is shown in Fig. 3(b)

3.3 *Deposition and lift-off of Au-black layer*

Vapor deposition was used to fabricate the Au-black layer. The requirements for the Au-black layer are not only good IR absorptivity, but also excellent patterning characteristics during the lift-off process.

The chamber was first evacuated to 1×10^{-2} Pa and then N_2 gas was introduced at the specified pressure. The evacuation system was then disconnected from the chamber and deposition was performed under those conditions. At a pressure of 5.30×10 Pa, gold luster was observed, but when the pressure was raised to 2.66×10^2 Pa, Au was deposited as fleecy particles. The Au-black layer showed high absorptivity of more than 90% when

illuminated by a light source having a wavelength of 10 μm. The Au-black layer deposited under these conditions exhibited an excellent peeling characteristic in the lift-off process.

Patterning of the IR absorber was accomplished in the lift-off process by utilizing a PSG sacrificial layer. As shown in Fig. 3(a), a PSG sacrificial layer is first formed following completion of the ordinary CMOS process. Only the area that becomes the IR absorber is removed in advance. This area is the exposed Al-Si wiring layer which is resistant to the hydrazine resist. Under these conditions, anisotropic etching is performed with hydrazine to fabricate the thermal isolation structure.

After the micromachining step, the second wiring layer and the PSG sacrificial layer, which prevents interaction between the second Al-Si wiring layer and the underlying amorphous Si (a-Si) layer, were removed as shown in Fig. 3(c). The sacrificial layers are removed with etchants of H_2SO_4:H_2O_2=1:1 at 80°C and NH_4F:CH_3COOH:H_2O=1:1:1 to expose the surface of the a-Si layer.

As shown in Fig. 3(d), the Au-black layer is then deposited under a pressure of 2.66×10^2 Pa.

Finally, as shown in Fig. 3(e), the PSG sacrificial layer is etched using an etchant of NH_4F: CH_3COOH: H_2O=1:1:1 to lift off the Au black from areas other than the IR absorber. This lift-off process is completed very quickly because the low density of the Au black allows the etchant to permeate this layer.

Strong adhesion to the underlying a-Si layer is obtained during Au-black deposition because Au diffuses to form an alloy. Diffusion of Au into the a-Si layer was measured by Auger electron spectroscopy (AES).[13] The results indicated that Au diffused to a depth of around 50 nm from the surface of the a-Si layer.

4. Characteristics of Thermopiles

The responsivity and time constant of the device were measured in a cryostat. The responsivity of the sensor was measured by illuminating it with infrared radiation emitted by a black body furnace at 500 K. The time constant was measured by illuminating the sensor with a He-Ne laser beam modulated by an optical chopper. The cryostat was evacuated to 7.33 Pa by a rotary pump. The sensor output signal was first amplified 100 times and then introduced into an oscilloscope to obtain a waveform for evaluating the time constant.

The measured results shown in Fig. 5 indicate that the responsivity R rose to 2100 V/W as a result of reducing the pressure of the cryostat because the thermal conductance via air decreased with the pressure. The time constant τ increased to 25 ms at the same pressure. These values indicate that the sensor provides good performance equal to that of a thermopile. Moreover, the fact that the internal electrical resistance of the sensor was 116 kΩ resulted in low thermal noise and a high S/N ratio. The measured time constant is sufficient for taking moving pictures at the standard NTSC frame rate of thirty frames per second.

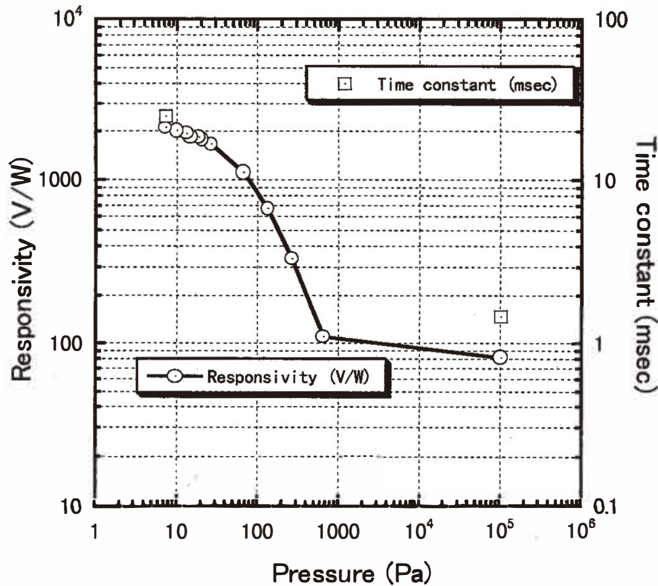

Fig. 5. Measured responsivity and time constant vs pressure.

5. 48×32 Element Focal Plane Array

5.1 *FPA design*

A micrograph of a fabricated 48×32 element IR FPA is shown in Fig. 6. The overall chip size is 10.5 mm×7.44 mm with a 9.12 mm×6.08 mm imaging area. Each detector consists of six pairs of p-n polysilicon thermocouples and two readout NMOS transistors. The external dimensions of each detector are 190 μm×190 μm.

A block diagram of the 48×32 element IR FPA and an equivalent circuit of one pixel are shown in Fig. 7. A low scanning frequency is necessary to reduce thermal noise from thermopiles and the latter-stage amplifier circuit. For that reason, the imaging area was divided into twelve blocks and the chip has a twelve channel parallel output. One block consists of 4×32 elements.

5.2 *Package*

Figure 8 shows the vacuum package containing the 48×32 element IR FPA. The package size is 44 mm in diameter and about 20 mm in height. The window is made of germanium, having an anti reflection coating for the 10 μm wavelength.

5.3 *Performance*

An IR camera was fabricated to evaluate the device. This camera did not use a chopper or an operating temperature stabilizer. It incorporated a digital offset correction circuit

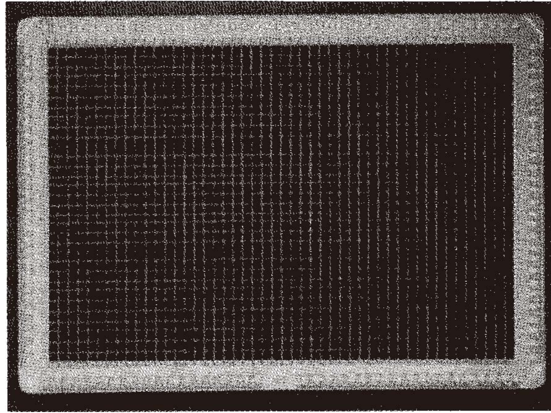

Fig. 6. Micrograph of a 48×32 element infrared focal plane array (10.5 mm×7.44 mm).

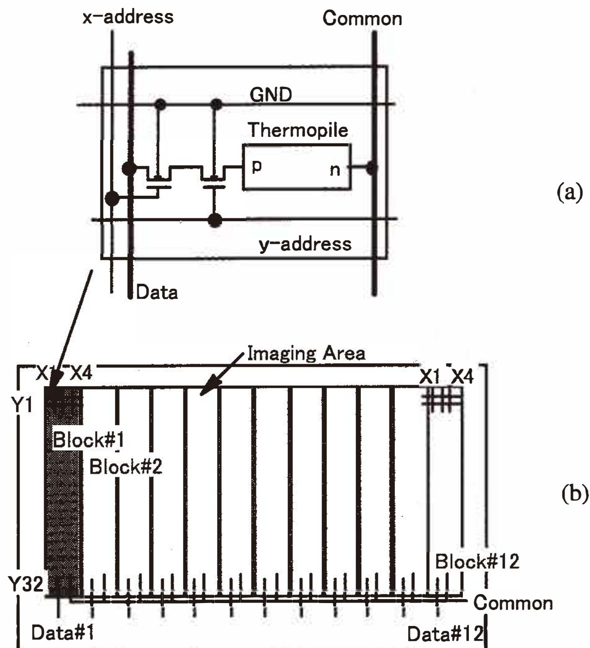

Fig. 7. Diagram of a 48×32 element infrared focal plane array ((a) equivalent circuit of one element, (b) chip diagram).

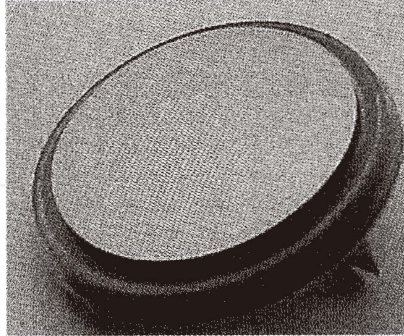

Fig. 8. Vacuum package of a 48×32 element infrared focal plane array (44 mm in diameter).

and both an RS-232C port and an NTSC interface circuit. The camera had a f/0.7 germanium lens with a horizontal field of view of approximately 30°. The lens had an anti reflection coating for the 10 μm wavelength. The responsivity of the chip was measured by illuminating it with infrared radiation emitted by a black body furnace at 500 K.

Figure 9 shows an example of the reproduced IR image, where the hot area is shown in white. The output offset was corrected by the digital offset correction circuit, but no gain correction was made.

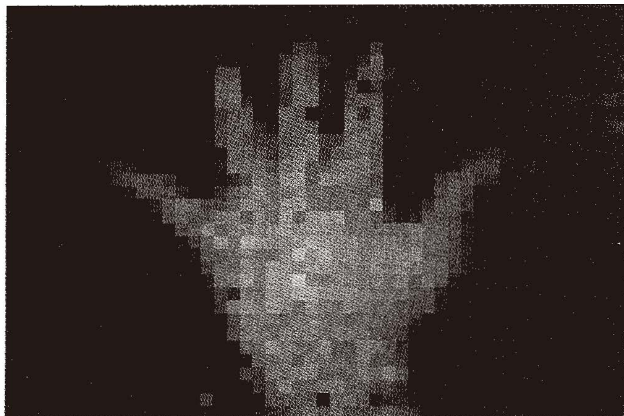

Fig. 9. An infrared image of a hand taken by a 48×32 element infrared focal plane array.

6. Summary

This paper has presented a 48×32 element thermoelectric infrared focal plane array that provides high responsivity and potential for low cost. The device has the high responsivity of 2100 V/W and an excellent time constant of 25 ms. Each detector consists of six pairs of p-n polysilicon thermocouples, and has a small internal electrical resistance of 116 kΩ. The processes for obtaining a precisely patterned Au-black infrared absorbing layer and reducing the thermal stress of the Si_3N_4 layer by the silicon ion implantation method were described. A thermal image of a human hand has been obtained with the device. The performance of the device is suitable for automotive applications.

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