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Bipolar Switching Properties and Electrical Conduction Mechanism of Silicon Carbide Thin-film Resistive Random-access Memory Devices

Kai-Huang Chen,[1,2*] Ming-Cheng Kao,[3**] Yao-Chin Wang,[1]
Hsin-Chin Chen,[1] and Chin-Chueh Huang Kao[1]

[1]Department of Electronic Engineering, Cheng Shiu University, Kaohsiung 83347, Taiwan
[2]Section of Mathematics and Physics Science, Center for General Education,
Air Force Academy, Kaohsiung 82047, Taiwan.
[3]Graduate Institute of Aeronautics, Department of Information and Communication Engineering,
Chaoyang University of Technology, Taichung 413310, Taiwan

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In this work, as-deposited silicon carbide (SiC) thin films, belonging to the class of third-generation semiconductor materials, were prepared on TiN/Si substrates by rf magnetron sputtering for application in resistive random-access memory (RRAM) devices. The SiC films were sputtered under rf powers of 50/75 W at various deposition times, while aluminum (Al) was subsequently deposited via thermal evaporation to form the metal–insulator–metal structure. Effects of rapid thermal annealing (RTA) at 300 °C on the electrical characteristics of the thin-film RRAM devices were investigated using a semiconductor parameter analyzer. The current–voltage (*I–V*) characteristics of the as-deposited and annealed films revealed a clear dependence on sputtering power and annealing conditions. As the deposition power increased, both the *I–V* curve slope and the memory window showed slight enhancement, accompanied by a high set/reset voltage. Specifically, the 50 W parameter exhibited a switching voltage of approximately 0.5 V, while that at 75 W showed 0.75 V. After annealing at 300 °C, the SiC thin films demonstrated a significant improvement in resistive switching behavior, with a memory window of 10^5 and set and reset voltages increasing to 3 V. These enhancements are attributed to reoxidation and recrystallization processes occurring during RTA, which promote defect redistribution and improved filament formation within the SiC layer, thereby enhancing switching stability and device endurance.

1. Introduction

The rapid advancement of modern technology has made 3C products, namely, computers, communication, and consumer electronics, an indispensable part of daily life. As manufacturing technologies continue to evolve, next-generation electronic devices are increasingly expected to

*Corresponding author: e-mail: 5977@gcloud.csu.edu.tw
**Corresponding author: e-mail: kmc@cyut.edu.tw
https://doi.org/10.18494/SAM5722

be portable, high-performance, and durable. Among the essential technologies enabling these advancements, memory capacity, processing speed, and system integration play pivotal roles in determining overall device performance. Various devices are generally categorized into different volatile types. Static random-access memory and dynamic random-access memory require continuous energy supply and lose stored information once power is removed. Although they offer high-speed operation and low power consumption, their inability to maintain data without power limits their applicability in long-term data storage.

In contrast, nonvolatile memory (NVM) retains data even in the absence of power and allows data retrieval after power restoration. Flash memory has long dominated the NVM market owing to its reliable data retention; however, it now faces fundamental scaling and endurance limitations. To address these challenges, research has shifted toward next-generation NVM technologies, including the ferroelectric RAM (FeRAM), magneto-resistive RAM (MRAM), phase-change memory (PCM), and resistive random-access memory (RRAM). Among these candidates, RRAM stands out owing to its simple metal–insulator–metal (MIM) architecture, high switching speed, low set/reset voltage, low power loss, and good scalability. The resistance states of RRAM, high-resistance state (HRS) and low-resistance state (LRS), correspond to binary data "0" and "1," respectively, enabling high-speed data access in the nanosecond range. Furthermore, RRAM devices operate under low-current conditions (μA–nA) and demonstrate excellent endurance and retention characteristics, making them strong candidates for future NVM applications.[1–5]

As the era of big data and IoT advances, memory technologies must accommodate vast data storage and high-speed processing demands. The limitations of volatile memory have further highlighted the importance of developing high-performance nonvolatile memories, particularly RRAM, which combines low cost, low operating power, and process compatibility with transistor technologies. Typically, RRAM devices are fabricated using physical vapor deposition (PVD) and chemical vapor deposition (CVD) methods to construct a MIM structure, employing metal oxides or wide-bandgap (third-generation) semiconductor materials as the switching layer.[6–10]

Third-generation semiconductor materials, such as GaN, SiC, and AlN, exhibit exceptional properties for wide bandgap energy, high breakdown electric field, and excellent thermal conductivity. These features enable high-power, high-frequency, and high-temperature operation while maintaining excellent energy efficiency. Consequently, they are ideal for next-generation power electronics, rf communication, and high-performance computing applications. In this paper, we report the bipolar switching characteristics and electrical transfer mechanism of silicon carbide (SiC) thin-film RRAM devices fabricated on TiN substrates, forming a MIM structure with aluminum as the top electrode through thermal evaporation.

2. Experimental Details

In this study, titanium nitride was employed as the bottom electrode for the RRAM device structure. A SiC thin film was subsequently prepared on the TiN substrate using an rf magnetron sputtering system equipped with both DC (240 W) and rf (1 kW) power supplies. The SiC layer

served as the active insulating layer within the RRAM structure. Finally, aluminum (Al) was deposited as the top electrode by a thermal evaporation method using a metal shadow mask, forming a MIM structure, as illustrated in Fig. 1.

Prior to film deposition, the TiN substrates were sectioned using a diamond cutter and sequentially cleaned for 10 min. The SiC films were sputtered at rf powers of 50 and 75 W, with deposition durations of 30, 60, and 120 min. Post-deposition, the SiC films were subjected to post-thermal treatment at 300, 400, and 500 °C to investigate the effects of annealing on the films' microstructural and electrical characteristics, particularly their bipolar switching behavior and conduction mechanisms.

The surface morphology of the SiC thin films was analyzed by field-emission scanning electron microscopy (FE-SEM; Philips Tecnai G2 F20 FEG-STEM), whereas the crystallographic structure was examined by X-ray diffraction (XRD; Bruker D2 Phaser). The current–voltage (*I–V*) characteristics of the SiC-based RRAM devices were evaluated using an Agilent B1500 semiconductor parameter analyzer. A precision power measurement system was employed to confirm resistive switching behavior and to assess the effects of sputtering power, deposition time, and annealing temperature on the overall electrical performance of the SiC thin-film RRAM devices.

3. Results and Discussion

The SiC thin films were prepared using an rf sputtering method under various deposition powers and durations. After fabrication, the RRAM devices were subjected to detailed physical and electrical characterization. The SiC thin films were deposited at rf powers of 50 and 75 W, with deposition times of 30, 60, and 120 min for each power level. The experimental parameter conditions are summarized in Table 1. Following the initial forming process, the SiC-based RRAM devices exhibited electrical conductivity, confirming the formation of conduction filaments of the SiC films. Additionally, negative bias was applied, rupturing the conduction filament and switching the device from LRS to HRS. Thereafter, bipolar voltage sweeps were repeatedly applied in both positive and negative directions to evaluate the resistive switching behavior and determine the memory window of the RRAM devices.

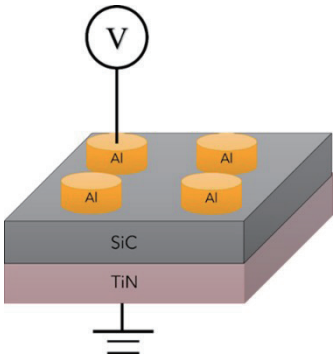

Fig. 1. (Color online) MIM structure of SiC thin-film RRAM device.

Table. 1
Parameter conditions of as-deposited thin-film RRAM devices.

rf power (W)	50, 75
Pressure (mTorr)	10
Temperature (℃)	25
Process time (min)	30, 60, 120

Figure 2 shows the *I–V* characteristics of SiC thin films deposited at the rf sputtering power of 50 W under different deposition times. All samples exhibited bipolar resistive switching properties, confirming stable reversible switching between HRS and LRS. A distinct memory window was observed, with an on/off resistance ratio of 1 and an operating voltage of 1.5 V. These results suggest that the resistive switching behavior of SiC films remains consistent across various deposition durations, demonstrating reliable switching capability under the tested conditions.

Figure 3 shows the *I–V* characteristics of SiC deposited at an rf power of 75 W with various deposition times. Similar to the 50 W samples, all devices exhibited bipolar resistive switching properties, demonstrating stable transitions between HRS and LRS. A distinct memory window was observed, with an on/off of 1 and an operating voltage of 1.5 V. Figure 3 shows that the variations in sputtering power and deposition duration produced no significant difference in resistive switching performance, indicating that film uniformity and stoichiometry were maintained under these deposition conditions.

To further investigate the charge transport mechanism and the formation of conduction filaments in the initial switching process, the *I–V* characteristics were analyzed through curve fitting using the Ohmic conduction and hopping conduction models. The experimental data were fitted to the corresponding theoretical equations by transforming the *I–V* relationship into ln *I*–$V^{1/2}$ and ln *I*–ln *V* plots, respectively. The fitting analysis provides insight into the dominant carrier transport pathways and the role of localized defect states within the SiC switching layer during the resistive switching process.

$$J = qunE \exp\left[\frac{-\left(\Delta E_{ac}\right)}{kT}\right] \tag{1}$$

Here, E_{ac} is the electron activation energy, q is the electron charge, E is the applied electrical field, n is the electronic concentration, k is the Boltzmann constant, T is the absolute temperature, and u is the carrier mobility. In addition, to calculate the $\ln\left(\frac{I}{T^2}\right)-\sqrt{V}$ curve, the hopping conduction mechanism equation was transformed to the *I–V* curves fitting the RRAM devices. For the hopping conduction,

$$J = qN_a v_o e^{-q\Phi_T/kT} e^{qaV/2dkT}, \tag{2}$$

where d, Φ_T, v_0, N, and a are the film thickness, the barrier height of hopping, the intrinsic vibration frequency, the density of space charge, and the mean hopping distance, respectively.[11–13]

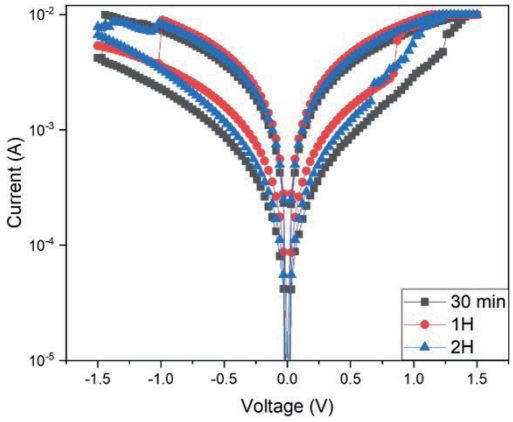

Fig. 2. (Color online) *I–V* curve of SiC thin films prepared using rf power of 50 W for different deposition times.

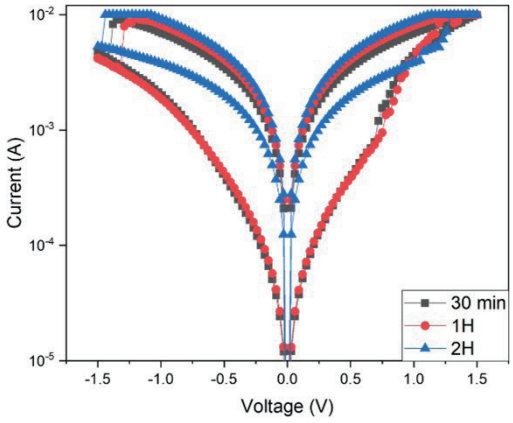

Fig. 3. (Color online) *I–V* curve of SiC thin films prepared using rf power of 75 W for different deposition times.

During the fabrication of the SiC-based RRAM devices, lattice imperfections within the thin film introduced intrinsic defect states near the edges of the conduction and valence bands. These defect states act as localized energy levels that significantly affect charge transport within the switching layer. Under an applied electric field, charge carriers can be captured by these defect sites, leading to trap-assisted hopping conduction. Once captured, carriers can gain sufficient energy—either through the applied electric field or thermal excitation—to overcome the potential barrier height and transfer to the conduction/valence band, thereby contributing to the overall current flow.

The Poole–Frenkel (P–F) conduction mechanism shares similarities with Schottky emission, as both involve the field-enhanced thermal excitation of trapped electrons. However, the P–F effect specifically arises from carrier emission from bulk trap states within the dielectric, rather

than at the metal–insulator interface. In this model, the energy barrier height corresponds to the depth of the defect potential well, which governs the probability of carrier release. The P–F conduction mechanism can be mathematically expressed as

$$J \propto E \exp[(-q(\Phi_B - \sqrt{((qE_i)/(\pi\varepsilon_i))})/kT], \tag{3}$$

where Φ_B represents the defect energy barrier height, E_i is the electron field, E is the applied electrical field, k is the Boltzmann constant, T is the absolute temperature, and ε_i is the dielectric constant.

Figure 4 shows the *I–V* curves of the RRAM devices using the as-deposited SiC films prepared with the rf power of 75 W. By linear fitting (fitting curve), it was determined that the HRS from 0 to 0.5 V adheres to P–F conduction, whereas the LRS predominantly followed Ohmic conduction.

Figure 5 shows the *I–V* curves of the RRAM devices using the 400 ℃-annealed SiC films prepared with the rf power of 75 W. Figure 5 also shows that at 400 °C, both HRS and LRS adhere to the Schottky emission mechanism. This result suggests that a potential barrier must be overcome to generate current during resistance switching. To define the memory window, the on/off ratio was calculated from the HRS/LRS in set/reset voltage. The on/off ratio was 6, the operating voltage was around 3 V, and the leakage current was about 10^{-7} A for HRS.

Figure 6 shows the *I–V* curves of the RRAM devices using the 500 ℃-annealed SiC films prepared with the rf power of 75 W. Figure 6 demonstrates that at an annealing temperature of 500 °C, HRS transitions from Schottky emission to hopping conduction. This change was likely due to an increase in the number of shallow defects caused by the elevated temperature. On the other hand, LRS continues to follow the Schottky emission mechanism. The on/off ratio was about 5, the operating voltage was around 3 V, and the leakage current was about 10^{-6} A for HRS.

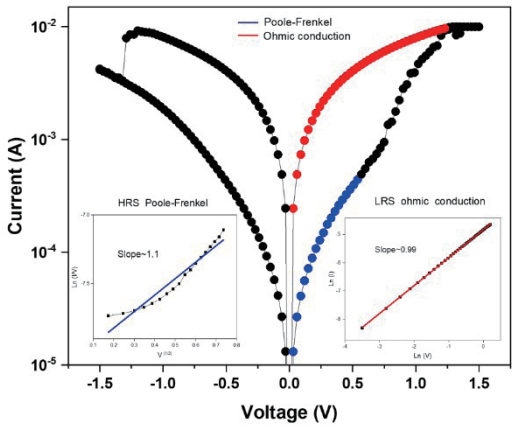

Fig. 4. (Color online) *I–V* curves of RRAM devices using as-deposited SiC films prepared with rf power of 75 W.

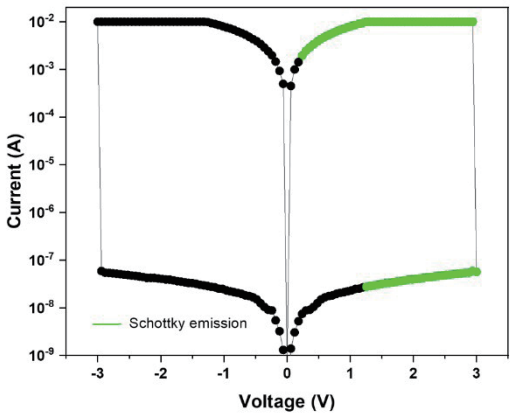

Fig. 5. (Color online) *I–V* curves of RRAM devices using the 400 °C-annealed SiC films prepared with rf power of 75 W.

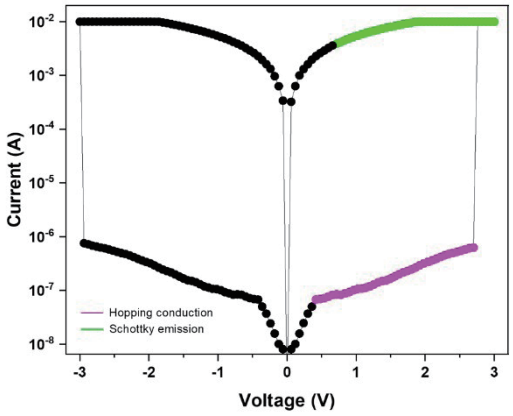

Fig. 6. (Color online) *I–V* curves of RRAM devices using the 500 °C-annealed SiC films prepared with rf power of 75 W.

Figure 7 shows the comparison of the *I–V* curves of RRAM devices using SiC films with different annealing treatments and prepared with the rf power of 75 W. The applied compliance currents are about 10 mA. The set and reset voltages of the RRAM device for nontreated films are less than −1 and 1 V, respectively. For films annealed at 400 and 500 °C, the memory windows exhibit 10^5 ratio for LRS/HRS and a stable set voltage. However, the nontreated RTA film RRAM devices exhibited low memory windows. This result may suggest the stable set voltage induced by the compliance current of 10 mA.

Figure 8 shows the 100 times *I–V* curves of the RRAM devices using the 500 °C-RTA-treated SiC films prepared with the rf power of 75 W. As shown in Fig. 8, the *I–V* curves of the SiC RRAM devices also exhibit stable bipolar switching properties for applications in nonvolatile memory devices.

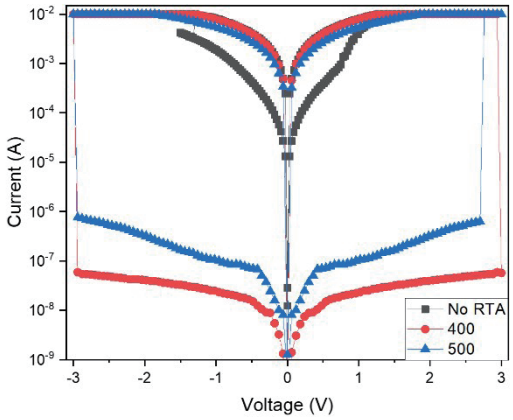

Fig. 7. (Color online) Comparison of *I–V* curves of RRAM devices using SiC films with different annealing treatments and prepared with rf power of 75 W. ("No RTA" denotes non-RTA treatment.)

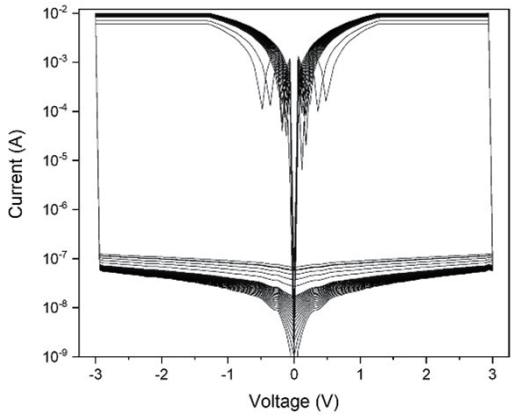

Fig. 8. (Color online) 100 times *I–V* curves of RRAM devices using 500 °C-RTA-treated SiC films prepared with rf power of 75 W.

Figure 9 shows the relationship between the switching cycles and resistance states of SiC thin-film RRAM devices, evaluated through retention and endurance measurements. This analysis was conducted to assess the long-term data stability and reliability of the devices for nonvolatile memory applications. As shown in the figure, the resistance values of both HRS and LRS remained stable over extended testing durations. The extrapolated data revealed that the on/off resistance ratio exhibited negligible degradation for over 10^3 s, confirming excellent retention performance and stable switching behavior during prolonged operation.

Figure 10 shows resistance evolution as a function of the number of switching cycles for RRAM devices fabricated using SiC films deposited at an rf power of 75 W and subjected to

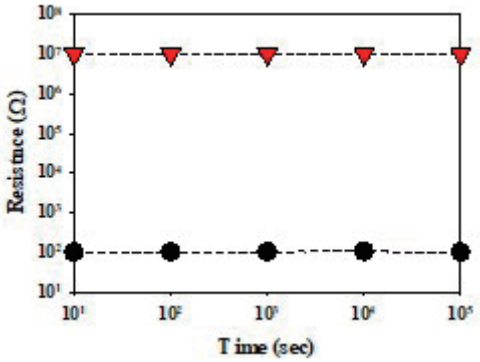

Fig. 9. (Color online) Resistance versus switching cycle curves of 500 °C-RTA-treated SiC thin-film RRAM devices.

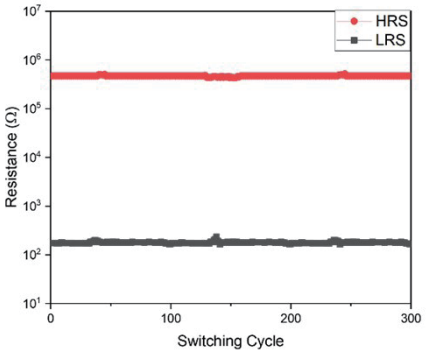

Fig. 10. (Color online) Resistance versus time curves of SiC thin-film RRAM devices.

various annealing treatments. The results indicate that the resistive switching characteristics were highly reproducible across repeated cycles. Furthermore, the on/off resistance ratio remained consistent for more than 10^2 cycles, as determined by extrapolation analysis, suggesting that post-deposition annealing effectively improved film uniformity, defect stability, and electrical endurance.

Figure 11(a) shows the distribution and accumulation of oxygen vacancies at the interface between the $SiCO_x$ layer and the SiC switching film in the RRAM structure. During the transition to LRS, these oxygen vacancies progressively accumulate and contribute to the formation and stabilization of the conductive filament. Figure 11(b) presents the physical conduction model, showing the continued oxidation–reduction dynamics along the metallic filament under high positive bias, which plays a crucial role in modulating the device resistive switching behavior.

The corresponding charge-transport model and the initial filament formation/rupture pathways for the set/reset states are summarized in Fig. 11. Consistent with previous studies, the

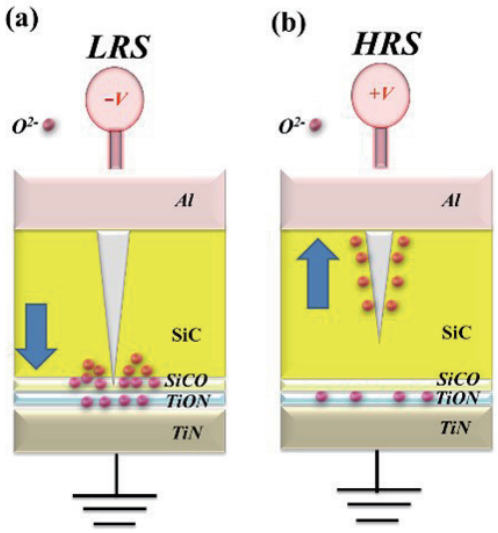

Fig. 11. (Color online) Electrical initial metallic filament path model of SiC thin-film RRAM devices for (a) set and (b) reset states.

electrical conduction mechanisms of RRAM devices exhibit a combination of P–F emission and Ohmic conduction in both HRS and LRS, reflecting the defect-assisted transport and field-enhanced carrier emission inherent to oxygen-vacancy-mediated switching systems.

5. Conclusions

In this work, we investigated the electrical characteristics and resistive switching behavior of third-generation semiconductor-material-based SiC thin films deposited on TiN substrates. The SiC films were fabricated using an rf power of 75 W with deposition durations of 30, 60, and 120 min. In addition to the as-deposited samples, the SiC films subjected to RTA were also evaluated to examine the effects of post-deposition treatment on switching performance. The Al top electrodes were deposited via electron-beam thermal evaporation to form a conventional MIM RRAM structure. Electrical measurements and resistive switching analyses were carried out using a precision semiconductor parameter and power measurement system.

The experimental results showed that the as-deposited SiC thin film with a deposition time of 60 min exhibited the most favorable switching behavior. The device demonstrated an on/off resistance ratio of 1, an operating voltage of 1.5 V, a leakage current of 10^{-4} A, and an endurance of 10^2 switching cycles. Conduction mechanism analysis revealed that charge transport in HRS followed the P–F emission model, whereas LRS was dominated by Ohmic conduction, consistent with defect-assisted transport in SiC-based RRAM.

Following RTA processing, the SiC films exhibited significantly improved resistive switching characteristics. For the samples subjected to moderate RTA, the on/off ratio increased to 6, the operating voltage rose to 3 V, the leakage current was 10^{-8} A, and the endurance improved to approximately 300 cycles. For the samples annealed at 500 °C, the device maintained an on/off

ratio of 3, an operating voltage of 3 V, a leakage current of 10^{-6} A, and an endurance approaching 10^3 switching cycles. These enhancements are attributed to the thermally induced defect redistribution, improved crystallinity, and reduced trap-state density within the SiC switching layer. Finally, third-generation semiconductor material SiC thin-film RRAM devices will be ideal for next-generation memory electronic devices.

Acknowledgments

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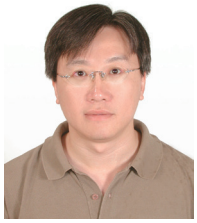
About the Authors

Kai-Huang Chen received his B.S. and M.S. degrees from the Department of Electronics Engineering, National Yunlin University of Science and Technology, Taiwan, in 1998 and 2000, respectively. He received his Ph.D. degree in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2007. He served at the Department of Electronics Engineering, Cheng Shiu University, Kaohsiung, Taiwan, from 2020 to 2025. His current research interests include the fabrication of functional thin films, the design of memory devices, and various functional materials for ferroelectric RAM and resistive random access memory devices.
(5977@gcloud.csu.edu.tw)

Ming-Cheng Kao received his M.S. and Ph.D. degrees in electrical engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2000 and 2004, respectively. He is currently a full professor in the Graduate Institute of Aeronautics, Department of Information and Communication Engineering, Chaoyang University of Technology, Taichung, Taichung City, Taiwan. His current research interests are in the areas of ferroelectric materials and dye-sensitized solar cells. (kmc@cyut.edu.tw)



Yao-Chin Wang received his Ph.D. degree from National Chiao Tung University, Taiwan, in 2014. Since 2022, he has been serving as an associate professor at Cheng Shiu University. His research interests include semiconductor engineering and photonic systems. (y.c.wang@ieee.org)

Hsin-Chin Chen received his Ph.D. degree from National Cheng Kung University, Taiwan, in 2016. Since 2022, he has been serving as an assistant professor at Cheng Shiu University. His research interests include semiconductor packaging, artificial intelligence, and IoT technology. (0662@glcloud.csu.edu.tw)

Chin-Chueh Huang Kao received his B.S. and M.S. degrees from the Department of Electronics Engineering, Cheng Shiu University, Kaohsiung, Taiwan, in 2022 and 2024, respectively. His current research interests include the fabrication of memory devices and various functional materials for resistive random access memory devices. (m1003101@gcloud.csu.edu.tw)