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Novel Design of Low-power Double Node Upset Tolerant Latch Cell

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To enhance the reliability of sensor interfaces and signal-processing circuits operating in radiation environments, a novel low-power double node upset (DNU)-tolerant latch, termed the low-power double-node upset tolerant (LDUT) latch, is proposed and implemented in this work. The design employs a redundant architecture based on C-elements (CE) and a self-recovery cell (SRC) module, achieving full DNU self-recovery capability through a clock-controlled feedback loop that enhances circuit robustness for sensor-related electronic systems. Simulation results under the Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm CMOS technology demonstrate that the LDUT latch significantly outperforms existing designs in key performance metrics. Dynamic power consumption is reduced to 0.77 μW, representing an improvement of 25.08% compared with the high-performance, low-cost, and DNU-tolerant latch (HLDTL) and 87.3% compared with the DNU-resilient latch (DNURL) design. Further process-voltage–temperature (PVT) analysis shows that the LDUT latch also provides low sensitivity to temperature variations, making it suitable for radiation-hardened sensor applications and high-reliability integrated circuits.

1. Introduction

Integrated circuits (ICs) have become increasingly vulnerable to single-event effects (SEEs) with the continuous scaling of semiconductor processes,[(1)] such as the single-event upset (SEU) and single-event transient (SET) in deep submicron technologies.[(2)] In particular, these effects threaten the reliability of sensing systems and mixed-signal interfaces deployed in aerospace and nuclear environments, where latch circuits are essential for reliable signal sampling and data retention. Traditional single-node upset (SNU) hardening techniques, such as dual interlocked storage cell (DICE), are insufficient for modern nanoscale technologies where multinode upsets (MNUs) occur owing to internode charge sharing.[(3,4)] High-energy particle strikes may induce simultaneous flips in adjacent nodes, termed double node upset (DNU), further exacerbating soft error rates.[(5)]

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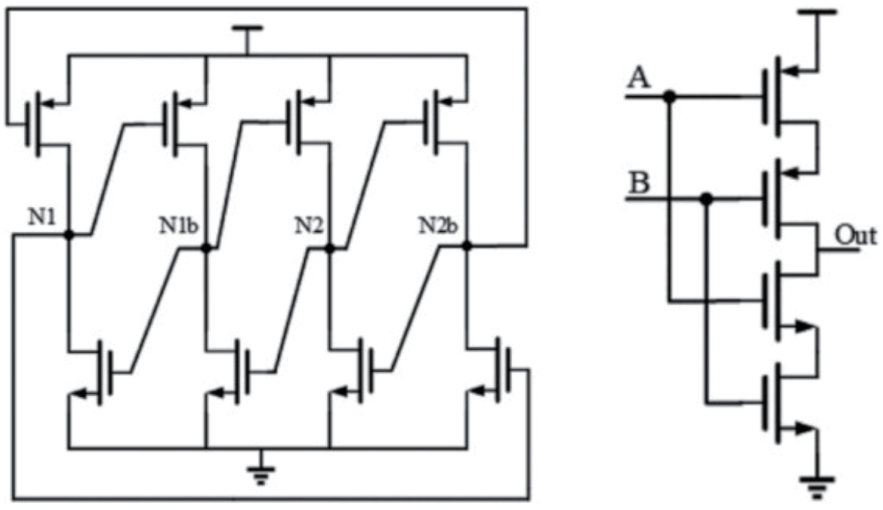
Recent research in the field of radiation-hardened by design (RHBD) focuses on circuit-level redundancy to maintain signal integrity in sensing and control electronics. These methods utilize structures such as Muller C-elements (MCE), DICE variants, and Schmitt triggers (STs).[6,7] However, these approaches still meet several limitations: MCE risks output floating states; DICE extensions suffer from long feedback activation times and high power consumption; and STs lack sufficient robustness when processes are scaled into deep-submicron nodes. Moreover, existing designs often suffer from excessive areas, power, and delay. To address these challenges, we propose a low-power DNU-tolerant (LDUT) latch cell design, combining clock-controlled C-elements and redundancy to enable self-recovery while minimizing sensitive nodes. Simulations under the 65 nm Taiwan Semiconductor Manufacturing Company (TSMC) technology confirm its superior radiation tolerance and low cost, making it suitable for high-reliability applications.

The rest of this paper is organized as follows: In Sect. 2, we review previous DNU-tolerant latches. In Sect. 3, we detail the LDUT circuit topology and its hardening mechanisms. In Sect. 4, we validate the performance via simulations. In Sect. 5, the work is summarized.

2. Previous DNU-tolerant Latch Designs

In this section, self-recovering DNU and DNU-tolerant latches are described. Most existing hardened latches utilize DICE and the C-element (CE) cell, both of which exhibit excellent SNU tolerance capabilities. The circuit topologies of these two units are illustrated in Fig. 1. Figure 1(a) shows the DICE circuit, which employs a dual-interlocked structure to effectively eliminate SNUs. Additionally, the symmetric design of the circuit balances metrics such as delay, power consumption, and area. Figure 1(b) presents a two-input CE cell circuit. In this section, we will introduce previously published typical DNU-hardened latches, as shown in Figs. 2 to 6.



(a) (b)

Fig. 1. Equivalent schematics of (a) DICE. Nodes N1 and N2 own the opposite data to those in N1b and N2b. (b) CE cell. A and B are the input signals; output signal Out depends on the level of A and B.

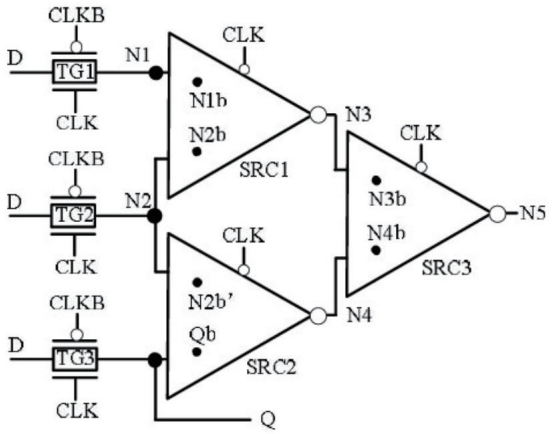


Fig. 2. Equivalent schematic of DNURL. Input data D transfers through TG controlled under clock signals CLK and CLKB into threes MCEs: SRC1–SRC3. Nodes N1, N2, N3, N4, and N5 store the corresponding data to N1b, N2b, N2b', Qb, N3b, and N4b.

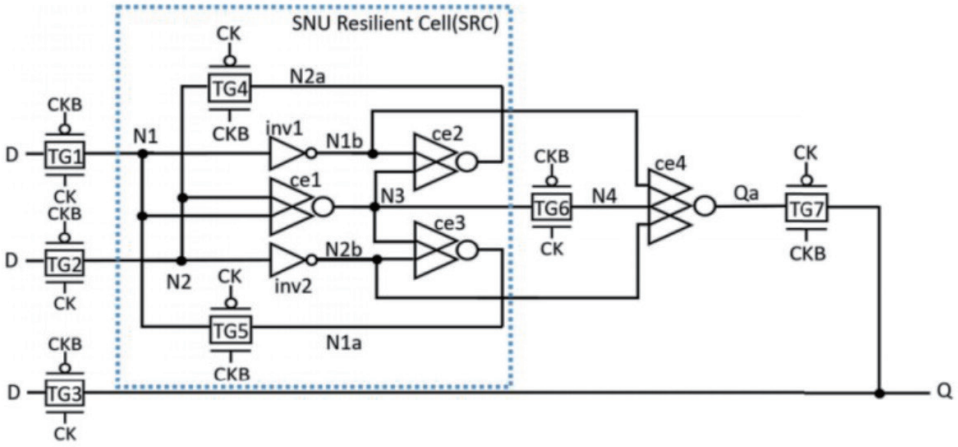


Fig. 3. (Color online) Equivalent schematic of HLDTL. Clock signals CK and CKB control input data D and node data N1–N4 through transfer gates TG1–TG7. Q is the final output data.

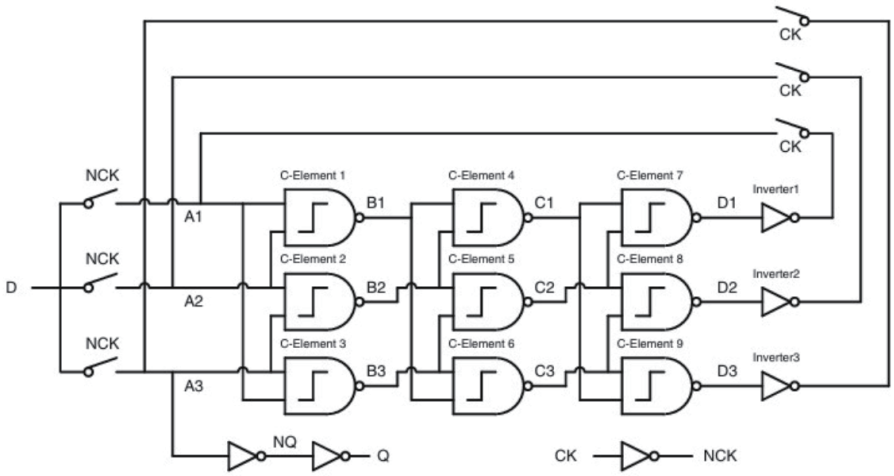


Fig. 4. Equivalent schematic of NTHLTCH. Input data D transfers to CE arrays controlled by clocks CK and NCK. Q and NQ are the output data.

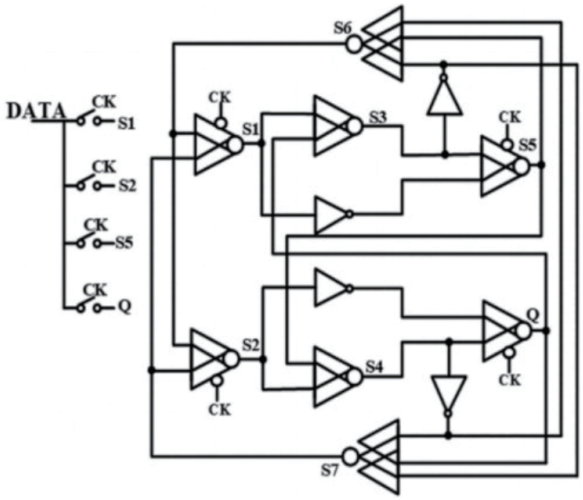


Fig. 5. Schematic of DNUSH latch. Input DATA transfers through the CK switch, S1–S7 are the stored data. Q is the final output.

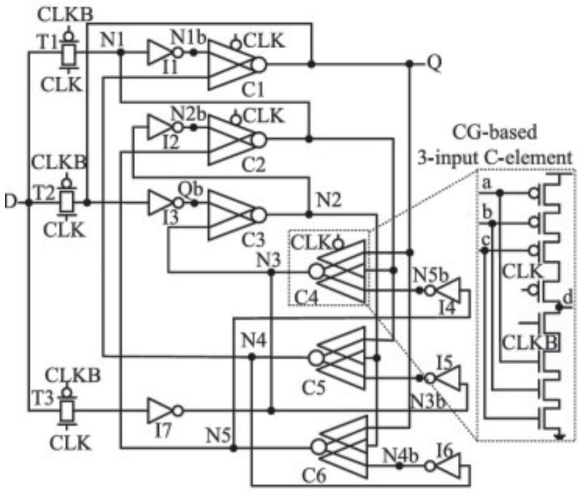


Fig. 6. Schematic of HRCE latch. Input data D transfers into a three-layer cyclic feedback structure under the control of clocks CK and CLKB through T1–T3. N1–N5 store the temporary data, I1–I7 are inverters, and C1–C6 are 3-input CEs.

2.1 DNURL

Figure 2 illustrates the structure of the DNURL, which comprises three interlocked single-node antishift units. Each unit primarily consists of three interconnected Muller CEs with mutual feedback.[8,9] However, the latch uses a large number of transistors, resulting in significant area cost, high power consumption, and poor overall performance.

2.2 High-performance, low-cost and DNU-tolerant latch (HLDTL)

Figure 3 shows the structure of the HLDTL.[10] This latch consists of an SRC module and an auxiliary module. Additional transmission gates added to the feedback loop significantly reduce propagation delay. Furthermore, the integration of extensive clock-controlled structures in the circuit substantially lowers the overall power consumption of the design.

2.3 Non-temporally hardened latch (NTHLTCH)

As shown in Fig. 4, the NTHLTCH features a three-stage cascaded feedback array composed of nine CEs and three inverters.[11] However, the extensive use of CEs leads to significant drawbacks, including excessive area, high power consumption, and increased internal latency. However, this scheme is not cost-effective since the design consists of numerous MCEs to ensure correct data retention.

2.4 DNU Self-healing (DNUSH) latch

As shown in Fig. 5, the DNUSH latch structure includes four clock-controlled CEs, two standard CEs, two three-input CEs, four inverters, and four transmission gates.[12] Because of the large number of CEs, the latch exhibits relatively high power consumption and a large area.

2.5 Highly robust and cost-effective (HRCE) latch

As shown in Fig. 6, the HRCE latch adopts a three-layer cyclic feedback structure.[13] However, the excessive number of CEs and inverters results in higher power and area costs. Although the inclusion of high-speed paths effectively reduces latch delay, the overall performance of the HRCE latch remains moderate.

3. Circuit Structure of Proposed LDUT Latch

3.1 Circuit structure and operational mechanism of LDUT latch

The proposed latch is based on CEs, ensuring SNU self-recovery capability, as shown in Fig. 7. Figure 8 illustrates its layout. The latch consists of four transmission gates, an SRC module, a standard CE, and a clock-controlled CE. The DNU tolerance of the latch is primarily achieved through the SRC module and CEs. The SRC structure eliminates SNU via its feedback loop, achieving full SNU immunity. Through integration with the clock-controlled CEs, the latch further realizes DNU tolerance.

In the latch circuit, the input is labeled DATA, the output is Q, CK is the system clock, and NCK is the inverted system clock. When CK is at a high logic level and NCK is at a low one, the latch operates in the transparent mode: DATA propagates through the transmission gates to precharge internal nodes and is output to Q via the final transmission gate. When CK is low and

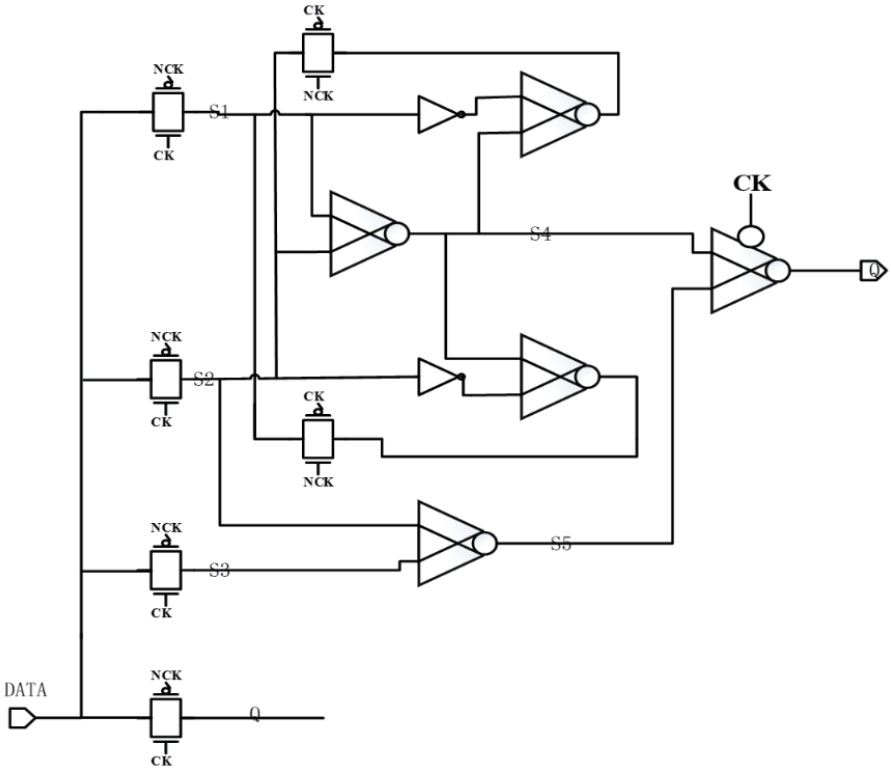


Fig. 7. Equivalent schematic of proposed LDUT latch. Input DATA transfers into CEs controlled by CK and NCK. S1–S5 are the temporary node data, and Q is the final output.

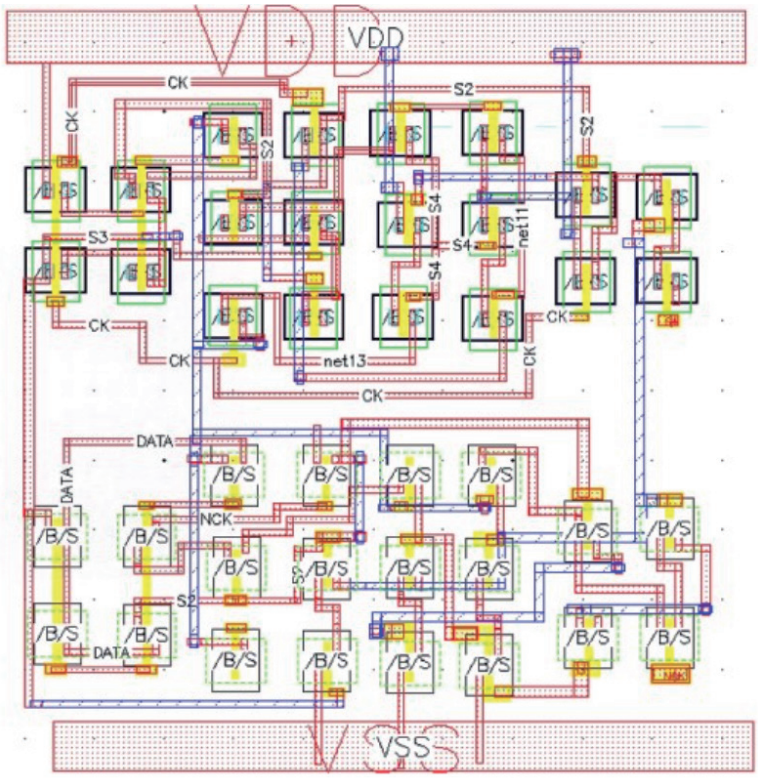


Fig. 8. (Color online) LDUT latch layout illustration. VDD and VSS stand for the power supply.

NCK is high, the latch switches to the hold mode. In this phase, the input to the SRC module is the precharged DATA from the transparent mode, and the output is driven by the CEs within the SRC. The outputs of the SRC and the standard CEs are then fed into the clock-controlled CEs to generate the final output Q.

In the next section, we discuss the fault-tolerant mechanism in the hold mode, taking Q = 1 as an example. Note that the analysis for Q = 0 follows a similar process and is therefore omitted for brevity.

First, the latch's tolerance to SNU is discussed. Since the SRC module inherently enables self-recovery from SNU and the output CEs further mask single-node errors, the latch fully tolerates all possible SNUs. Detailed analysis of SNU tolerance is omitted here owing to its straightforward resolution.

Next, the DNU tolerance mechanism is analyzed. The latch contains five critical nodes (denoted as $CZ = 10$), leading to 10 possible node pair combinations. These scenarios are categorized into two primary cases.

Case 1: Dual-node flips within the SRC module (e.g., <S1, S2>, <S1, S4>, <S2, S4>). In this scenario, all internal nodes of the SRC flip. However, the clock-controlled CEs at the output stage receive only one flipped input, causing it to retain the previous logic state. This effectively neutralizes the SNU propagated from the SRC. Thus, this Case 1 DNU has no impact on the output.

Case 2: A single-node flip inside the SRC and another critical node flip outside (e.g., <S1, S3>, <S1, S5>, <S3, S4>, <S4, S5>, <S2, S3>, <S2, S5>). The SRC's intrinsic SNU self-recovery capability resolves the internal single-node flip. For external flips (e.g., S2 and S3), the CEs between S2, S3, and S5 ensure that a single SNU on S2 or S3 does not propagate to S5. Even if both S2 and S3 flip simultaneously, the error at S5 is blocked by the clock-controlled CEs, preserving the correct output Q. Therefore, the latch fully tolerates the Case 2 DNU.

3.2 Simulation results

The proposed LDUT latch was implemented and evaluated using the TSMC 65 nm CMOS technology, which is widely adopted in low-power mixed-signal and sensor-interface ICs. It is simulated at 1.2 V at room temperature using the Cadence Virtuoso Spectre simulator, a SPICE-level simulation engine capable of accurately modeling transient behaviors, charge-sharing effects, and radiation-induced current pulses. Spectre is particularly suitable for SET/SNU/DNU analysis because its device models include parasitic capacitance and nonlinear transistor responses under fast transient conditions. All compared latches (DNURL, HLDTL, NTHLTCH, HRCE, and DNUSH) were evaluated under identical simulation conditions and workflows. All devices were taken directly from the TSMC 65 nm Process Design Kit (PDK). The PMOS and NMOS transistors employed in all latch modules use the standard-threshold-voltage (SVT) device models provided by the PDK. For fair comparison, PMOS transistors were sized with W/L = 200 nm/60 nm and NMOS transistors with W/L = 200 nm/60 nm across all latches. Figure 9 shows the basic functional waveform of the latch without SNU or DNU injection. The simulation

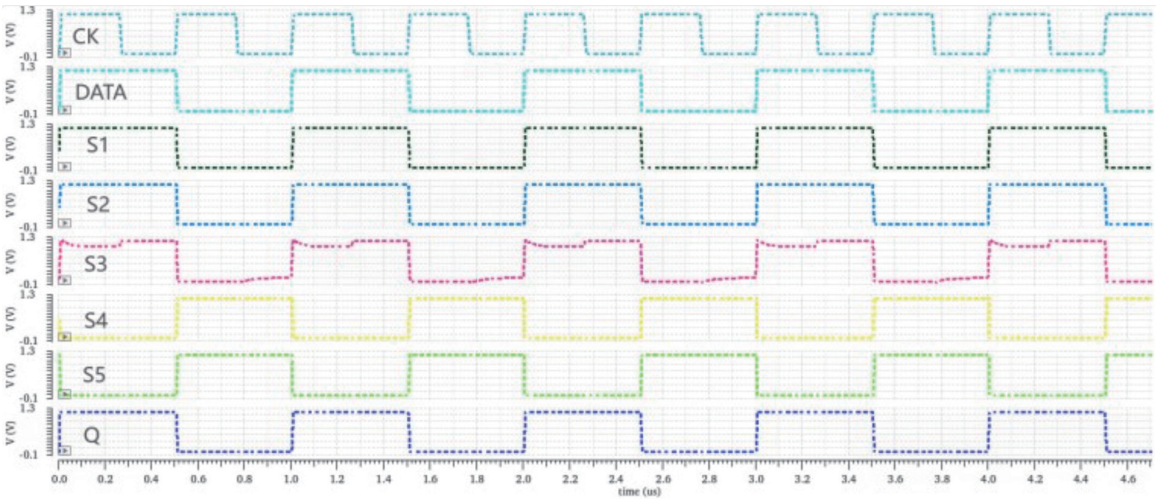


Fig. 9. (Color online) Normal operation waveforms of the LDUT latch. DATA is the input, CK stands for the clock signal, S1–S5 are node voltages, and Q retains its origin value corresponding to input DATA.

results confirm that the proposed latch behaves identically to a conventional static D-latch under normal conditions. The S1–S5 waveforms in the figure represent key nodes of the circuit.

For error injection testing, charge injection was modeled using transient current sources to evaluate the latch's SNU and DNU tolerance. The mathematical expression of the dual-exponential current source model is given in Eq. (1). This model, widely adopted for simulating single-event transient pulses induced by high-energy particles, closely matches actual transient pulse characteristics.[14–16]

$$\begin{cases} I_0 = \dfrac{Q_{in}}{\tau_\alpha - \tau_\beta} \\ I(t) = I_0 \cdot (e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \end{cases} \tag{1}$$

In this dual-exponential current source model, $\tau\alpha$ represents the time constant for the current to rise to its peak value, and τ_β denotes the time constant for the current to decay from the peak to zero.[17,18] On the basis of relevant process parameters from the literature, τ_α is set to 500 ps, and τ_β to 100 ps.[19] As illustrated, DNU tests were conducted on the latch. Figures 10(a) 10(j) illustrate pulse current injection into two randomly selected critical nodes within the circuit in 10 distinct combination scenarios. The results demonstrate that, regardless of the transmitted data, the latch output Q quickly recovers within a short period after any DNU injection, without significant distortion. This confirms that the circuit architecture exhibits robust DNU hardness, with specific nodes demonstrating strong self-recovery capabilities. Since the simulated nodes are all critical ones, the results fully validate the latch's DNU tolerance performance.

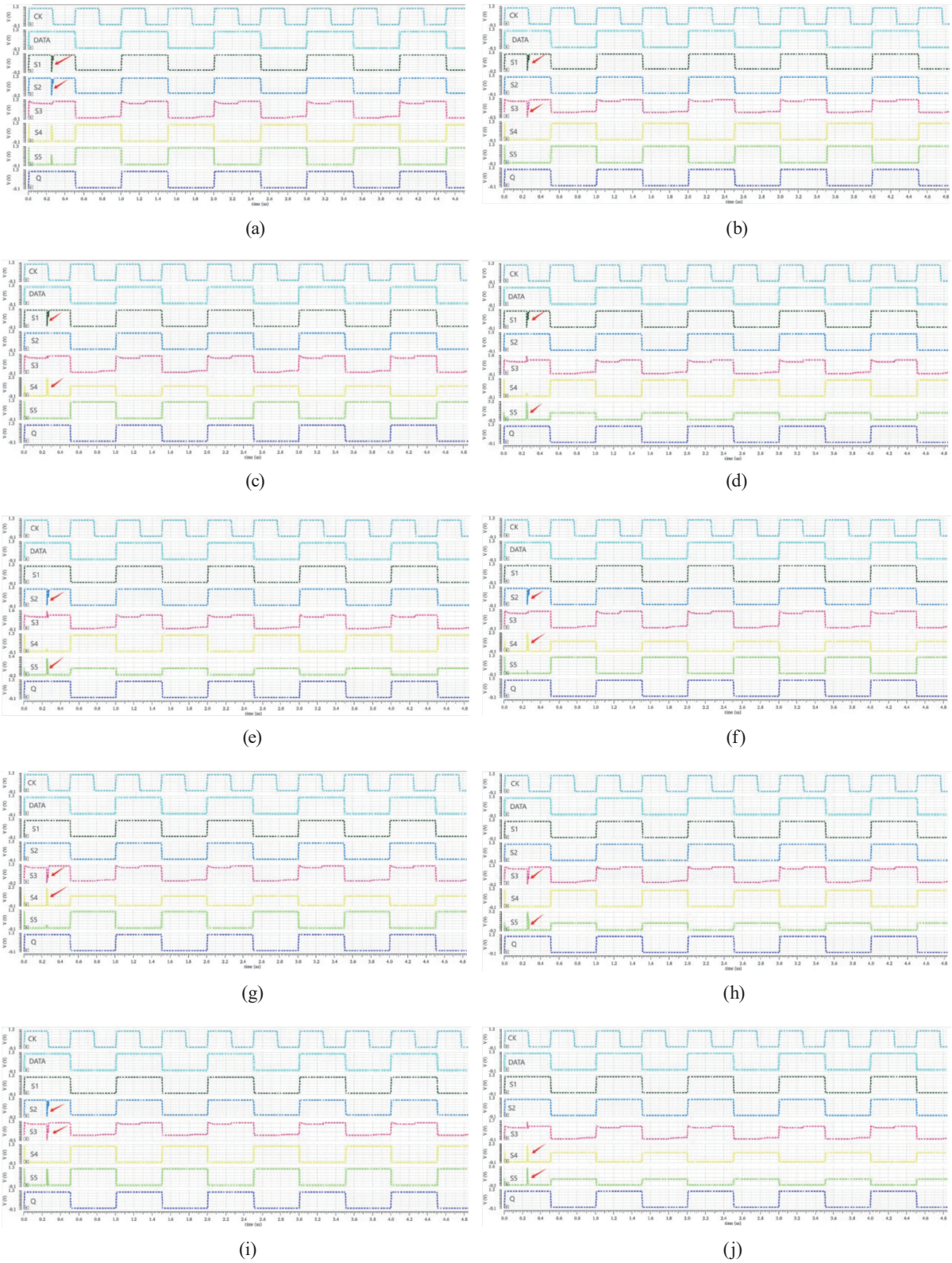


Fig. 10. (Color online) Simulation results of DNU injection into the two different sensitive nodes of the proposed LDUT latch. (a) <S1, S2>; (b) <S1, S3>; (c) <S1, S4>; (d) <S1, S5>; (e) <S2, S5>; (f) <S2, S4>; (g) <S3, S4>; (h) <S3, S5>; (i) <S2, S3>; (j) <S4, S5>. Although there are sharp collapses of node voltage, the LDUT latch shows excellent self-recovery ability to double node injections.

4. Comparison of Latch Performance

All aforementioned latches were implemented under the TSMC 65 nm technology, with transistor sizing configurations consistent with the LDUT latch. Simulation results in Sect. 3 indicated the reliability and radiation tolerance of the proposed LDUT latch against SNU/DNU injections. Table 1 shows the results for the LDUT latch and the latches mentioned in Sect. 2 in terms of delay, power consumption, area, composite metric, and transistor count.[20] The area–power–delay product (APDP) is widely used as a figure of merit (FOM) in RHBD latch evaluation because it captures the trade-off among delay, power, and area simultaneously. Here, area refers to the physical layout area of the latch; power consumption represents the average power dissipation during dynamic and static operation over a clock cycle; delay denotes the average rise and fall propagation delay from the input signal DATA to the output signal Q. The comprehensive APDP metric is defined as follows.

$$APDP = Area \cdot Power \cdot Delay \tag{2}$$

As shown in Table 1, the delay of the LDUT latch is slightly higher than those of HLDTL and DNUSH. The DNUSH latch exhibits excellent low-delay performance, but its complex feedback structure results in higher power consumption and somewhat higher comprehensive metric. The HLDTL that utilizes a large number of transmission gates achieves superior delay performance at the cost of slightly higher power consumption, leading to a marginally elevated APDP. In contrast, the LDUT latch consumes only slightly more power than the NTHLTCH while its area and transistor count remain relatively small. The APDP metric demonstrates that the LDUT latch achieves a prominent balance in overall performance with lower cost. Furthermore, the LDUT latch incorporates the SRC module from the DNURL, significantly outperforming the DNURL in key metrics. Simulation results indicate that the LDUT latch achieves a maximum improvement of 62.72% in power consumption, 30.36% in propagation delay, and 87.33% in APDP compared with other designs.

After comparing the LDUT latch with the latches mentioned in Sect. 2 in terms of the APDP metric, the impact of PVT variations on the LDUT latch and other referenced latches was further analyzed.

Figures 11(a) and 11(b) illustrate the impact of temperature variations from −50 to 150 °C on the power consumption and propagation delay of the latches. The results indicate that higher

Table 1
LDHL latch performance indicators.

Latch	*Delay* (ps)	*Power* (uW)	*Area* (um^2)	*APDA*	Transistor count
LDHL	128.346	0.7672	3.54	348.573	40
DNURL	184.308	1.728	8.64	2751.704	66
HLDTL	117.522	1.024	5.39	648.646	46
NTHLTCH	164.436	0.7277	7.26	868.732	58
DNUSH	118.08	2.058	4.7	1142.140	60
HRCE	125.983	1.24	7.06	1102.906	56

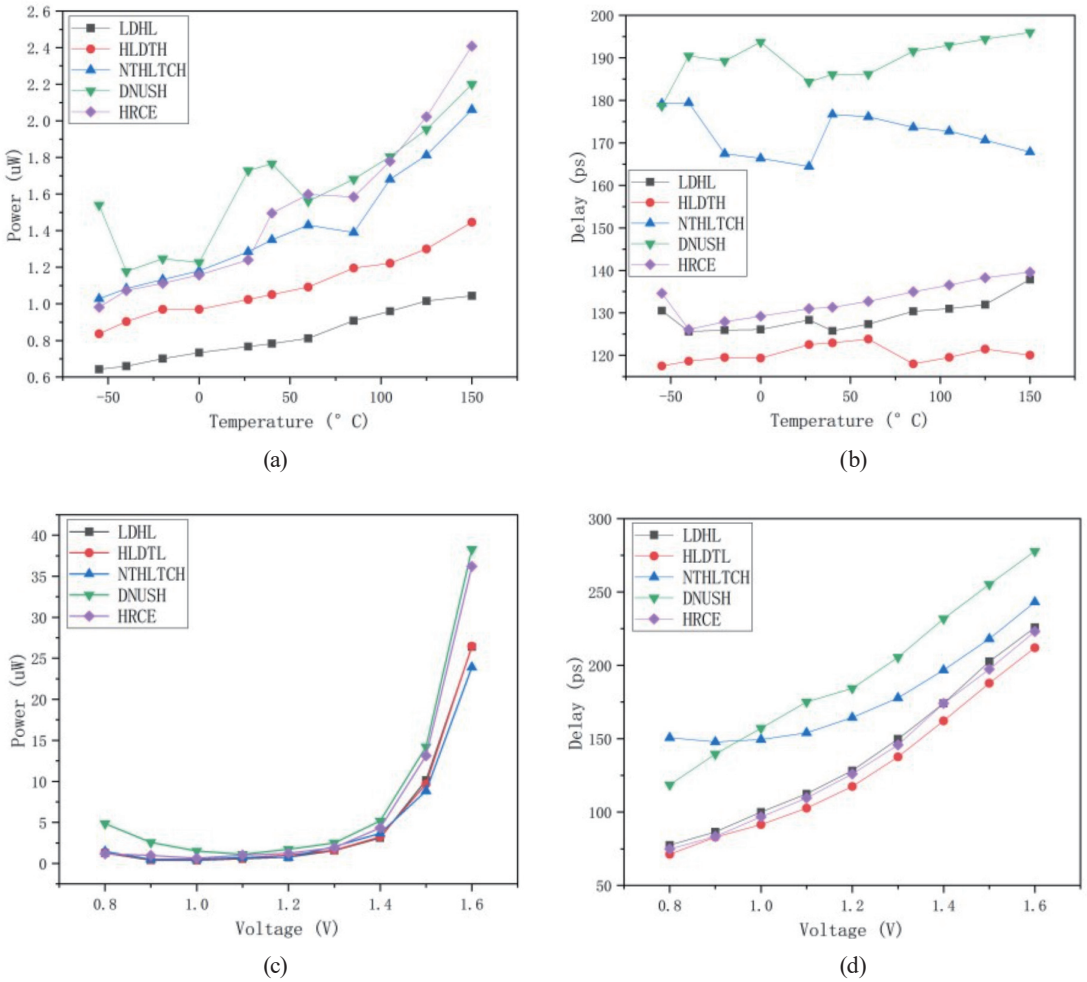


Fig. 11. (Color online) PVT characteristics of proposed LDUT latch cell. (a) Power consumption versus temperature. (b) Delay versus temperature. (c) Power consumption versus supply voltage. (d) Delay versus supply voltage.

temperatures increase power consumption and propagation delay for most latches. However, the LDUT latch exhibits better stability, showing low sensitivity to temperature variations. Figures 11(c) and 11(d) show the effects of voltage variations from 0.8 to 1.6 V on power consumption and propagation delay. The results reveal that as voltage increases, both power consumption and propagation delay exhibit an upward trend.

5. Conclusions

In this work, we proposed a novel low-cost LDUT latch with immunity to SNU and DNU. The design utilized distinct modules and fewer transistors to implement high-speed paths and feedback structures. Simulation results demonstrated that the proposed LDUT latch achieves DNU tolerance and cost-effectiveness compared with other DNU-resistant latch architectures. Compared with the best-architecture HLDTL, the LDUT latch exhibits a 25.08% improvement

in power consumption and a 46.26% improvement in the area–power–delay product. Additionally, temperature variations have minimal impact on the LDUT latch's performance. Compared with previously mentioned latches, the LDUT latch maintains superior performance while balancing key metrics. In summary, the proposed LDUT latch delivers outstanding and balanced performance, particularly those used in sensor interfaces and harsh-environment applications.

References

1 J. D. Black, P. E. Dodd, and K. M. Warren: IEEE Trans. Nucl. Sci. **60** (2013) 1836. https://doi.org/10.1109/TNS.2013.2260357
2 P. E. Dodd and L. W. Massengill: IEEE Trans. Nucl. Sci. **50** (2003) 583. https://doi.org/10.1109/TNS.2003.813129
3 A. Yan, A. Cao, Z. Huang, J. Cui, and T. Ni: IEEE Trans. Emerging Top. Comput. **11** (2023) 1070. https://doi.org/10.1109/TETC.2023.3317070
4 Z. Chen, Y. Xie, and J. Liang: Int. J. Circuit Theory Appl. **52** (2024) 5374. https://doi.org/10.1002/cta.3990
5 M. J. Gadlage, A. H. Roach, A. R. Duncan, A. M. Williams, D. P. Bossev, and M. J. Kay: IEEE Trans. Device Mater. Reliab. **17** (2017) 157. https://doi.org/10.1109/TDMR.2016.2634626
6 S. Tajima, N. Togawa, M. Yanagisawa, and Y. Shi: IEICE Trans. Fundam. Electron. Commun. Comput. E101-A (2018) 1025. https://doi.org/10.1587/transfun.E101.A.1025
7 T. Calin, M. Nicolaidis, and R. Velazco: IEEE Trans. Nucl. Sci. **43** (1996) 2874. https://doi.org/10.1109/23.556880
8 A. Yan, Z. Huang, M. Yi, X. Xu, Y. Ouyang, and H. Liang: IEEE Trans. Very Large Scale Integr. VLSI Syst. **25** (2017) 1978. https://doi.org/10.1109/TVLSI.2017.2655079
9 A. Yan, H. Liang, Z. Huang, X. Xu, Y. Ouyang, and H. Liang: IEICE Trans. Electron. E98-C (2015) 1171. https://doi.org/10.1587/transele.E98.C.1171
10 Y. Yamamoto and K. Namba: Proc. IEEE Int. Symp. on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) (IEEE, 2018) 1–6. https://doi.org/10.1109/DFT.2018.8602841
11 Y. Li, H. Wang, S. Yao, X. Liu, and Q. Zhou: J. Electron. Test. **31** (2015) 537. https://doi.org/10.1007/s10836-015-5551-3
12 S. Kumar and A. Mukherjee: IEEE Trans. Very Large Scale Integr. VLSI Syst. **29** (2021) 2076. https://doi.org/10.1109/TVLSI.2021.3110135
13 H. Li, L. Xiao, J. Li, and C. Qi: Microelectron. Reliab. **93** (2019) 89. https://doi.org/10.1016/j.microrel.2019.01.005
14 T. Wang, L. Xiao, Z. Chen, and H. Liang: Microelectron. Reliab. **55** (2015) 863. https://doi.org/10.1016/j.microrel.2015.03.014
15 Q. Zhou and K. Mohanram: Proc. IEEE/ACM Int. Conf. On on Computer Aided Design. (IEEE, 2004) 100. https://doi.org/10.1109/ICCAD.2004.1382551
16 G. C. Messenger: IEEE Trans. Nucl. Sci. **29** (1982) 2024. https://doi.org/10.1109/TNS.1982.4336490
17 C. M. Hsieh, P. C. Murley, and R. R. O'Brien: IEEE Trans. Electron Devices. **30** (1983) 686. https://doi.org/10.1109/T-ED.1983.21190
18 H. Cha and J. H. Patel: Proc. IEEE Int. Conf. On Computer Design. (IEEE, 1993) 127. https://doi.org/10.1109/ICCD.1993.393319
19 H. Zhang, Z. Liu, J. Jiang, J. Xiao, Z. Zhang, and S. Zou: Electron. Lett. **56** (2020) 1243. https://doi.org/10.1049/el.2020.182
20 Z. Song, A. Yan, J. Cui, Z. Chen, X. Li, and X. Wen: Proc. IEEE Int. Test Conf. Asia (IEEE, 2019) 139. https://doi.org/10.1109/ITC-Asia.2019.00037