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A New Process Technique for Complementary Metal-Oxide-Semiconductor [CMOS] Compatible Sensors

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A new sacrificial-etching-window (SEW) structure is reported for the first time, which can be used for most complementary metal-oxide-semiconductor (CMOS) compatible sensor structures. Using a buried sacrificial layer, the etching windows of the substrate can be extended beneath the membrane. The SEW technique combines the advantages of both surface micromachining by using a sacrificial layer structure and bulk micromachining by anisotropic etching of a silicon substrate. Using the SEW structure, one can speed up the etching rate and design a larger membrane with a larger active area. Several sensors are fabricated by 1.2 μm industrial CMOS IC technologies combined with subsequent anisotropic front-side etching stops. Three kinds of SEW thermoelectric sensors are reported in this paper, and the characteristics of the sensors are analyzed and measured.

1. Introduction

Varieties of silicon-micromachining sensors compatible with industrial CMOS processes combined with one post-processing etching step have been reported in the last decade.[1–7] Using materials and processing steps compatible with standard CMOS or bipolar technology allows highly reliable sensors to be inexpensively batch-produced almost independent of a foundry. Furthermore, the sensor unit can be combined on the same chip with the circuitry necessary for signal conditioning and error compensation. On-chip circuitry enhances sensor performance and noise immunity and provides a totally integrated system.

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Post-etching can be done either from the back or from the front side of the wafer without requiring any further lithography steps. For the front-side etching technique, there are several conventional structures of thermoelectric sensors reported, including microbeam and suspended-bridge membrane structures.[1] The main drawback of the microbeam is that it is very fragile and will bend because of gravity. Therefore, it cannot be made large. For most of the suspended-bridge membrane structures, the area of the membrane is limited by the condition that the extended under-cut etching area of opened windows must overlap. Therefore, the etching time is considerable for the etchant to flow into the windows and carry out etching.

We propose a SEW technique for the first time, which allows more flexible designs of structures to reach a larger area of membrane and reduce etching time. The SEW technique combines the advantages of both the surface micromachining technique using a sacrificial layer and the bulk micromachining technique using anisotropic etching of the silicon substrate. Three kinds of thermopile structures using the SEW technique for CMOS technology have been fabricated and measured in this study. The detectivity of the samples presented can reach over 1.56×10^8 $\mathrm{cm}\sqrt{\mathrm{Hz}}/\mathrm{W}$, which is even larger than that recorded thus far using back-surface etching techniques.[6]

2. Design and Fabrication

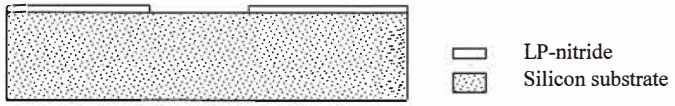
2.1 *Process design*

Using the SEW technique, we present three kinds of samples for the first time, which are fabricated by an industrial 1.2 μm CMOS process, provided by UTEK (United Technology) in Taiwan as the pre-process for silicon micromachining. The anisotropic etching of a silicon substrate is performed using two kinds of etching windows.

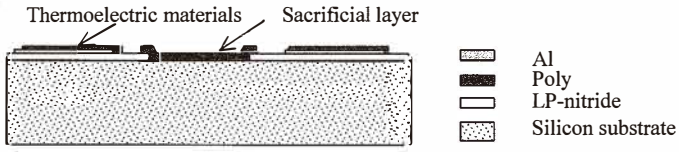
The first pattern is of a "natural" etching window at four corners, which is defined by superimposing a device well, contact cut and pad opening in the standard CMOS mask layout. Using a buried sacrificial layer, the second pattern is of a window defined beneath the membrane and opened after the sacrificial layer is removed. With several via windows patterned on the passivation layer above, the etchant can flow and realize etching under the passivation layer, and the sacrificial layer is easily removed.

The central part of the silicon substrate is removed and only a roughly 2 μm thin sandwich layer of SiO_2/Si_3N_4 is left on top. Onto this membrane, standard materials of two thermoelectric conductors (n-poly, Al) are deposited and structured. An IR-absorbing layer is deposited and patterned to cover the hot junctions. For the post-process, after the CMOS process is finished, anisotropic etching is performed by a hydrazine solution (N_2H_4:H_2O=1:1) at 90°C with an etching rate of about 2 μm/min to etch the silicon substrate beneath the floating membrane. All the samples are etched in under 6.5 h.

Figure 1 shows the process flow of a schematic cross section of the SEW structure. The first step is to open v-groove etching windows in thin oxide (900 Å)/LP-nitride (1500 Å). It is noteworthy that some etching windows are the conventional v-groove etching windows without a sacrificial layer and some are used as sacrificial etching windows which are covered by a sacrificial layer later. After the sacrificial layer is removed, the SEW is the same as the conventional v-groove windows.

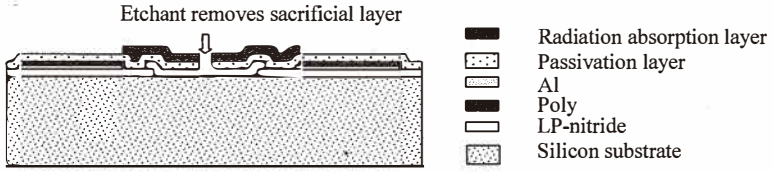


Step 1. A LPCVD nitride layer is grown on a silicon substrate

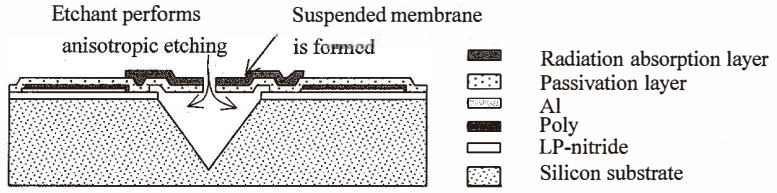


Step 2. The thermoelectric materials are formed and some regions of poly are deposited as a sacrificial

Step 3. Several passivation layers are deposited.



Step 4. Surface micromachining process



Step 5. Bulk micromachining process

Fig. 1. Process flow of SEW fabrication with the standard CMOS process.

The second step is to deposit the thermoelectric materials, n-polysilicon (3800 Å)/ aluminum layers (6000 Å). These materials are easy to use and available in any CMOS process. The n-polysilicon layer is doped with a 60 keV default dose of 10^{14} cm^{-2} at UTEK.

In addition to the thermoelectric application, it is important to apply the polysilicon to serve as the sacrificial layer, which is deposited directly over the SEW without a thin oxide/LP-nitride beneath. Therefore, after the sacrificial layer is removed, the anisotropic etchant N_2H_4 can etch the substrate via the wide SEW.

For the third step, after the deposition of thermocouples, several passivation layers, PECVD oxide (5000 Å)/PECVD nitride (5000 Å) are deposited to protect the thermocouples and to compensate for the stress in the membrane. After the deposition of passivation layers, a 50 Å NiCr thin film is sputtered and patterned by a lift-off process to be used as a blackbody layer.

The fourth step is to open etching windows in the passivation layers and blackbody layer and then remove the underlying sacrificial layer. Some etching windows are defined as the conventional v-groove windows and some are used as via windows to allow the etchant of polysilicon to enter and remove the sacrificial layer. The via windows of the passivation layers are much smaller than the SEW. From the top view of the sensor, via windows cover only a small area and therefore more area of the membrane could be used to position the thermocouples. Therefore, the fourth step is performed as a typical surface-micromachining process.

The final step is designed to etch the silicon substrate through the via windows and the conventional v-groove windows. After the etchant, a hydrazine solution (N_2H_4) flows through the via windows and then flows laterally along the SEW to attack the substrate beneath the SEW. Therefore the fifth step is performed as typical bulk-micromachining.

2.2 *Fabrication of samples*

Three new structures of membrane are proposed, and named HM236S1, HM236S2 and OTC236S1. The first one, HM236S1, with 56 pairs of thermoelectric elements, is well constructed on an 1100×1100 mm^2 floating membrane. The SEW is patterned as a cross shape in the central part of the membrane, which is shown in Fig. 2, using a polysilicon layer 20 μm wide. Along the cross pattern of SEW, there is only one row of via windows for each strip of SEW; the windows have a small circle pattern 14 μm in diameter, shown in Fig. 3. Therefore, the hydrazine solution can flow through the via windows and along the cross shape of the SEW to realize the anisotropic etching so that the silicon substrate beneath the central part of membrane is etched.

In Fig. 4, the four corners of the membrane were not used to position the thermocouples because the process would be inefficient. Therefore, four conventional v-groove windows at the corners are opened to let more etchant enter the SEW laterally and directly etch the silicon substrate to accelerate the etching process. Using the SEW and v-groove windows at the corners, the silicon substrate is etched, and after the etching a pyramidal cavity is left, as shown in Fig. 5.

The second sample, HM236S2, shown in Fig. 6, with 92 pairs of thermoelectric elements is well constructed on a floating membrane with the same area as HM236S1. A cross pattern of SEW is also used and two parallel rows of via windows are opened to a diameter of 4 μm, as shown in Fig. 7. The silicon substrate is etched via the SEW and v-groove windows, and after the etching a pyramidal cavity is left.

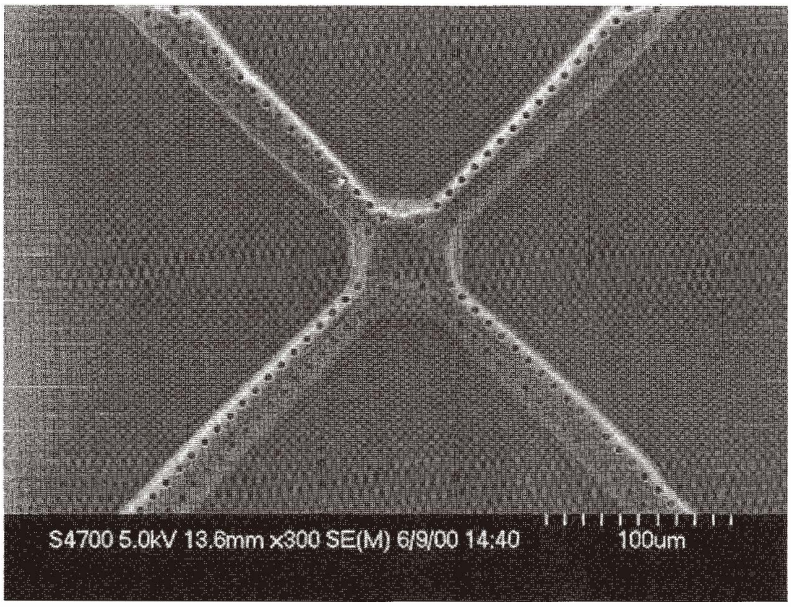


Fig. 2. The cross area of SEWs in the central part of the membrane.

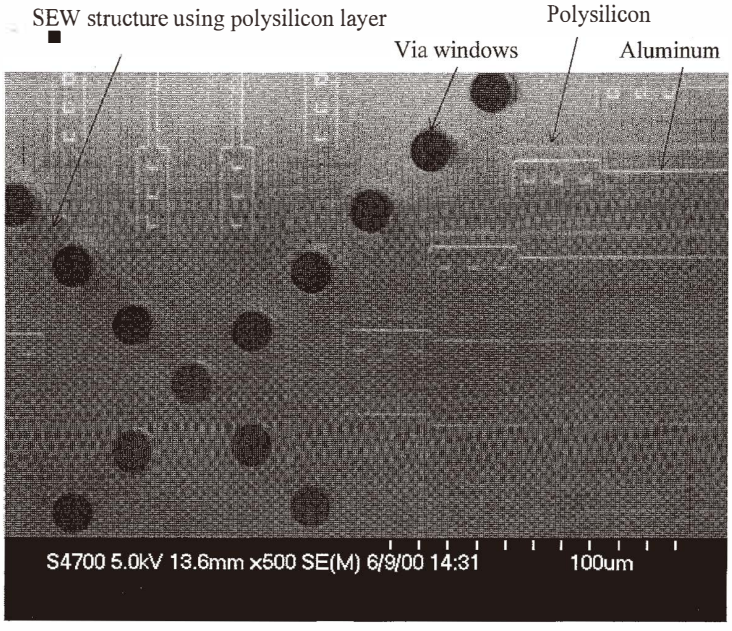


Fig. 3. SEM of SEWs of sample HM236S1.

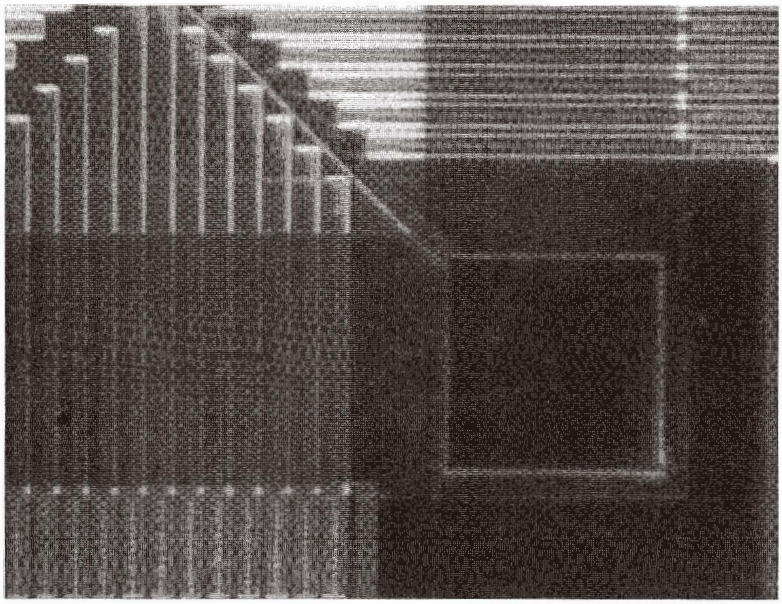


Fig. 4. Photograph of etching windows at the corner of the floating membrane.

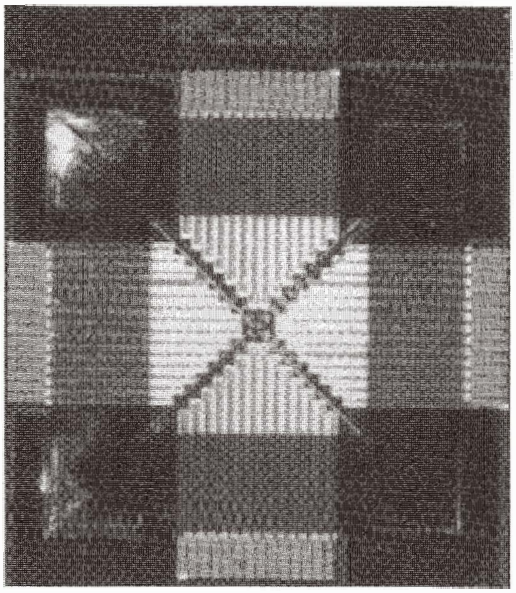


Fig. 5. Photograph of the overview of sample HM236S1.

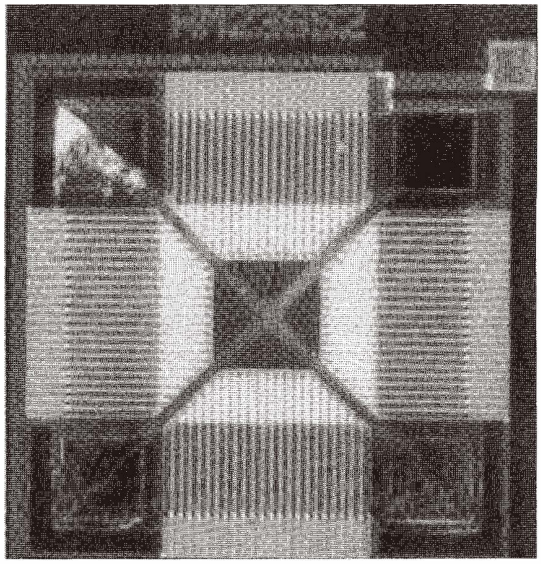


Fig. 6. Photograph of the overview of sample HM236S2.

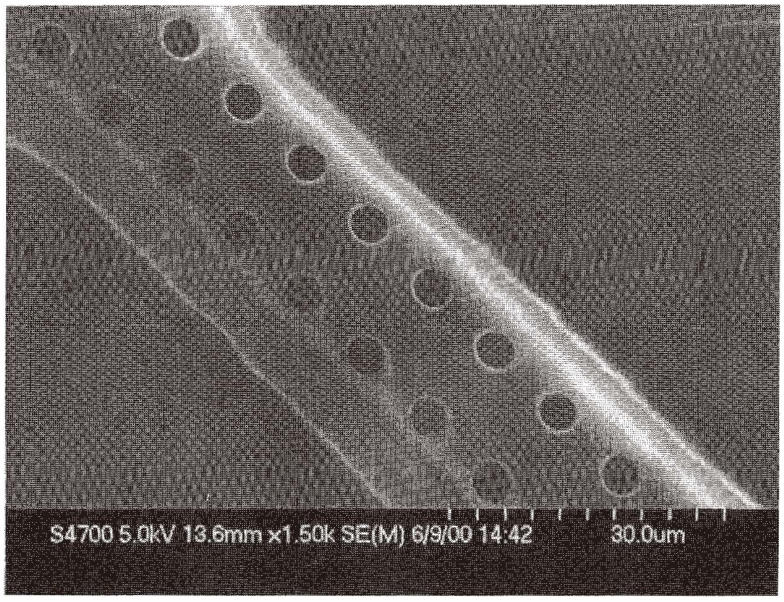


Fig. 7. SEM of SEWs of sample HM236S2.

The third sample, OTC236S1, which is shown in Fig. 8, with 44 pairs of thermoelectric elements is well constructed on a floating membrane with four leads and has the same area as HM236S1. Conventionally, for the four-lead membrane, the substrate beneath the central part of the membrane is etched after the undercut of leads and overlaps each lead. It is interesting to compare the performance of this conventional structure with samples HM236S1 and HM236S2, which have more active area to collect radiation and on which to place the thermocouples.

This sample is designed to use the SEW at the central part of the membrane by modifying the conventional four-lead membrane.[7] The SEW is patterned as a circle 200 μm in diameter, and 16 small via windows are symmetrically placed around the circle. The etchant flowing through the via windows provides a faster etching rate in the central part of membrane.

3. Measurements

Responsivity and spectral-response measurements were carried out in air using a blackbody source at 500 K with a 5.78-μm peak wavelength. In front of the blackbody source, a mechanical chopper was located to modulate the radiation from the source to the measured samples. All of the sensors were packaged in a standard TO-5 metal can to avoid environmental interference.

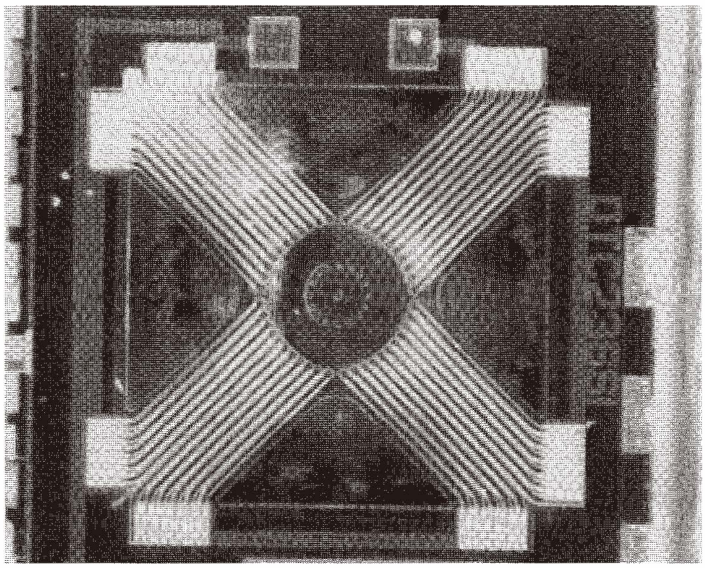


Fig. 8. Photograph of the overview of sample OTC236S1.

The packaged samples were placed on a holder 12 cm from the blackbody source, and the signals from the sensors were picked up with a phase-loop-lock-in amplifier SR530. The signals were automatically read out by a GBIP interface to a PC, which controls both the SR530 and the frequency of chopper.

Using Labview 5.0 software, a control program was created automatically to handle all the measurements. To calibrate the responsivity of samples at the same time, a calibrated thermopile sensor was used.

4. Results and Discussion

To evaluate the characteristics of the thermopile using different structures with the same materials, we construct Table 1 to compare the data between the SEW samples with reported devices which use the conventional thermoelectric materials (n-poly, Al) in CMOS technology.

One of the important characteristics is the sensitivity, which produces a larger voltage with more incoming infrared radiation power. We can see from Table 1 that the sensitivities of HM236S1 and HM236S2 are high, over 100 V/W, which is even higher than the back-surface-etched device.[6] Considering the noise, the dominant noise of a thermopile is the Johnson's noise. Although the sensitivity of HM236S1 is 102 V/W lower than the sensitivity of HM236S2, 125 V/W, the resistance of the HM236S1 is also lower than that of HM236S2. This means that HM236S1 produces less noise than HM236S2.

Therefore, to evaluate the total performance of a sensor, it is necessary to compare the figure of merit, i.e., the detectivity. For the front-side etched thermopile devices using the same thermoelectric materials as in the CMOS process, the detectivities are always small and on the order of magnitude of 10^7 $cm\sqrt{Hz}$ / W.[6] For HM236S1 and HM236S2, the detectivities are over 1.56×10^8 and as such are higher than all devices previously reported

Table 1
Table showing comparisons of different thermopiles.

Parameter	Unit	OTC236S1	HM236S1	HM236S2	H. Baltes[3]	TPS434[6]
Chip size	mm^2	1.72×1.95	1.72×1.95	1.72×1.95	–	2.2×2.2
Elements N		44	56	92	40	40
Resistance	kΩ	70	67	95	–	40
Sensitivity	V/W	65	102	125	30	48
NEP	$nW / \sqrt{Hz}$	0.5	0.32	0.31	–	0.54
Detectivity D*	$cm\sqrt{Hz} / W$	9.71×10^7	1.56×10^8	1.60×10^8	3×10^7	9.3×10^7
Time constant	ms	18	18	18	10	20
Etching Method		Front-side	Front-side	Front-side	Front-side	Back-surface

using the front-side etching method.[3] Moreover, it is also sufficiently good to compete with the back-surface-etched device.[6] The OTC236S1 device has poor performance not only in sensitivity but also in noise, and we predict that the major difference is the small active region of absorption compared with HM236S1 and HM236S2.

5. Conclusions

In this report, we propose a new structure for floating membrane devices for the first time, which enhances the structure by realizing in a large membrane area and a reduction in the etching time. The SEW technique combines the advantages of both the surface micromachining technique using a sacrificial layer structure and the bulk micromachining technique by anisotropic etching of the silicon substrate. Therefore, for the first time we have successfully fabricated thermoelectric sensors with the largest membrane area for front-side etching devices.

The sensitivities of the SEW samples are larger than reported devices and are even over 100 V/W. The detectivity of proposed samples HM236S1 and HM236S2 can reach over 1.56×10^8 $\mathrm{cm}\sqrt{\mathrm{Hz}}/\mathrm{W}$, which is even larger than that cited in existing reports using the back-surface etching techniques. A larger area of membrane structure can be achieved using SEW structures, and more flexible structures could be designed by incorporating this process technique.

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