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Integrated High-Speed, High-Sensitivity Photodiodes and Optoelectronic Integrated Circuits

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A review of the properties of photodiodes available through the use of standard silicon technologies is presented and some examples of how to improve monolithically integrated photodiodes are shown. The application of these photodiodes in optoelectronic integrated circuits (OEICs) is described. An innovative double photodiode requiring no process modifications in complementary metal-oxide semiconductor (CMOS) and bipolar CMOS (BiCMOS) technologies achieves a bandwidth in excess of 360 MHz and data rates exceeding 622 Mb/s. Furthermore, a new PIN photodiode requiring only one additional mask for the integration in a CMOS process is capable of handling a data rate of 1.1 Gb/s. Antireflection coating improves the quantum efficiency of integrated photodiodes to values of more than 90%. Integrated optical receivers for data communication achieve a high bandwidth and a high sensitivity. Furthermore, an OEIC for application in optical storage systems is introduced.

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1. Introduction

Photons with an energy larger than the band gap generate electron-hole pairs in semiconductors. This photogeneration G obeys an exponential law:

$$G(x) = \frac{\alpha P_0}{A h \nu} \exp(-\alpha x), \quad (1)$$

where x is the penetration depth coordinate, P_0 is the nonreflected portion of the incident optical power, A is the light-sensitive area of a photodiode, $h\nu$ is the energy of the photon, and α is the wavelength-dependent absorption coefficient. Photogeneration, i.e., the optical absorption coefficient, and the transport mechanisms of photogenerated carriers determine the speed and the dynamic quantum efficiency of photodiodes.

There are two transport mechanisms for electrons and holes photogenerated in semiconductors: carrier drift and carrier diffusion. Drift is a fast mechanism; however, slow diffusion of photogenerated carriers usually limits the bandwidth and the dynamic quantum efficiency of pn photodiodes available in standard CMOS and BiCMOS technology to several megahertz.[1,2] Measured results for the n^+/p-substrate photodiode fabricated by a 0.8-μm BiCMOS technology confirm these findings. Other photodiodes in typical standard-buried-collector (SBC)-based BiCMOS technology only achieved a low quantum efficiency due to the thin epitaxial layer (n^-collector) used as the intrinsic region of a PIN photodiode.[3,4] For a high quantum efficiency, all carriers should ideally be photogenerated within the drift region. To increase the quantum efficiency and to avoid the slow diffusion of photogenerated carriers by extending the space-charge region, up to three additional masks (without masks for antireflection coating) for the integration of fast PIN photodiodes with a thick intrinsic region were used in a SBC based bipolar process.[5,6] In this work, the innovative double photodiode approach is described, which does not require additional process complexity to achieve faster integrated photodiodes and to improve the quantum efficiency in the red region of the spectrum. In addition, a new PIN photodiode with a high quantum efficiency requiring only one additional mask in a CMOS process and extending the bandwidth further is shown. Results of PIN photodiodes integrated on p-type and n-type substrates are compared and the innovative photodiodes are implemented in advanced OEICs.

2. Materials and Methods

Direct band-gap III/V semiconductor materials such as GaAs, InP and InGaAs possess a steep absorption edge for light.[7] The large absorption coefficients in the visible and near-infrared spectral range allow thin III/V absorption regions and a very fast photodetector response enabling data rates in excess of 20 Gb/s.[8] The optical absorption coefficient of the indirect semiconductor material Si is much lower for wavelengths larger than approximately 400 nm.[7] Thicker Si absorption regions are therefore necessary for a high quantum efficiency, resulting in a slower transient response.

The crystal growth and process technologies of III/V materials, however, cannot compete with those of silicon. Defect densities are much higher in III/V crystals, hindering the fabrication of highly integrated III/V circuits. The III/V chips, therefore, only contain approximately 10^5 transistors, whereas Si dynamic random access memory (DRAM) chips contain up to 10^9 transistors. The prices of III/V photodetectors and integrated circuits are much higher than those of Si photodetectors and integrated circuits. Silicon, therefore, is the first choice in microelectronics. A low price for optical sensor chips is important for high volume applications in automation and consumer electronics. Silicon allows the integration of photodetectors and signal-processing circuits monolithically on one chip, resulting in a low price and a high reliability. The monolithic integration improves immunity against electromagnetic interference (EMI) compared to two-chip solutions with a photodetector chip and an amplifying or signal-processing chip. This improvement is due to a very short connection between the photodetector and the amplifier in an OEIC. A one-chip solution, i.e., an OEIC, avoids bond pads and their parasitic capacitance, thereby increasing the bandwidth. For some applications, the die area of the integrated photodiodes is smaller than the die area which would be needed for bond pads, resulting in a cost advantage. The OEICs for optical storage systems such as CD-ROMs and digital-versatile-disks (DVDs), for instance, are such examples, where the die area for photodiodes is smaller than for the corresponding number of bond pads. Receivers for short-range optical communication and data transmission in the wavelength range of 630–850 nm via plastic optical fibers (POFs) and optical silica-based fibers in local area networks are another application of silicon OEICs. This article presents the results of integrated photodiodes and OEICs for these two applications. Although silicon cannot compete with the bandwidths of III/V photodetectors, it will be shown that silicon photodetectors and OEICs can achieve data rates of more than 1 Gb/s and bandwiths of more than 1 GHz.

The development of OEICs is supported by process and device simulation programs such as SUPREM, TSUPREM, MEDICI and ATLAS with implemented photogeneration. Process technologies, therefore, can be investigated by simulation with respect to the properties of photodiodes available in these technologies. Circuit simulation programs are extensively used for chip development in universities, research institutes and microelectronic companies. Examples of frameworks including circuit simulation, layout, extraction and verification tools are CADENCE and MENTOR. For the development of ASICs, circuits and layouts are available to customers of foundries in libraries. It can be concluded that there is much know-how and that there are many tools that can be exploited to develop OEICs. No special simulation tools have to be created for the investigation of integrated photodiodes and for the development of OEICs. Some very interesting results for integrated photodiodes and OEICs can now be described in detail.

3. Results

3.1 n^+/p-substrate photodiode

Most modern CMOS and BiCMOS processes implement self-adjusting well formation and require only one lithography step for the formation of both n- and p-type wells. Therefore, throughout a wafer or a chip, either a p-type well or an n-type well is present.

The p-type doping concentration in an n^+/p-substrate photodiode (Fig. 1) consequently is higher than 10^{16} cm^{-3}, and the space-charge region, i.e., the drift region for photogenerated carriers, is very thin. In turn, a large portion of the carriers is photogenerated outside the space-charge region and a large contribution of slow carrier diffusion to the photocurrent results (Fig. 2). For measurements, an emitter coupled logic (ECL) generator was used to modulate a diode laser with a wavelength of 638 nm. The laser light was coupled into the photodiode on a wafer prober by an optical single-mode fiber.

The transient response of the photodiode was measured with a digital sampling oscilloscope HP54750/51 and a picoprobe (pp) with an input capacitance of 100 fF and a bandwidth of 3 GHz. The frequency response of the photodiode was measured using the picoprobe and a network analyzer HP8751A, which also modulated the laser in this case. A 500-Ω polysilicon resistor was integrated with the photodiode to allow its transient characterization. The rise and fall times determined from Fig. 2 are 26 ns and 28 ns, respectively. The measured –3 dB frequency is only 6.7 MHz.[9]

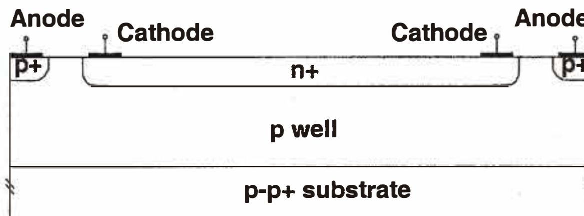

Fig. 1. Cross section of an n^+/p-substrate photodiode obtained through the use of a technology based on self-adjusting wells.

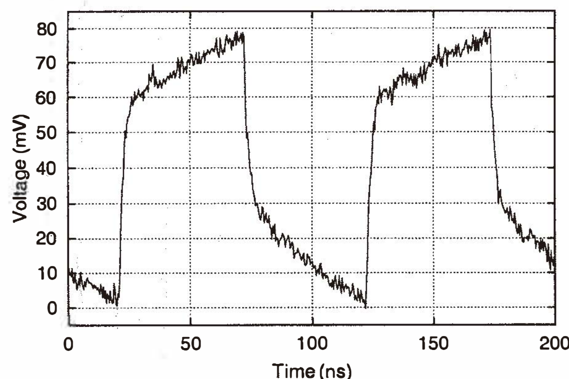

Fig. 2. Transient response of an n^+/p-substrate photodiode fabricated by an industrial 0.8-μm BiCMOS technology based on self-adjusting wells.

3.2 *Double photodiode*

To avoid the slow diffusion of photogenerated carriers for wavelengths shorter than approximately 650 nm without additional process steps, an innovative double photodiode (DPD) is suggested (Fig. 3). The limitation of slow carrier diffusion is avoided using two vertically arranged p/n junctions. One p/n junction is formed by a p^+-source/drain region and an n-well in CMOS or BiCMOS technology. The other p/n junction is composed of the n well and the p substrate. Both anodes of the double photodiode are connected to the ground.

The DPD with a light-sensitive area of approximately 23×23 μm^2 was fabricated by an 0.8-μm BiCMOS process. For the characterization of the transient behavior, a bipolar transimpedance amplifier (Fig. 4) with a simulated postlayout bandwidth of 640 MHz was integrated with the DPD.

The transistor Q1 is used in common emitter configuration with the load resistor R1. Transistor Q2 works as an emitter follower reducing the output impedance. Together, Q1, Q2 and the feedback resistor R_{fb} form a transimpedance amplifier. The source follower Q3

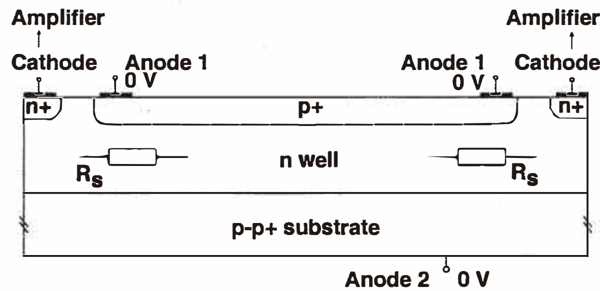

Fig. 3. Cross section of a double photodiode.

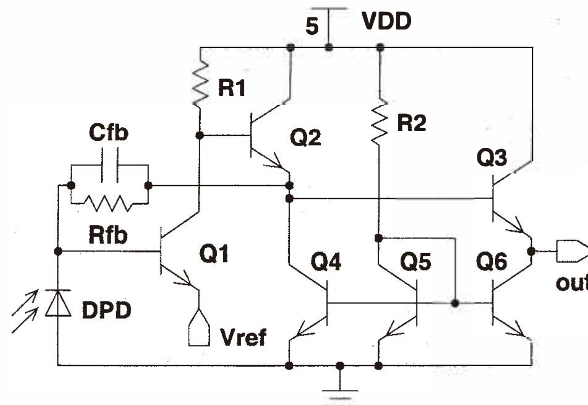

Fig. 4. Bipolar transimpedance amplifier integrated with the double photodiode in an OEIC.

decouples the feedback path from the output and provides some level shifting towards V_{ref} = 2.5 V. The reverse voltage across the DPD is $V_{ref} + V_{BE} \approx 3.3$ V.

Rise and fall times of 0.49 and 0.89 ns, respectively, were measured for this reverse bias at the DPD (Fig. 5). From the oscilloscope values $t_r^{osc,disp} = 0.49$ ns and $t_f^{osc,disp} = 0.89$ ns, the rise and fall times t_r^{DPD} and t_f^{DPD} of the DPD would have to be evaluated according $(t_{r/f}^{DPD})^2 = (t_{r/f}^{osc,disp})^2 - (t_{r/f}^{Laser})^2 - (t_{r/f}^{pp})^2 - (t_{r/f}^{osc})^2 - (t_{r/f}^{amp})^2$. Without knowing $t_{r/f}^{amp}$ exactly, however, only upper limits $t_r^{DPD} \leq 0.37$ns and $t_f^{DPD} \leq 0.70$ns can be estimated. Using a rather conservative estimate, the non-return-to-zero (NRZ) data rate DR = $2/(3(t_r + t_f)) \geq 620$ Mb/s can be derived for the DPD bipolar transimpedance amplifier OEIC.[9] A –3 dB bandwidth of 367 MHz has been measured for the DPD with a network analyzer modulating the laser. For the DPD realized without an amplifier, a dark current of less than 1 pA at room temperature was measured for reverse biases of up to 5 V.[9] The responsivity R = 0.40 A/W of the DPD was increased to R = 0.49 A/W (quantum efficiency η = 95 %) by an antireflection coating (ARC) optimized for a wavelength of 638 nm.

The bandwidth improvement of the DPD over the n^+/p-substrate photodiode for red light can be explained in the following way: At the two vertically arranged p/n junctions, two space-charge regions are present. Both anodes, i.e., the surface anode and the substrate anode, are biased at 0 V and the common cathode is biased at 3 V, for instance. In the first space-charge region at the p^+/n-well junction, the photogenerated electrons, therefore, drift towards the n well and the photogenerated holes drift to the p^+ anode at the silicon surface. In the second space-charge region at the n-well/p-substrate junction, the photogenerated electrons drift to the n well and the photogenerated holes drift towards the p substrate. In addition to the two zones with a high electric field in the two space-charge regions, an electric field in the vertical direction exists between the two space-charge regions (Fig. 6) due to the doping gradient of the n well. In the lateral direction, carrier transport is ohmic in the n well in the low-field zone. Because of the vertically directed electric field and the

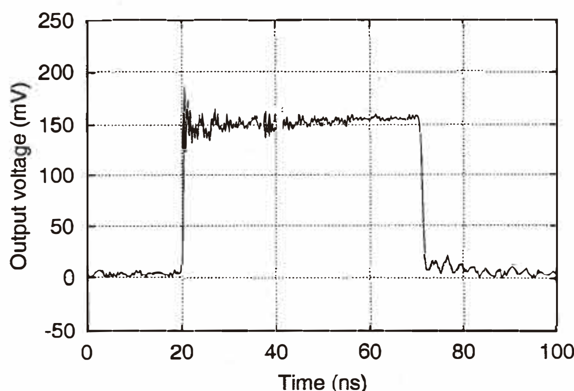

Fig. 5. Transient response of the DPD with an area of 530 μm^2.

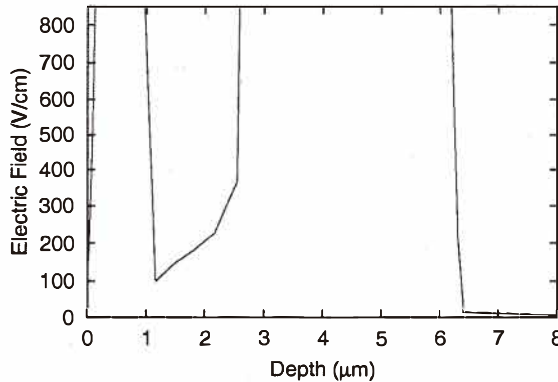

Fig. 6. Electric field in a double photodiode vs depth.

two space-charge regions, drift regions are present throughout the penetration depth of the light and the slow contribution of carrier diffusion to the photocurrent is eliminated for red light. For deeper-penetrating infrared light with a wavelength of 850 nm, the space-charge region does not penetrate deep enough into the silicon. Carrier diffusion, therefore, is still a problem for light with a wavelength of 850 nm.

Compared to an investigation in which a bandwidth of 156 MHz and rise and fall times of 1.8 ns and 1.9 ns, respectively, were measured for the DPD with a size of 2700 μm^2 at an integrated polysilicon resistor of 500-Ω,[10] the speed of the DPD has been improved because of the integrated amplifier with an input impedance of approximately 100 Ω.[11] With the integrated amplifier, the limitation due to the time constant of the 500-Ω resistor and of the bond pad plus DPD capacitances is avoided. In addition, the series resistance R_S present in the n well of the DPD is reduced due to the smaller DPD size of 23 × 23 μm^2. Therefore, the values of 0.37 and 0.70 ns for t_r^{DPD} and t_f^{DPD}, respectively, better characterize the intrinsic drift speed of the DPD.[9]

3.3 *DPD BiCMOS OEIC for optical storage systems*

OEICs for optical storage systems such as CD-ROMs or DVDs contain eight photodiodes and eight amplifiers. The four channels A–D are fast channels for reading the stored information and for extracting the focus error signal. The other four channels E–H are sensitive channels for tracking control. Due to the DC coupling of signal-processing circuits in a DVD system, a low output offset voltage with respect to the reference voltage U_{REF} = 2.5 V of the OEIC channels is required. This low-offset condition usually can only be fulfilled with operational amplifiers. The photocurrent-to-voltage conversion is usually carried out using an operational transimpedance amplifier. Such a circuit for channels A–D of a DVD OEIC is shown in Fig. 7.[12] Three different gains H (high), M (medium), and L (low) are switchable by MOS transistors for universal applicability of the OEIC in DVD video, DVD ROM and DVD RAM systems. The circuit was implemented using a 0.8-μm BiCMOS technology.

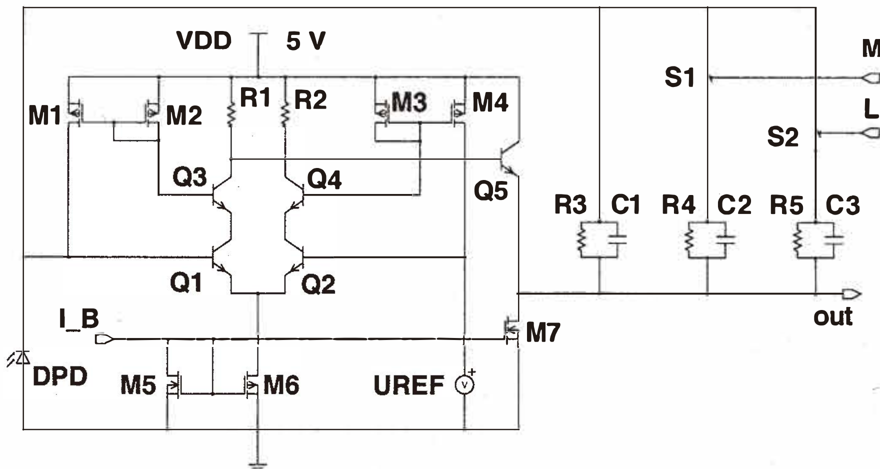

Fig. 7. Schematic of a fast-channel BiCMOS OEIC for optical storage systems.

Only npn transistors are used in the signal path to achieve a high bandwidth. Without Q3, Q4 and M1–M4, the base current of the input transistor Q1 would flow across one of the feedback resistors and cause an output offset voltage of more than 100 mV, which is far beyond the specification. Therefore, the bias current cancellation using Q3, Q4 and M1–M4 is implemented. Transistor Q3 senses the base current of Q1, and this current is mirrored to the base of Q1 via M2 and M1. Components Q4, M3 and M4 are needed for reasons of symmetry. In this way, the output offset voltage is reduced below a value of 11 mV for a feedback resistor of 20 kΩ. The results for such a fast channel are listed in Table 1.

In the sensitive channels, feedback resistors of 200 kΩ are needed and the bias current cancellation used in the fast channels would violate the offset specification. Therefore, the source followers M1 and M2 are implemented at the inputs of the operational amplifier shown in Fig. 8. The bandwidth of the sensitive channels is much lower than that of the fast channels, and the load resistors in the difference amplifier stage are substituted by the PMOS transistors M3 and M4 to increase the gain. The results for such sensitive channels are included in Table 1.

Table 1 shows that an operational BiCMOS amplifier in transimpedance configuration can combine a bandwidth of 90 MHz with a low output offset voltage of less than 11 mV and with a sensitivity of 8.8 mV/μW at a wavelength of 638 nm. The sensitive channels achieved bandwidths in excess of 5 MHz with offset voltages less than 7.5 mV and a sensitivity of 88 mV/μW for $\lambda = 638$ nm.

The power consumption of the eight-channel OEIC was approximately 75 mW at a supply voltage of 5 V. The total OEIC die area was 3.25 mm^2. The demonstration of this OEIC for applications in optical storage systems was possible due to the implementation of the double photodiode without process modification (disregarding modification for antireflection coatings).

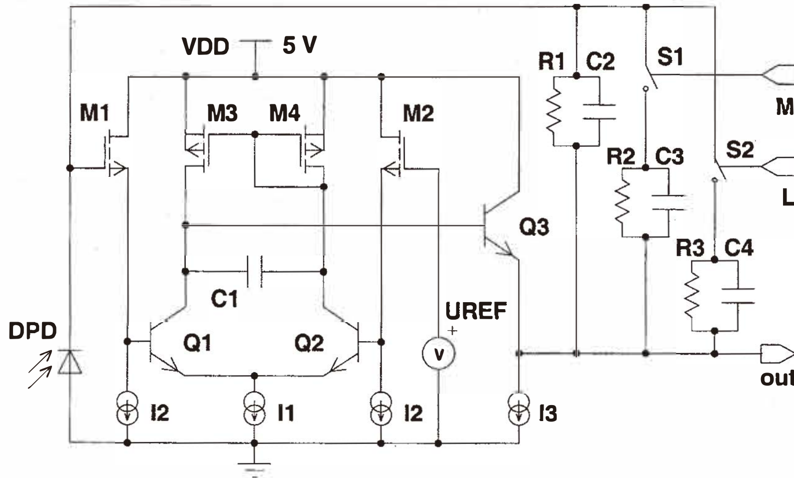

Fig. 8. Schematic of a sensitive channel BiCMOS OEIC for optical storage systems.

Table 1
Measured results of the high-bandwidth BiCMOS OEIC for optical storage systems.

	H	M	L
f_{-3dB} (MHz) A–D	92.0	94.9	95.1
f_{-3dB} (MHz) E–H	5.2	8.5	14.6
Sensitivity (mV/μW) A–D	8.8	2.9	0.9
Sensitivity (mV/μW) E–H	88.1	29.3	9.1
U_{offset} (mV) A–D	<10.8	<9.5	<9.0
U_{offset} (mV) E–H	<7.4	<6.4	<6.4
Noise (dBm) A–D	–81.5	–85.0	–85.2
Noise (dBm) E–H	–66.0	–67.5	–73.5

3.4 *PIN photodiode*

The integration of PIN photodiodes allows even faster photoresponses than that of the double photodiode, but at the expense of a slightly increased process complexity. For the 1.0-μm twin-tub CMOS process used here, which is not based on a self-aligned well process scheme, only one additional mask (photodiode protection mask) is necessary to block out an originally unmasked p-type threshold implant from the photodiode area.

Figure 9 shows a schematic cross section of a twin-tub CMOS optical receiver. The key step for its performance enhancement is the reduction of the doping concentration C_e in the epitaxial layer. This, however, does not result in further process complexity for a CMOS fab, because the epitaxial wafers are purchased. The electrical performance of the MOS transistors is not influenced as they are placed in wells with doping levels above 10^{16} cm^{-3} and as the threshold implantations generate doping levels of approximately 10^{17} cm^{-3}. It has been verified in experiments that the transistor parameters do not depend on C_e in the range from $\approx 10^{15}$ cm^{-3} to 2×10^{13} cm^{-3} and that the transistor parameters specified for the

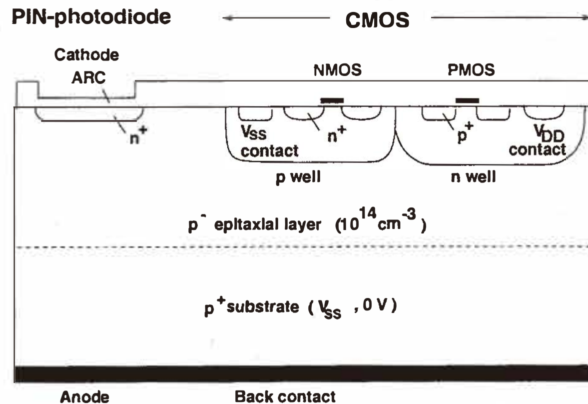

Fig. 9. Cross section of CMOS-integrated PIN photodiode.

original CMOS process can be used for circuit simulations of OEICs.(13) Returning to Fig. 9, the highly doped substrate serves as the anode of the PIN photodiode, requiring an ohmic contact at the reverse side of the wafer, which is either part of many modern processes for latch-up prevention anyway or is easy to provide.

A danger involving latch-up exists at places where n- and p-type wells are in contact. Figure 10 shows p- and n-type regions acting as parasitic bipolar transistors in a CMOS cross section.

A thyristor results, which can turn on, for instance, when the base-emitter voltage of one of the transistors exceeds a value of approximately 0.6 V due to a lateral current in one of the wells across R_{wp} or R_{wn} as a result of voltage spikes on the well-interconnect lines. The turn-on of the thyristor leads to a shorting of V_{DD} and V_{SS} and the transistors lose their function in the circuit at least until the next power-off and power-on. They may even be destroyed due to large currents resulting in strong heating. Therefore, latch-up has to be excluded by proper design.

Figure 11 shows the results of latch-up test measurements for various doping levels in the epitaxial layer at a special test structure with an n^+/well-boundary and p^+/well-boundary distance of 2 μm. This test structure can be obtained from Fig. 10 when the drain regions, the drain contacts and the gates are omitted.

The injected hole current I_h^{trig} necessary for triggering latch-up reduces only by a factor of approximately 2.5 when the doping concentration in the epitaxial layer is reduced from $\approx 10^{15}$ cm^{-3} to 5×10^{13} cm^{-3}. The latch-up immunity, therefore, is not substantially reduced when the epitaxial layer doping concentration is lowered to integrate fast PIN photodiodes. Design measures such as guard rings around wells and a reduced source/drain-contact to well-contact distance(14) can easily be applied to obtain PIN-CMOS-OEICs with high latch-up immunity. The change in C_e was shown not to influence the latch-up immunity of OEICs on n-type substrate. The die area increases only slightly due to latch-up precautions. Fast PIN photodiodes, therefore, can be easily integrated in analog full custom OEICs or optoelectronic application specific integrated circuits (OPTO-ASICs).

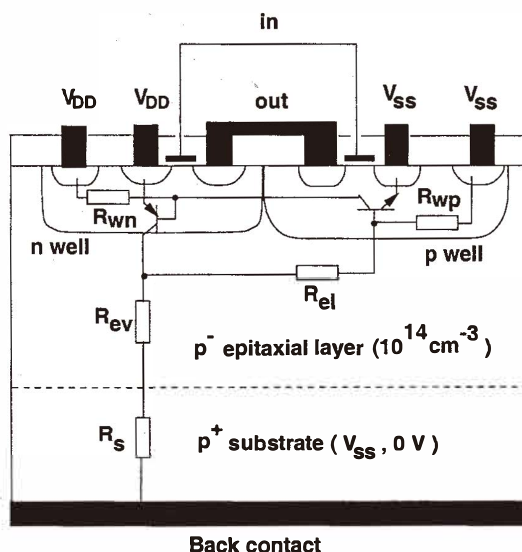

Fig. 10. Parasitic bipolar transistors in a CMOS cross section resulting in a thyristor structure.

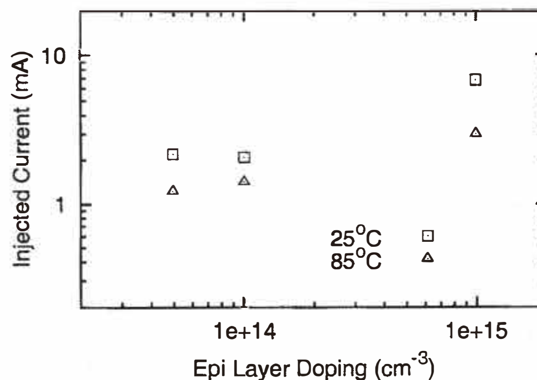

Fig. 11. Injected hole current necessary for triggering latch-up.

Another effect necessary to evaluate is reach-through between neighboring analog wells of doping type complimentary to the substrate. A reduction of C_e causes wider space-charge regions around the wells. Therefore, the specified minimum distance of analog wells on different potentials has to be increased to avoid reach-through currents between neighboring wells. Reach-through currents can change operating points of analog circuits and should be avoided, in particular, when bias currents are low. An increased minimum distance between analog n wells to avoid reach-through increases the active die area of optical receiver chips only slightly.

Latch-up immunity and reach-through certainly exclude the implementation of circuit modules from libraries. These effects, however, can be dealt with successfully in the development of full custom OPTO ASICs.(15) The following results demonstrate that a reduction of C_e leads to an enormous improvement in the speed of integrated photodiodes and that special design measures for maintaining latch-up immunity and avoiding reach-through in full custom OPTO ASICs are justified.

Rise and fall times of 0.39 and 0.63 ns, respectively, were determined with the oscilloscope for the PIN photodiodes with $C_e = 5 \times 10^{13}$ cm^{-3} and a thickness of the epitaxial layer of 10 μm at a reverse bias of 3.0 V (Fig. 12) leading to values of 0.23 and 0.36 ns after correction for the laser and picoprobe rise and fall times. These values enable operation of the PIN photodiodes at a data rate of 1.1 Gb/s. With an antireflection coating (ARC), a quantum efficiency of 94 % is obtained for $\lambda = 638$ nm.(9)

3.5 *Results for PIN photodiodes on n-type substrate*

In the PIN photodiode shown in Fig. 9, the photogenerated holes drift downwards to the p^+ substrate, whereas the electrons drift the shorter distance upwards to the Si surface because of the exponential dependence of photogeneration. The drift times and, therefore, the rise and fall times can be reduced when the electrons with a higher mobility μ_n than the hole mobility μ_p have to drift the longer distance towards the substrate. This is of course possible in a PIN photodiode integrated in an OEIC on n^+/n^-substrate. Such a photodiode has already been characterized.(16) The photodiode protection mask was implemented in the CMOS flow chart to block out an originally unmasked p-type threshold implantation from the photodiode area. Rise and fall times of 0.19 and 0.24 ns, respectively, were obtained for a PIN photodiode with an n-type doping level $C_e = 2 \times 10^{13}$ cm^{-3} on a highly doped n^+ substrate for a reverse bias of 3.0 V. From these rise and fall times a bandwidth of 1.7 GHz and a data rate of 1.5 Gb/s were estimated. The 1.7 GHz bandwidth of the PIN photodiode with $C_e = 2 \times 10^{13}$ cm^{-3} is increased tremendously compared to the value of 20 MHz measured for the standard doping concentration of the epitaxial layer $C_e \approx 10^{15}$ cm^{-3}.

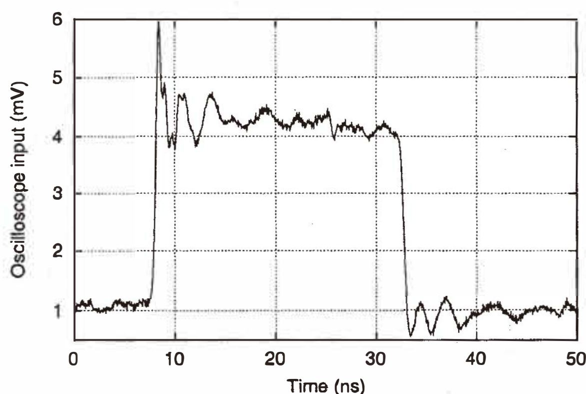

Fig. 12. Transient response of CMOS-integrated PIN photodiode.

The quantum efficiency has been increased from about 50% to values larger than 90 % for the red region of the spectrum by an antireflection coating (ARC) consisting of a thin silicon dioxide and a thin silicon nitride layer.[13] In the wavelength region from 500 to 900 nm, quantum efficiencies larger than 80 % can be achieved according to optical simulations using MEDICI-optical device advanced application module (ODAAM). It should be mentioned that ARC requires at least one additional mask.

3.6 *PIN CMOS OEIC for data communication*

A CMOS photoreceiver circuit on an n-type substrate which contains a monolithically integrated vertical PIN photodiode and which combines a data rate of 622 Mb/s with a quantum efficiency of 94 % is shown in Fig. 13.[16] It is a typical high-frequency amplifier. Only n-channel MOSFETs are used to obtain a high bandwidth.

The transistors M1–M4 are used in a transimpedance input stage, which converts the photocurrent change in the integrated PIN photodiode to a voltage change. Two further stages with identically dimensioned transistors provide an additional voltage gain. The cascade transistors M1, M5 and M9 reduce the Miller effect and correspondingly increase the bandwidth. The source followers M3, M7 and M11 as well as the current sources M4, M8 and M12 are used for level shifting. The threshold voltage of transistors M3, M7 and M11 has been reduced intentionally to approximately 0.4 V by the photodiode protection mask to obtain lower V_{GS} values. Polysilicon resistors were implemented as load elements, since depletion transistors were not available in the digital CMOS process used. Due to feedback across the 2-kΩ resistor R_{fb} and to the identical dimensions of the transistors in the different stages, a good independence from process deviations within the relatively large specified process tolerances of the digital CMOS process has been achieved. Three identical biasing circuits with UB1 = UB2 = UB3 were used instead of one to minimize parasitic coupling between the stages. The preamplifier OEIC was fabricated by 1.0-μm

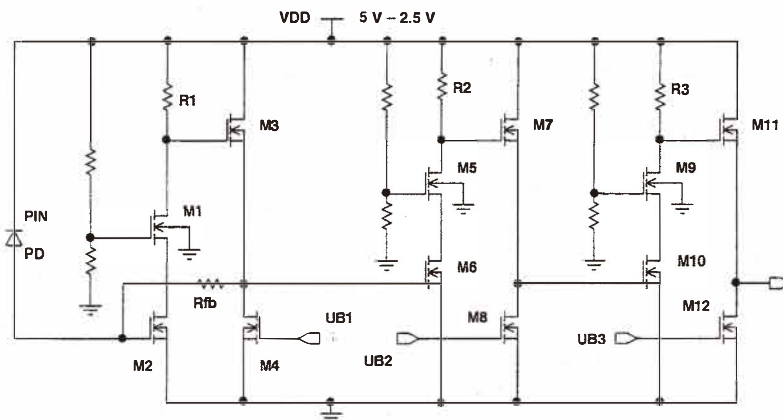

Fig. 13. Circuit diagram of a CMOS preamplifier OEIC for application in a fiber and interconnect receiver.

CMOS technology. Its sensitivity was 4.7 mV/μW for $\lambda = 638$ nm, increasing to 9.0 mV/μW with ARC. Bit error measurements showed the sensitivity of –14 dBm necessary to achieve a bit error rate of 10^{-9} at an NRZ data rate of 622 Mb/s with $\lambda = 638$ nm. This sensitivity is much better than the value of –6.3 dBm reported for an OEIC in 0.35-μm CMOS technology.(17) The power consumption was 44 mW at 5.0 V reducing to 17 mW at 3.3 V and to less than 9 mW at 2.5 V.

The photodiode, surrounded by a metal shield, covers an area of approximately 150×150 μm^2. The preamplifier occupies an active area of less than 190×200 μm^2. Values of 0.53 ns and 0.69 ns for the rise and fall times, respectively, at the output of the preamplifier were found for a concentration of 2×10^{13} cm^{-3} in the epitaxial layer, where the depletion region spreads through the entire epitaxial layer already at a supply voltage of less than 3 V.

These values for the rise and fall times indicate that CMOS OEICs with a reduced doping concentration in the epitaxial layer having an appropriate output buffer can be used as receivers for optical data transmission via fibers or for optical interconnects on a board level up to a bit rate BR of 622 Mb/s in the NRZ mode, verified by a measured eye diagram with a pseudo-random bit sequence (PRBS) of 2^{23}–1 (Fig. 14).(16)

New measurements at a supply voltage of only 2.5 V also verified a data rate of 622 Mb/s.(18) The data rate of the OEIC was limited by the amplifier in 1.0-μm technology. With sub-micrometer PIN-CMOS-OEICs, however, data rates in excess of 1 Gb/s are easily possible. Work to achieve a 1-Gb/s receiver in 1.0-μm CMOS technology with another circuit topology is in progress.

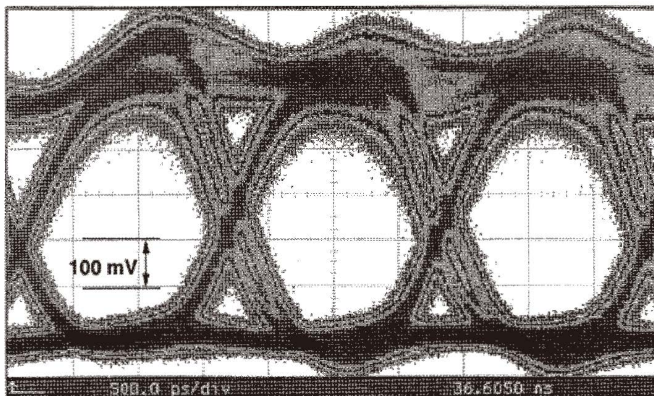

Fig. 14. Measured eye diagram of the CMOS preamplifier OEIC for application in a fiber and interconnect receiver ($\lambda = 638$ nm, time: 500 ps/div, amplitude: 0.1 V/div).

4. Discussion

It is worthwhile to compare the published results on silicon OEICs in Table 2.[19] A hybrid receiver-transmitter circuit containing a 0.8-μm CMOS amplifier and a flip-chip bonded GaAs-AlGaAs multi-quantum-well modulator, which also could be used as a PIN photodiode, has been reported to operate up to 625 Mb/s.[20] A SiGe OEIC with a PIN photodiode and heterojunction bipolar transistors in the amplifier achieved a bandwidth of 460 MHz corresponding to a bit rate of approximately 690 Mb/s with a photodiode bias of 9 V.[21] A lateral PIN photodiode was used in an NMOS receiver OEIC, which operated at a bit rate of 300 Mb/s [22] when biased at VDD = 8 V and with a very large photodiode bias V_{PD} = 30 V. In a redesigned version, the NMOS OEIC achieved a data rate of 1 Gb/s at a sensitivity of –9.3 dBm still requiring a photodiode bias of V_{PD} = 30 V.[23]

A data rate of 150 Mb/s was achieved with a bipolar OEIC using the BEST-process of AT&T with 1.5-μm design rules.[24,25] An n^+/p-substrate photodiode limited this data rate. Vertical PIN photodiodes have been integrated with SBC bipolar transistor technology.[5,6] The optical receivers described in these two articles demonstrated a data rate of 50 Mb/s[6] and a frequency response of 147 MHz[5] at a supply voltage of 5 V, although the PIN photodiodes showed bandwidths of ≈300 MHz at a bias of 3 V. The thin p^+/n-collector/n^+-buried collector PIN photodiode in 0.6-μm BiCMOS technology was used together with a MOS amplifier and a low responsivity of the photodiode was observed.[3,4] A double photodiode in standard 0.8-μm BiCMOS technology enabled a bit rate of the OEIC with a

Table 2
Comparison of silicon receiver OEICs (BR = bit rate; PR = photoreceiver; PD = photodiode;[1] with ARC).

Process (μm)	VDD (V)	λ (nm)	BR_{PR} (Mb/s)	V_{PD} (V)	BR_{PD} or f_{3dB}	R_{PD} (A/W)	η_{PD} (%)
0.8 CMOS-MQW[20]	5	850	625	2.5	-	0.5	75
Bipolar SiGe[21]	6	850	690	9	460 MHz	0.3[1)]	43[1)]
1.0 NMOS[22]	8	870	300	30	500 Mb/s	0.52[1)]	74[1)]
1.0 NMOS[23]	1.8	850	1000	30	1.0 Gb/s	0.54[1)]	80[1)]
1.5 Bipolar[24]	5	850	150	4.2	150 Mb/s	0.21	30
Bipolar[6]	5	780	50	3.0	300 MHz	0.35	56
Bipolar[5]	5	830	150	3.0	280 MHz	0.5[1)]	75[1)]
0.6 BiCMOS[3]	3.3	850	531	2.5	700 MHz	0.07	10
0.6 BiCMOS[4]	3.3	670	622	2.5	700 MHz	0.16	29
0.8 BiCMOS[11]	5	638	531	3.3	531 Mb/s	0.49	95[1)]
0.8 BiCMOS[9]	5	638	622	3.3	622 Mb/s	0.49	95[1)]
0.35 CMOS[17]	3.3	850	1000	10	1.0 Gb/s	0.04	5.9
0.25 CMOS SOI[26]	2.0	850	1500	1.5	1.0 GHz	0.4	59
1.0 p^+p^-CMOS[9]	5	638	-	3.0	1.1 Gb/s	0.48	94[1)]
1.0 n^+n^-CMOS[16]	5	638	622	3.0	1.7 GHz	0.25	49
1.0 n^+n^-CMOS[16]	3.3	638	622	1.8	1.4 GHz	0.48[1)]	94[1)]

bipolar amplifier in excess of 531 Mb/s.[11] With a reduced light-sensitive area of the double photodiode, a data rate of 622 Mb/s became possible.[9] A very low responsivity of 0.04 A/W corresponding to a quantum efficiency of only 5.9 % has been reported for the p^+/n-well photodiode of a 1 Gb/s OEIC in 0.35-μm CMOS technology.[17] The most sophisticated avalanche photodiode approach in SOI CMOS technology enabled the realization of an OEIC with a bandwidth of 1 GHz corresponding to a bit rate of approximately 1.5 Gb/s at a supply voltage of only 2 V.[26] In sum, a low responsivity has been present to achieve a high data rate in the investigations,[3,4,17,24] or a high voltage for the photodiode was needed,[21–23] or a high additional process complexity has been needed for the integration of fast and highly efficient photodiodes.[5,6] Even compared to sophisticated detectors,[17,26] the vertically integrated PIN photodiode[9,16] achieved the highest speed and the highest quantum efficiency with an antireflection coating. The CMOS-integrated vertical PIN photodiode shows the largest speed-responsivity product of all integrated silicon photodiodes reported thus far for which standard or near-standard processes have been used.

It can be concluded that with CMOS receiver OEICs, comparable or even better data rates were obtained than with bipolar OEICs.[5,6] In contrast to the integration of PIN photodiodes in bipolar circuits, the integration of vertical PIN photodiodes in CMOS circuits requires minimal additional process complexity. The vertical PIN photodiodes combine a high data rate and a high quantum efficiency already at a low reverse bias with a single power supply voltage for the OEIC. Low-cost PIN-CMOS receiver OEICs for optical data transmission and for optical interconnects on boards and between boards via optical backplanes seem feasible.

The double photodiode is a good candidate for the implementation in fast OEICs without additional process complexity when a CMOS or BiCMOS process with self-adjusting well technology has to be used. The double photodiode makes high-volume, low-cost OEICs for consumer applications possible.

5. Conclusion

High-speed photodiodes being available by standard CMOS and BiCMOS technologies with few or no modifications were described. CMOS-integrated PIN photodiodes for data rates up to 1.5 Gb/s and double photodiodes for a data rate of 622 Mb/s possess very high quantum efficiencies larger than 90% with antireflection coating. These outstanding properties make the DPD and the PIN photodiode appropriate for applications in high-speed integrated optical receivers, optical storage systems and high-speed integrated cameras and imagers.

The double photodiode has been applied in a BiCMOS OEIC for optical storage systems. This DPD BiCMOS OEIC combines a high bandwidth and a low output offset voltage with a high sensitivity. The CMOS-integrated PIN photodiode has been implemented in a receiver OEIC for optical short-range communication and optical interconnects. This PIN CMOS OEIC shows a high sensitivity. PIN CMOS OEICs in submicrometer technology for data rates in excess of 1 Gb/s are possible.

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References

1 E. Brass, U. Hilleringmann and K. Schumacher: IEEE J. Solid-State Circuits **29** (1994) 1006.
2 E. Fullin, G. Voirin, M. Chevroulet, A. Lagos and J.-M. Moret: IEDM Digest Technical Papers (IEEE, Piscataway, NJ, 1994) p. 527.
3 P. J.-W. Lim, A. Y. C. Tzeng, H. L. Chuang and S. A. S. Onge: Int. Solid-State Circuits Conference (IEEE, Piscataway, NJ, 1993) p. 96.
4 D. M. Kuchta, H. A. Ainspan, F. J. Canora and R. P. Schneider: IBM J. Res. Develop. **39** (1995) 63.
5 M. Kyomasu: IEEE Trans. Electron Devices **42** (1995) 1093.
6 M. Yamamoto, M. Kubo and K. Nakao: IEEE Trans. Electron Devices **42** (1995) 58.
7 K. J. Ebeling: Integrated Optoelectronics (Springer, Berlin, Heidelberg, 1993) Chap. 11.
8 V. Hurm, W. Benz, W. Bronner, T. Fink, G. Kaufel, K. Kohler, Z. Lao, M. Ludwig, B. Raynor, J. Rosenzweig, M. Schlechtweg and J. Windscheif: Electronics Letters **33** (1997) 624.
9 H. Zimmermann, K. Kieschnick, T. Heide and A. Ghazi: Proc. 29th European Solid-State Device Research Conference (Edition Frontieres, Neuilly, 1999) p. 332.
10 H. Zimmermann, K. Kieschnick, M. Heise and H. Pless: Electronics Letters **34** (1998) 1875.
11 K. Kieschnick, H. Zimmermann, H. Pless and P. Seegebrecht: Interconnects in VLSI Design, ed. H. Grabinski (Kluwer, Boston, 2000) p. 213.
12 H. Zimmermann, K. Kieschnick, M. Heise and H. Pless: Int. Solid-State Circuits Conference (IEEE, Piscataway, NJ, 1999) p. 384.
13 H. Zimmermann, A. Ghazi, T. Heide, R. Popp and R. Buchner: Proc. Electronic Components and Technology Conference (IEEE, Piscataway, NJ, 1999) p. 1030.
14 R. R. Troutman: Latch-up in CMOS Technology (Kluwer, Hingham, MA,1986) Chap. 6.
15 H. Zimmermann, T. Heide, A. Ghazi and P. Seegebrecht: Interconnects in VLSI Design, ed. H. Grabinski (Kluwer, Boston, 2000) p. 203.
16 H. Zimmermann, T. Heide and A. Ghazi: IEEE Photonics Technology Letters **11** (1999) 254.
17 T. K. Woodward and A. V. Krishnamoorthy: Electronics Letters **34** (1998) 1252.
18 K. Kieschnick, T. Heide, A. Ghazi, H. Zimmermann and P. Seegebrecht: Proc. 25th European Solid-State Circuits Conference (Edition Frontieres, Neuilly, 1999) p. 398.
19 H. Zimmermann: Integrated Silicon Optoelectronics (Springer, Heidelberg, 2000) Chap. 12.
20 A. L. Lentine, K. W. Goossen, J. A. Walker, J. E. Cunningham, W. Y. Jan, T. K. Woodward, A. V. Krishnamoorthy, B. J. Tseng, S. P. Hui, R. E. Leibenguth, L. M. F. Chirovsky, R. A. Novotny, D. B. Buchholz and R. L. Morrison: Electronics Letters **33** (1997) 894.

21 J.-S. Rieh, D. Klotzkin, O. Qasaimeh, L.-H. Lu, K. Yang, L. P. B. Katehi, P. Bhattacharya and E. T. Croke: IEEE Photonics Technology Letters **10** (1998) 415.
22 J. Qi, C. L. Schow, L. D. Garrett and J. C. Campbell: IEEE Photonics Technology Letters **9** (1997) 663.
23 C. L. Schow, J. D. Schaub, R. Li, J. Qi and J. C. Campbell: IEEE Photonics Technology Letters **11** (1999) 120.
24 H. H. Kim, R. G. Swartz, Y. Ota, T. K. Woodward, M. D. Feuer and W. L. Wilson: IEEE J. Lightwave Technology **12** (1994) 2114.
25 K. G. Moerschel, T. Y. Chiu, W. A. Possanza, K. S. Lau, R. G. Swartz, R. A. Mantz, T. Y. M. Liu, K. F. Lee, V. D. Archer, G. R. Hower, G. T. Mazsa, R. E. Carsia, J. A. Pavlo, M. P. Ling, J. L. Dolcin, F. M. Erceg, J. J. Egan, C. J. Fassl, J. T. Glick and M. A. Prozonic: Custom Integrated Circuits Conference 1990 (IEEE, Piscataway, NJ, 1990), p. 18. 3. 1.
26 T. Yoshida, Y. Ohtomo and M. Shimaya: IEDM Digest Technical Papers (IEEE, Piscataway, NJ, 1998) p. 29.