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Fabrication and Resistive Switching Characteristics of Sol–Gel-derived $SrBi_4Ti_4O_{15}$ Memory Devices

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In this study, $SrBi_4Ti_4O_{15}$ (SBT) thin films were deposited on TiN/Si substrates by the sol–gel method, forming a metal–insulator–metal (MIM)-structured resistive random access memory (RRAM) device. Subsequently, rapid thermal annealing (RTA) was employed to improve the crystallinity and repair surface defects through lattice reorganization. An aluminum (Al) top electrode was then deposited by physical vapor deposition (PVD) to complete the MIM structure. The surface morphology of the SBT insulating layer was characterized using a field-emission scanning electron microscopy (FE-SEM) system, while the current–voltage (I–V) characteristics were measured using a precision source/measure unit (Keysight B2902A) to investigate the resistive switching behavior and underlying carrier transport mechanisms.

1. Introduction

With the rapid advancement of technology, semiconductor manufacturing processes have continuously evolved to meet the demand for smaller, lighter, and more portable devices with enhanced performance. As device performance requirements increase, memory capacity must also scale accordingly. Memory devices are widely used in personal computers, mobile devices, and various other applications. Memory can be broadly classified into two categories: volatile memory and nonvolatile memory. Volatile memory requires a continuous power supply to retain stored data; once power is removed, all stored information is lost. Common types include dynamic random-access memory (DRAM)(1) and static random-access memory (SRAM).(2) In contrast, nonvolatile memory retains data even without a power supply and allows data retrieval once power is restored. Currently, flash memory(3–5) is the dominant form of nonvolatile storage. With the proliferation of modern electronic devices and the growing demand for low-power components, nonvolatile memory technologies have become an inevitable trend.

Resistive random access memory (RRAM) is regarded as a promising candidate for next-generation nonvolatile memory owing to its simple metal–insulator–metal (MIM) structure, fast

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switching, and CMOS-compatible fabrication. In many oxide-based RRAM systems, defect redistribution and oxygen-vacancy-induced conductive filaments dominate switching behavior. Perovskite and complex-oxide materials have attracted particular interest because of their high permittivity, switchable polarization, and potential for stable bipolar switching.

Among them, bismuth layer–structured ferroelectrics (BLSFs) such as $SrBi_2Ta_2O_9$, $Bi_4Ti_3O_{12}$, and $SrBi_4Ti_4O_{15}$ (SBTi) are valued for their high Curie temperature, fatigue resistance, and anisotropic ferroelectricity. Early studies confirmed that SBTi thin films prepared by sol–gel or spin-on processes exhibit good ferroelectricity and a stable microstructure. The sol–gel route is particularly attractive because it enables excellent stoichiometry control, uniform coating, and relatively low processing temperatures suitable for silicon integration.[6–15]

Recent work on BLSF-based resistive switching, including $Bi_4Ti_3O_{12}$ and $CaBi_4Ti_4O_{15}$, has demonstrated that layered Aurivillius oxides can serve as effective RRAM active layers, with switching governed by oxygen vacancies and filamentary conduction. However, despite extensive studies on the ferroelectric and dielectric behaviors of SBTi films and ceramics, reports on SBTi-based RRAM—especially films prepared by low-cost sol–gel methods—remain limited and fragmented. Preliminary studies indicate that annealing temperature and post-treatments significantly affect SBTi leakage current, switching ratio, dielectric constant, and polarization behavior.[6–18]

Therefore, in this work, we investigate the fabrication and resistive switching characteristics of sol–gel-derived $SrBi_4Ti_4O_{15}$ thin films. We examine how processing and annealing conditions affect crystallization, morphology, electrical response, and resistive switching behavior, aiming to clarify the conduction mechanism and establish SBTi as a viable lead-free BLSF material for future nonvolatile memory applications.

2. Experimental Details

In this study, strontium bismuth titanate (SBT) precursor solution was synthesized by the sol–gel method, using TiN/Si substrates as the base material. The insulating layer was deposited by spin coating, followed by thermal treatments at different annealing temperatures. Finally, the top electrode was fabricated by thermal evaporation to complete the device structure. The chemical reagents used in this work were CH_3COOH (99.9%), $HOCH_2CH_2OH$ (99.3%), $Bi(NO_3)_3{\cdot}5H_2O$ (99.3%), $Sr(CH_3COO)_2$ (99.9%), $Ti\{OCH(CH_3)_2\}_4$ (97%), and $C_5H_8O_2$ (99%). The precursor solution was prepared by dissolving bismuth nitrate and strontium acetate in ethylene glycol and glacial acetic acid, respectively, in accordance with the stoichiometric ratio at room temperature. Acetylacetone, used as a stabilizing agent, was added dropwise into titanium isopropoxide, followed by heating and stirring until a homogeneous solution was obtained. The solution was then aged at room temperature for 24 h.

The aged solution was deposited on TiN/Si substrates by a spin coating first at 1000 rpm for 10 s and then at 3000 rpm for 25 s, followed by baking at 250 °C for 10 min. This process was repeated until the desired film thickness for RRAM applications was achieved. The coated films were annealed using a rapid thermal annealing (RTA) system at 400, 500, and 600 °C for 30 min to improve crystallinity, as summarized in Table 1. Subsequently, the top electrode was deposited by thermal evaporation, forming a MIM RRAM structure, as illustrated in Fig. 1.

Table 1
Parameters of the SBT thin film RRAM devices fabricated by RTA.

Working pressure	80 mTorr
Temperature	400, 500, 600 °C
Temperature rate	10 °C/s
Soak time	30 min

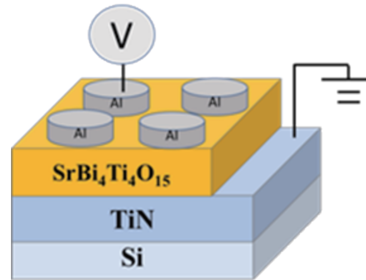

Fig. 1. (Color online) MIM structure of SBT film RRAM devices.

For characterization, a field-emission scanning electron microscopy (FE-SEM) system was employed to examine the surface morphology of the insulating layer, while a precision semiconductor parameter analyzer (B2902A) was used to measure the current–voltage (*I*–*V*) characteristics. The switching mechanisms were further analyzed on the basis of *I*–*V* measurements.

3. Results and Discussion

Figure 2 presents the surface morphologies of insulating layers prepared with different annealing temperatures. SEM observations reveal significant changes in microstructure after annealing. As shown in Fig. 2(a), the unannealed sample exhibits a smooth surface with no observable grain formation. Upon annealing at 400 °C [Fig. 2(b)], well-defined grains are clearly visible, indicating improved crystallinity. However, with higher annealing temperatures [Fig. 2(c)], the grains begin to merge and cracks appear on the film surface, suggesting structural degradation. These results indicate that 400 °C is the optimal annealing temperature for the SBT films.

For *I*–*V* resistive switching measurements, a positive bias was applied to the Al top electrode to induce the SET process, switching the $SrBi_4Ti_4O_{15}$ layer from a high-resistance state (HRS) to a low-resistance state (LRS) through the formation of conductive filaments. In the as-deposited sample, the forming voltage was approximately 2 V. To prevent permanent device breakdown during forming, a compliance current of 5 mA was applied with a maximum voltage of 10 V. Once formed, the device was switched back to the HRS by applying a negative bias (RESET), breaking the conductive filament. Subsequent cyclic sweeps between positive and negative biases allowed the determination of the RRAM window.

Figure 3 shows the *I*–*V* characteristics of samples prepared under different annealing conditions. The unannealed device exhibited no discernible memory window, likely owing to the amorphous nature of the insulating layer, leading to disordered filament formation. At 400 °C, a pronounced memory window of approximately one order of magnitude was observed.

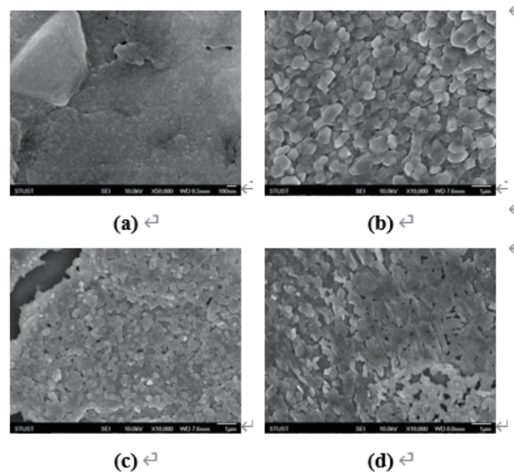

Fig. 2. SEM images of morphologies of SBT thin films prepared with different RTA temperatures: (a) no RTA, (b) 400, (c) 500, and (d) 600 °C.

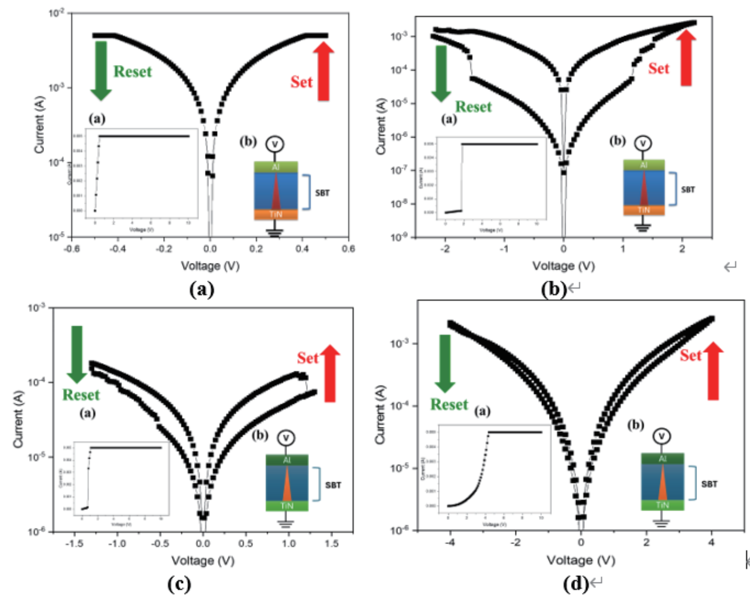

Fig. 3. (Color online) *I*–*V* curves of SBT thin films prepared with different RTA temperatures: (a) no RTA, (b) 400, (c) 500, and (d) 600 °C.

At 500 °C, the presence of an increased number of film defects led to a reduced memory window, indicating performance degradation. These findings confirm that 400 °C yields the most stable and well-defined *I*–*V* switching behavior.

To define the *I*–*V* curve fitting, we use the electrical conduction mechanism equation

$$J = qunE \exp\left[\frac{-(\Delta E_{ac})}{kT}\right], \tag{1}$$

where E_{ac} is the electron activation energy, q is the carrier mobility, E is the applied electrical field, n is the electronic concentration, k is the Boltzmann constant, and T is

absolute temperature. In addition, to calculate the $\ln\left(\frac{I}{T^2}\right)-\sqrt{V}$ curve, the hopping conduction mechanism equation was transformed to the *I*–*V* curve fitting for the RRAM devices. For the hopping conduction,

$$J = qN_a v_0 e^{-q\Phi_T/kT} e^{qaV/2dkT}, \tag{2}$$

where d, Φ_T, v_0, N, and a are the film thickness, the barrier height of hopping, the intrinsic vibration frequency, the density of space charge, and the mean hopping distance, respectively.(19–21)

Since the unannealed sample exhibited no memory window, conduction mechanism analysis was performed only for annealed devices. For the 400-°C-annealed device in Fig. 4, the linear fitting of Ln(*I*)–Ln(*V*) plots revealed an HRS slope of ~1 in the low-voltage region, indicating ohmic conduction. The LRS data exhibited linear fit in *V*–Ln(*I*) plots, consistent with hopping conduction. The conduction mechanism of the 500-°C-annealed device was similar: ohmic conduction in the low-voltage HRS and hopping conduction in the LRS. In the 600-°C-annealed device, both HRS and LRS followed hopping conduction, suggesting that excessive annealing induced a high density of defects in the insulating film, enabling carrier transport via trap-assisted hopping.

During the fabrication of the SBT switching layer in the RRAM device, imperfections within the lattice structure introduce defect states near the conduction and valence band edges. These defect states create additional energy levels that readily trap charge carriers during conduction.

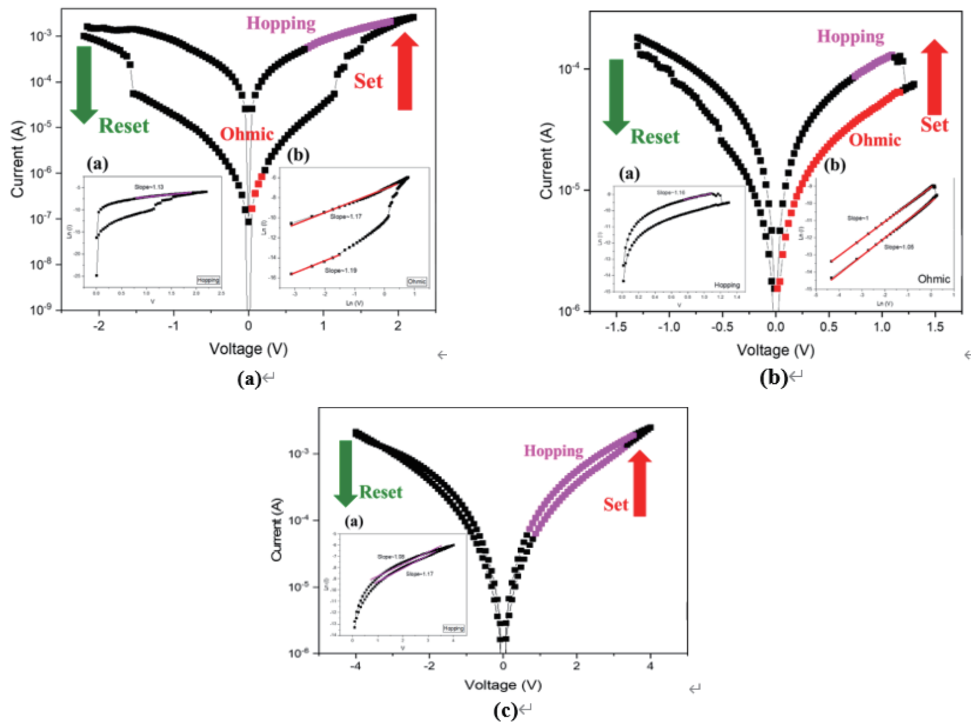

Fig. 4. (Color online) *I*–*V* curve fitting of SBT thin films with (a) 400, (b) 500, and (c) 600 °C RTA.

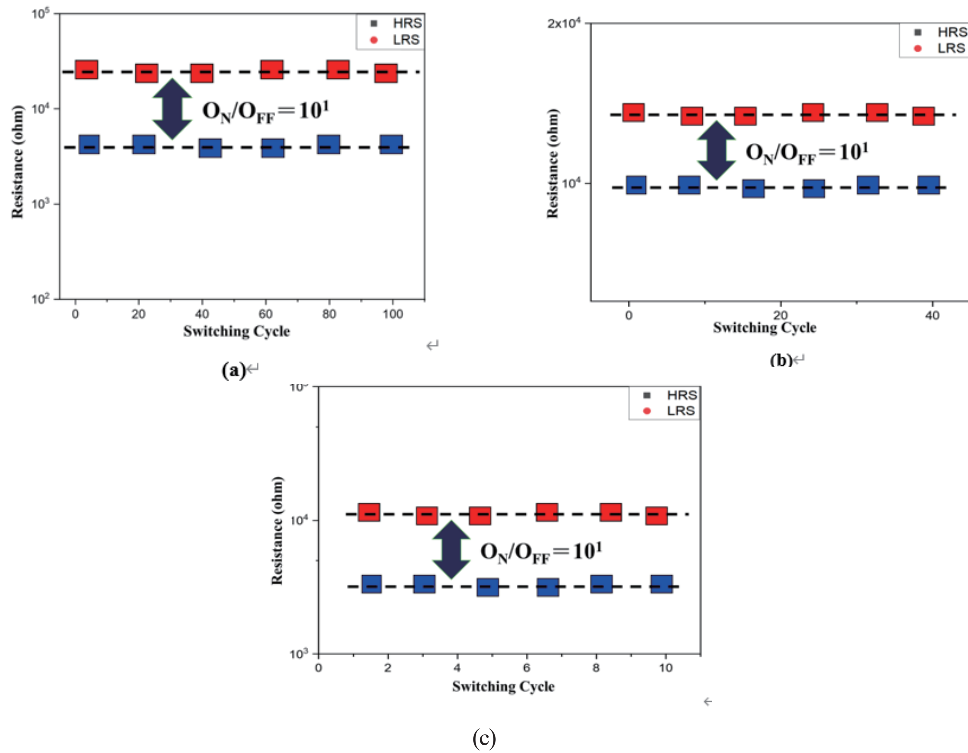

Fig. 5. (Color online) Switching cycle performance properties of SBT thin films with (a) 400, (b) 500, and (c) 600 °C RTA.

When an external electric field is applied or when thermal excitation occurs, the trapped carriers can acquire sufficient energy to overcome the energy barriers and transition into the conduction or valence band. This mechanism leads to carrier hopping and trapping behavior within the SBT switching layer, which significantly affects the resistive switching characteristics of the device.

To examine the switching cycle characteristics of SBT thin-film RRAM devices, Fig. 5 shows the endurance performance of Al/$SrBi_4Ti_4O_{15}$/TiN/Si RRAM devices prepared with different annealing temperatures. With annealing at 400–600 °C, the device maintained stable resistive switching for over 100 consecutive cycles, demonstrating excellent reliability. At high annealing temperatures, the increased defect density—consistent with SEM observations—led to reduced endurance and accelerated performance degradation.

5. Conclusions

In this study, SBT thin films were fabricated on TiN/Si substrates by sol–gel spin coating, followed by pyrolysis and crystallization to promote phase formation. After deposition, the films were subjected to RTA at various temperatures to evaluate the effects of thermal treatment on crystallinity, defect states, and electrical characteristics. Aluminum top electrodes were subsequently deposited by thermal evaporation to form a MIM structure, enabling the characterization of resistive switching behavior in the Al/SBT/TiN/Si RRAM device.

Systematic electrical testing revealed that the device annealed at 400 °C exhibited the most favorable performance among all samples. At this optimized temperature, the SBT switching layer presented improved crystallinity and a reduced concentration of oxygen-related defects,

leading to enhanced filament formation and rupture dynamics. The device required a forming voltage of approximately 2 V, followed by stable bipolar switching with an operating (SET/RESET) voltage near 2 V. The resulting on/off current ratio reached 2 at a read voltage of 0.1 V, while the leakage current level remained in the order of 10^{-5} A, indicating a relatively suppressed leakage pathway.

In addition, the Al/SBT/TiN/Si structure demonstrated reliable endurance, maintaining consistent resistive switching characteristics for up to 100 consecutive cycles. The reproducible switching window and stable current levels throughout cycling suggest that the defect-mediated conduction mechanism—primarily governed by oxygen vacancies and localized trap states—is effectively stabilized under the optimal RTA temperature. These results confirm that precise thermal processing is critical for tailoring the microstructure and electrical performance of sol–gel-derived SBT thin films for nonvolatile memory applications.

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