Sensors and Materials, Vol. 38, No. 11 (2026) 6455–6470
MYU Tokyo

S & M 4690

Effects of Oxygen Flow and Sputtering Parameters on the Bipolar Switching and Electrical Conduction Properties of Sm–SiO_2 Thin-film Resistive Random-access Memory Devices

Wen-Lung Lee,[1] Kai-Huang Chen,[2*] Ming-Cheng Kao,[3**] and Chien-Min Cheng[4]

[1]Section of Mathematics and Physics Science, Center for General Education, Air Force Academy, Kaohsiung 82047, Taiwan
[2]Department of Electronic Engineering, Cheng Shiu University. Kaohsiung 83347, Taiwan
[3]Graduate Institute of Aeronautics, Department of Information and Communication Engineering, Chaoyang University of Technology, Taichung 413310, Taiwan
[4]Department of Electronic Engineering, Southern Taiwan University of Science and Technology, Tainan, Taiwan

(Received March 12, 2026; accepted May 22, 2026)

Keywords: Sm–SiO_2, oxygen flow, resistive random-access memory, thin films, *I–V*

In this study, Sm cosputtered SiO_2 thin films were fabricated and systematically optimized for resistive random-access memory (RRAM) applications by controlling oxygen flow rate, Sm sputtering power, and sputtering time. The effects of deposition parameters on surface morphology, electrical switching behavior, endurance performance, retention characteristics, and conduction mechanisms were comprehensively investigated. Among the examined conditions, an oxygen flow rate of 6 sccm and a sputtering power of 20 W yielded the most uniform microstructure and stable bipolar switching performance. The optimized devices exhibited a clear distinction between high-resistance state (HRS) and low-resistance state (LRS), with a resistance ratio of approximately 10^3. Endurance measurements demonstrated stable switching behavior over multiple cycles, while retention tests confirmed reliable data storage exceeding 10^4 s without significant degradation. Ln(I)–Ln(V) analysis revealed that Ohmic conduction dominates in the LRS, whereas the HRS may transition to space-charge-limited current under high electric fields or nonoptimized deposition conditions. The results highlight the critical role of oxygen stoichiometry and sputtering parameters in regulating defect distribution and charge transport. This work provides a practical strategy for enhancing the stability and reliability of Sm-doped SiO_2-based RRAM devices for future nonvolatile memory applications.

1. Introduction

The rapid advancement of information and communication technologies has fundamentally reshaped modern society, enabling real-time access to global information without geographical constraints. Concurrently, electronic systems have undergone a dramatic evolution in form

*Corresponding author: e-mail: 5977@csu.edu.tw
**Corresponding author: e-mail: kmc@cyut.edu.tw
https://doi.org/10.18494/SAM6332

ISSN 0914-4935 © MYU K.K.

factor, transitioning from large, space-consuming platforms to compact, lightweight, and highly integrated mobile devices. This trend has imposed increasingly stringent requirements on core electronic components, particularly memory technologies, which must support aggressive scaling, low power consumption, high operating speed, and long-term reliability.

Memory devices are generally classified into volatile and nonvolatile types according to their data retention characteristics. Volatile memories, such as static and dynamic random access memories, offer high access speeds and endurance but lose stored data when power is removed. In contrast, nonvolatile memories preserve information without continuous power supply, enabling persistent data storage. Among commercially available nonvolatile memories, flash memory has dominated the market owing to its relatively mature fabrication technology and acceptable performance. However, conventional flash memory suffers from inherent limitations in scaling, endurance, and operation speed, primarily caused by charge-storage-based mechanisms and increasing tunnel oxide reliability concerns.

As device dimensions continue to shrink, further performance improvements in flash memory become increasingly challenging. These limitations have stimulated extensive research into emerging nonvolatile memory technologies capable of overcoming the physical and architectural constraints of charge-based storage. In recent years, several alternative memory concepts have been proposed, including magnetoresistive random access memory (MRAM), ferroelectric random access memory (FeRAM), phase-change random access memory (PCRAM), and resistive random access memory (RRAM). Each of these technologies exhibits distinct operating principles and performance trade-offs, yet none has fully satisfied the combined requirements of scalability, low power consumption, high speed, and fabrication simplicity.[1–3]

Among these candidates, RRAM has attracted considerable attention as a promising next-generation nonvolatile memory technology. RRAM typically employs a simple metal–insulator–metal (MIM) structure and operates on the basis of electrically induced resistance switching phenomena within the insulating layer. Compared with other emerging memory technologies, RRAM offers several key advantages, including high switching speed, low operating voltage, high scalability, small cell area, nondestructive readout, and long data retention. In addition, the compatibility of RRAM with complementary metal–oxide–semiconductor (CMOS) processes makes it particularly attractive for high-density integration and three-dimensional memory architectures.[1–6]

The resistive switching behavior in RRAM is commonly attributed to the formation and rupture of conductive filaments composed of defects such as oxygen vacancies or metallic ions within the dielectric layer. Although this filamentary switching mechanism enables low-power and high-speed operation, it also introduces challenges related to device variability, endurance degradation, and reliability. Consequently, extensive efforts have been devoted to material engineering, interface modification, and process optimization to improve the electrical stability and uniformity of RRAM devices. Sm–SiO_2 thin films are promising for RRAM owing to their tunable oxygen vacancy concentration, low leakage current, and excellent CMOS compatibility. Sm doping acts as a defect regulator, enabling the controlled formation and rupture of conductive

filaments, which improves switching uniformity and stability. The SiO_2 matrix provides a wide bandgap and strong insulating properties, ensuring reliable high-resistance states. Additionally, the balanced defect distribution enhances charge trapping and transport behavior. Overall, Sm–SiO_2 films offer stable resistive switching, good endurance, and high reliability, making them suitable for next-generation nonvolatile memory applications.[1–6]

From an application perspective, modern electronic systems—including smartphones, portable computing devices, digital cameras, and data storage units—demand memory technologies that support rapid data access, low energy consumption, and reliable long-term operation. The continuous growth of data-centric applications further amplifies the need for high-performance nonvolatile memories capable of sustaining repeated program/erase cycles without significant performance degradation. Therefore, understanding and improving the physical mechanisms governing resistive switching is critical for the practical deployment of RRAM technologies.[1–11]

In this work, resistive random access memory devices are systematically investigated to evaluate their electrical characteristics and switching performance. By optimizing device structure and material properties, in this study, we aim to address key challenges associated with resistive switching stability and reliability. The results are expected to provide valuable insights into the development of high-performance RRAM devices and to contribute to the advancement of next-generation nonvolatile memory technologies.[12–28]

2. Experimental Details

In this study, thin films were deposited on Si substrates by radio-frequency (rf) magnetron cosputtering using SiO_2 and Sm targets. Various deposition parameters were systematically adjusted to investigate their effects on film properties, including oxygen flow rate, sputtering power, and deposition time, with the objective of identifying the optimal sputtering conditions. After film deposition, an aluminum (Al) top electrode was deposited by thermal evaporation, forming a MIM device structure. To evaluate the effects of cosputtering conditions, the resulting films and devices were characterized by scanning electron microscopy (SEM), electrical measurements, current–voltage (I–V) analysis, leakage current mechanism evaluation, and endurance (cycling) measurement. The measured results were recorded and analyzed in detail to provide a comprehensive comparison of the electrical and structural characteristics under different deposition conditions.

To prepare the TiN/SiO_2/Si substrate, the 50 nm TiN film was prepared using a power of 80 W and an argon flow rate of 10 sccm. During sputtering, the argon (Ar) flow rate was maintained constant, whereas the oxygen (O_2) flow rate was varied to control the concentration of oxygen vacancies within the deposited films. Since oxygen vacancies are inevitably generated during sputtering, introducing controlled oxygen flow allows the partial compensation of these defects, thereby inducing distinct material and electrical properties. In this work, Ar and O_2 were used as the working gases, and O_2 flow rates of 4, 6, 10, and 16 sccm were employed to systematically investigate the corresponding effects on film characteristics and device performance in SiO_2

target (rf power = 120 W) and 10 sccm Ar flow rate. Additionally, the aluminum material was deposited as the electrode through evaporation to form a MIM structure, as shown in Fig. 1.

The surface morphology and microstructural characteristics of the Sm–SiO_2 thin films were characterized by field-emission scanning electron microscopy (FE-SEM, JEOL JSM-6701F). Cross-sectional SEM observations were performed when required to evaluate film thickness uniformity and interfacial integrity. Electrical characterization was carried out using a Keysight B2902A precision source/measurement unit (SMU). *I–V* measurements were conducted under both positive and negative voltage sweeps to investigate the resistive switching behavior, current compliance dependence, and dominant conduction mechanisms of the fabricated MIM devices.

Figure 2 presents the forming characteristics of the Sm–SiO_2 oxide film RRAM devices. An initial electroforming process is necessary to initiate the formation of conductive filaments within the Sm–SiO_2 dielectric layer under a sufficiently high electric field. This electroforming step was carried out by applying a voltage of approximately 6 V, which successfully established a stable conductive path through the film.

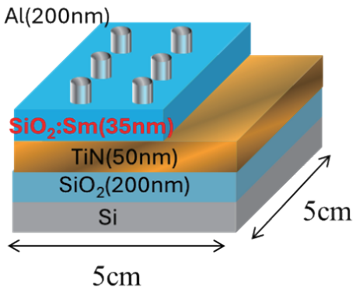

Fig. 1. (Color online) MIM structure of Sm–SiO_2 oxide film RRAM devices.

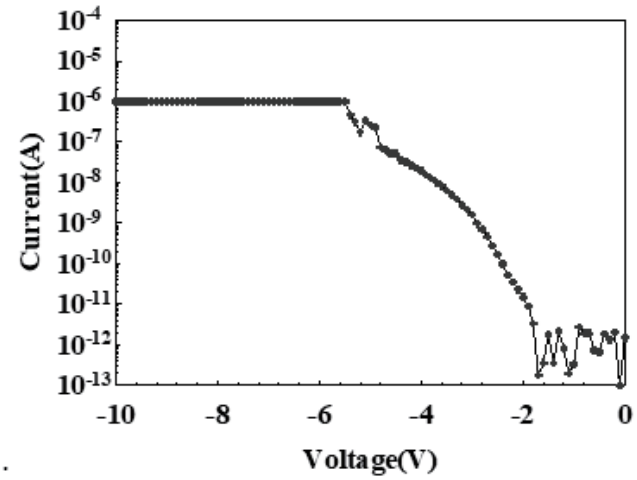

Fig. 2. Initial forming process of Sm–SiO_2 oxide film RRAM devices.

3. Results and Discussion

Figure 3 shows the SEM images of the films deposited under different oxygen flow rates: (a) 4, (b) 6, (c) 10, and (d) 16 sccm. As shown in the figure, when the oxygen flow rate is 4 sccm, the surface exhibits nonuniform grain sizes accompanied by densely packed grain clusters, indicating insufficient oxidation during film growth. At an oxygen flow rate of 6 sccm, the surface morphology is significantly improved. The grain size distribution becomes more uniform, the film surface appears smoother, and structural defects are less pronounced, suggesting that 6 sccm provides a more optimal oxygen environment for controlled crystallization and grain growth. When the oxygen flow rate increases to 10 sccm, the grains become notably larger, and distinct voids can be observed between adjacent grains. The surface becomes relatively rough, implying excessive grain growth and reduced film compactness. At 16 sccm, the excessive oxygen supply results in pronounced grain size nonuniformity and dense grain agglomeration. This condition leads to structural degradation and poor crystallinity.

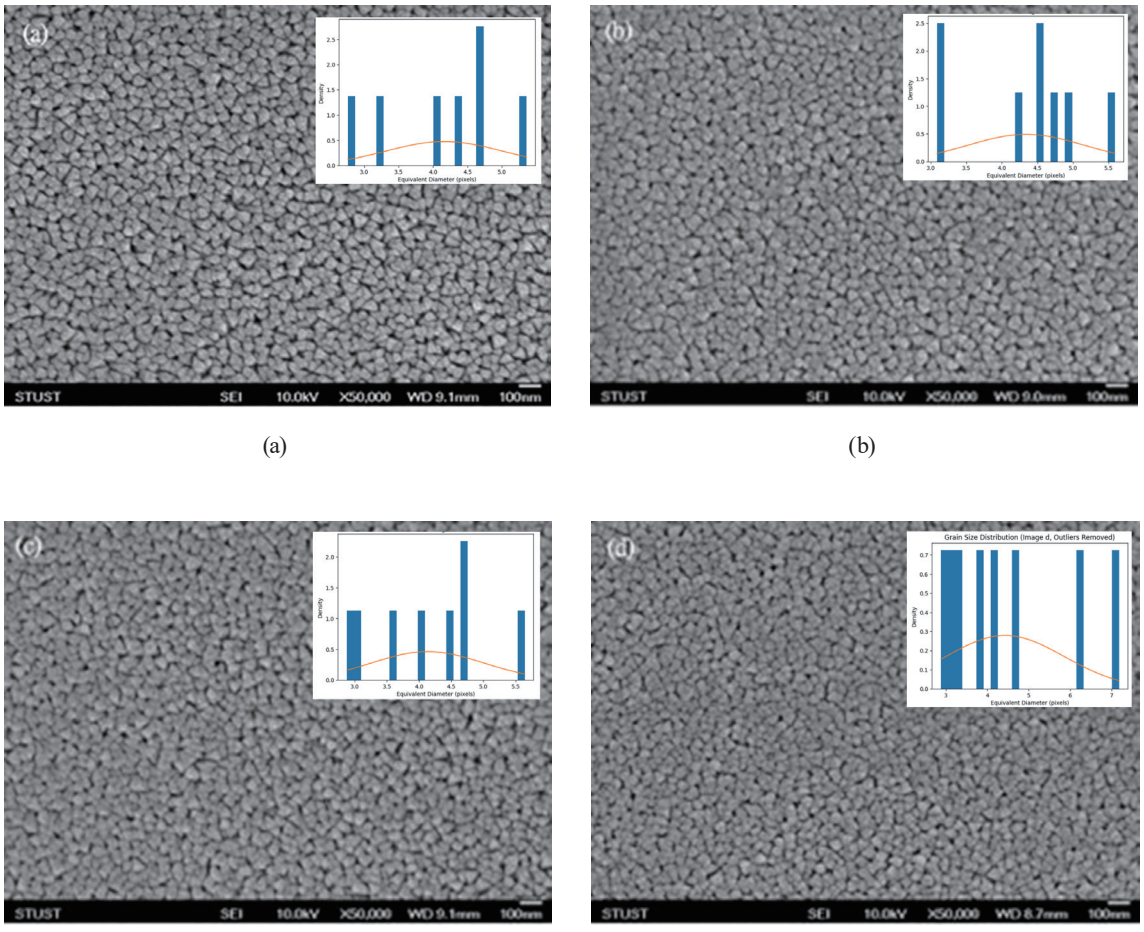

Fig. 3. (Color online) Surface morphology of Sm–SiO_2 oxide film RRAM devices for oxygen flow rates of (a) 4, (b) 6, (c) 10, and (d) 16 sccm.

Therefore, an oxygen flow rate of 16 sccm adversely affects the microstructural quality of the film.

According to a previous study, a Sm-doped colloidal SiO_2 composite material exhibited similar grain size to colloidal silica as seen from SEM images and size distribution curves.[28] The grain size distributions of samples in the insets of Figs. 3(a)–3(d) were analyzed from FE-SEM images using histogram plots with Gaussian fitting after outlier removal. All samples exhibit near-Gaussian distributions, indicating a consistent nucleation-dominated growth mechanism. Among them, sample (b) shows the narrowest distribution with the smallest standard deviation, suggesting superior grain uniformity and optimized film morphology. In contrast, sample (d) presents a broader distribution, implying nonuniform grain growth likely caused by grain coalescence or uneven nucleation. Samples (a) and (c) exhibit intermediate behavior with moderate dispersion. The results indicate that improved grain size uniformity plays a crucial role in enhancing microstructural quality. Such uniformity is expected to promote stable conductive filament formation, reduce leakage current, and improve the switching reliability of RRAM devices. These findings highlight the importance of controlling film growth conditions to achieve optimal device performance.[28]

Figure 4 shows the SEM images of the films deposited under different Sm sputtering powers: (a) 20, (b) 30, (c) 40, and (d) 50 W. When the 2 inch Sm target is operated at 20 W, the film exhibits a relatively uniform grain size distribution and a smooth surface morphology. Grain boundaries are well defined, and no significant structural defects are observed, indicating a stable and controlled deposition condition. At 30 W, although the sputtering power is increased by 10 W, no considerable morphological change is immediately apparent. However, notable differences in intergranular voids begin to emerge, and the grain size uniformity becomes slightly inferior to that at 20 W.

When the sputtering power is further increased to 40 W, the surface grains become significantly larger and exhibit irregular arrangements. The intergranular voids expand considerably, and the surface becomes rougher and less compact, suggesting excessive adatom mobility and accelerated grain growth. At 50 W, the higher sputtering power results in densely packed and stacked grains. Although the voids are not as pronounced as those observed at 40 W, the grain size distribution becomes highly nonuniform, even more evident than at 40 W. This indicates that excessive sputtering power deteriorates the microstructural homogeneity of the film.

The grain size distributions of samples in the insets of Figs. 4(a)–4(d) were analyzed from FE-SEM images using histogram plots with Gaussian fitting after outlier removal via the interquartile range (IQR) method. All samples exhibit well-defined Gaussian-like distributions, indicating a uniform nucleation-dominated growth mechanism. The narrow distributions and strong agreement with Gaussian fitting suggest suppressed grain coalescence and stable growth kinetics. Slight variations in mean grain size imply minor differences in nucleation density and growth conditions. Such uniform microstructures are beneficial for achieving consistent conductive filament formation, reduced leakage current, and improved switching reliability in resistive random-access memory (RRAM) devices. These results highlight the importance of controlling thin film growth parameters to optimize device performance.[28]

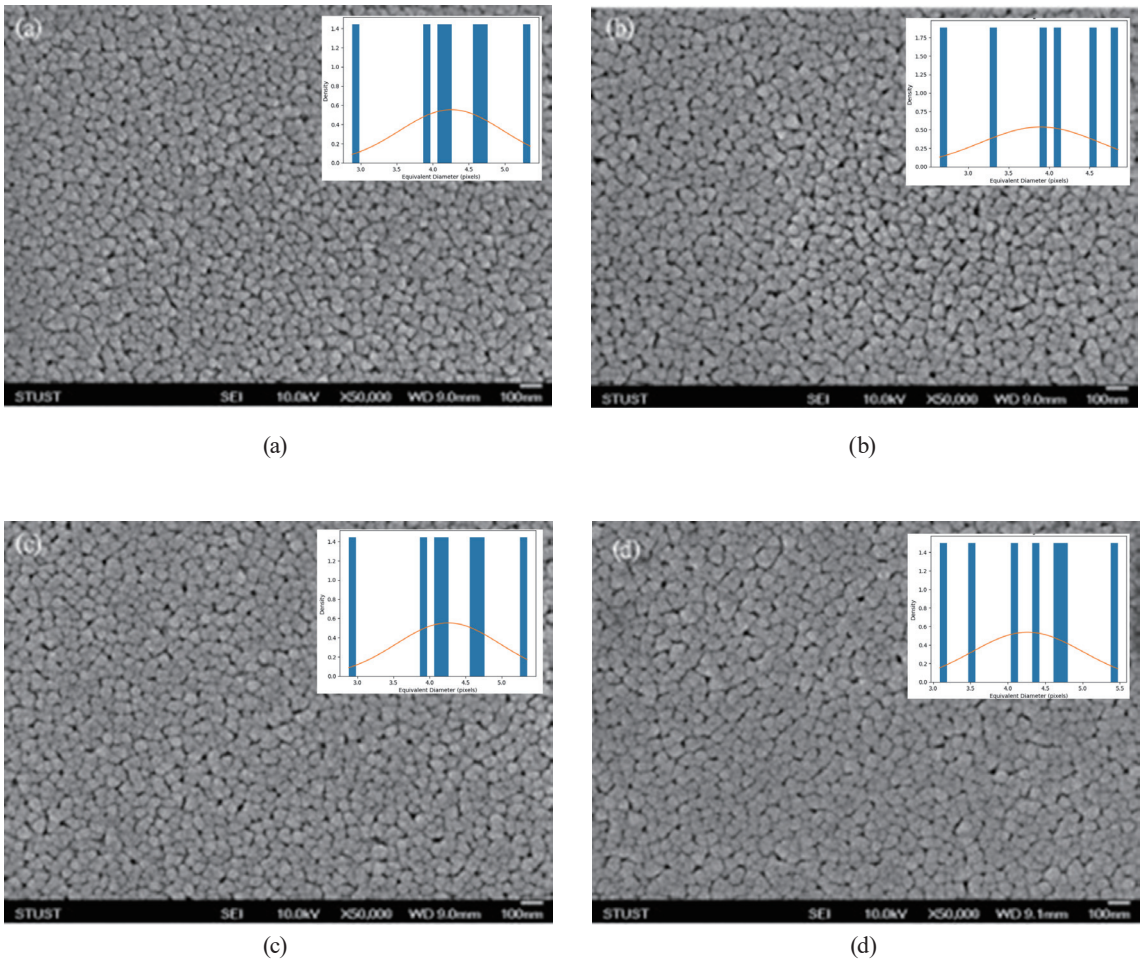

Fig. 4. (Color online) Surface morphology of Sm–SiO_2 oxide film RRAM devices for rf powers of (a) 20, (b) 30, (c) 40, and (d) 50 W.

While higher sputtering power typically enhances plasma energy and improves film density, excessively high power can lead to high-energy ion bombardment, causing structural damage and increased defect density. Furthermore, the resputtering effect and oxygen doping imbalance at high powers further exacerbate defect formation in Sm-SiO_2 films. These effects result in uneven grain growth and degraded electrical properties, as observed in our SEM and *I–V* testing results.[29]

During the SET operation, the device switches from the high-resistance state (HRS) to the low-resistance state (LRS) when a negative bias exceeding the SET threshold voltage is applied, indicating the formation or reconnection of conductive filaments. In contrast, during the RESET process, the application of a positive bias beyond the RESET voltage induces a transition from the LRS back to the HRS. This transition is associated with the partial rupture or dissolution of the conductive filament, resulting in a gradual decrease in operating current.

To assess the switching reliability and endurance performance, repetitive SET/RESET cycling tests were conducted for 100 consecutive cycles, as illustrated in Fig. 5(b). A current

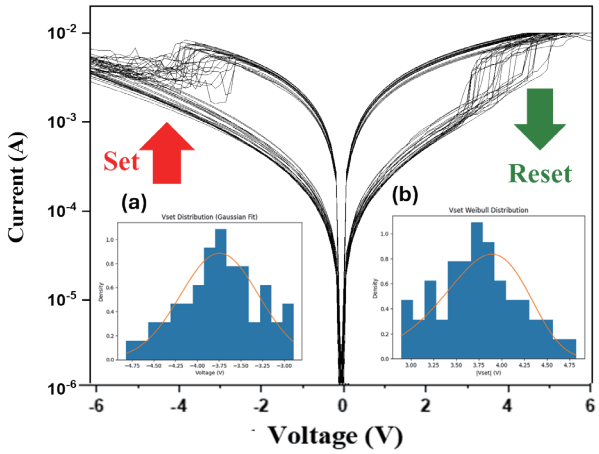

Fig. 5. (Color online) *I–V* curves of Sm–SiO_2 oxide film RRAM devices for (a) V_{set} distribution and (b) V_{set} Weibull distribution analyses.

compliance of 10 mA was applied during measurements to avoid irreversible dielectric breakdown. The extracted SET and RESET voltages were both approximately −0.5 V, demonstrating stable, repeatable, and well-defined bipolar resistive switching behavior in the Sm–SiO_2 oxide film RRAM devices.

The cycle-to-cycle variation of the switching parameters was analyzed using statistical and Weibull methods. The set voltage (V_{set}) shows a narrow Gaussian distribution centered at approximately −3.8 V, indicating good uniformity. Weibull analysis yields a high shape parameter (β is about 8.9), demonstrating excellent switching stability and low variability. The high β value suggests consistent conductive filament formation across switching cycles, with η of about 3.95 V representing the characteristic voltage. These results confirm reliable resistive switching behavior, attributed to the uniform microstructure and controlled defect distribution.

To further elucidate the SET-state transport behavior, the dominant electrical conduction mechanisms were systematically analyzed through *I–V* curve fitting for RRAM devices fabricated with neodymium oxide thin films under different oxygen contents. By correlating the oxygen concentration with the extracted slope values in the Ln(I)–Ln(V) plots, the underlying charge transport processes within the RRAM structure were identified and compared. In particular, the conduction behavior was interpreted on the basis of Ohmic conduction at low electric fields and space-charge-limited current (SCLC) at high electric fields. The corresponding transport equations for Ohmic and SCLC mechanisms are described as follows.[12–28]

The electrical current density of the ohmic conduction mechanism is determined using as

$$J = E_i \exp\left(\frac{-\Delta E_{ac}}{kT}\right), \tag{1}$$

where E_i is the electric field in the insulator, ΔE_{ac} is the electron activation energy, k is the Boltzmann constant, and T is the temperature.[12–28]

When the rate of electron injection from the electrode into the insulator exceeds the carrier

transport rate within the insulating layer, electrons accumulate inside the insulator. These excess carriers form residual charges within the bulk region, resulting in the formation of space charge. Under such conditions, the current becomes limited by the accumulated space charge, a phenomenon known as SCLC.[30]

When the injected carrier concentration exceeds the intrinsic or dopant concentration in the insulating layer, further carrier injection is restricted. The excess injected carriers contribute to additional space charge accumulation, which modifies the internal electric field distribution. Consequently, the current magnitude is significantly affected, and further carrier injection may be hindered, leading to nonlinear conduction behavior.

The SCLC current density can be expressed as

$$J = \frac{9\varepsilon_i \mu V^2}{8d^3}, \tag{2}$$

where J is the current density, ε_i is the dynamic dielectric constant of the insulating layer, μ is the carrier mobility, V is the applied voltage, and d is the thickness of the dielectric layer.[29]

Figure 6 presents the Ln(I)–Ln(V) plots of the conduction mechanisms for the films deposited under different oxygen flow rates: (a) 4, (b) 6, (c) 10, and (d) 16 sccm. The dominant conduction mechanisms were identified on the basis of the slope values extracted from the linear fitting regions. In Fig. 6(a), corresponding to 4 sccm, the Set process shows a slope of 1.015 in the LRS, indicating Ohmic conduction. In the HRS, slopes of 1.593 and 2.563 are observed, corresponding to Ohmic conduction and SCLC, respectively. During the Reset process, the LRS exhibits a slope of 1.003, consistent with Ohmic conduction. In the HRS, slopes of 1.560 and 2.635 suggest a transition from Ohmic conduction to SCLC behavior.

Under the 6 sccm condition shown in Fig. 6(b), the Set process exhibits a slope of 1.092 in the LRS, indicating Ohmic conduction. In the HRS, slopes of 1.002 and 1.266 are observed, both close to unity and consistent with Ohmic-dominated transport. During the Reset process, the LRS shows a slope of 1.0395, while the HRS exhibits slopes of 1.020 and 1.262. These values indicate that Ohmic conduction dominates in both resistance states under this oxygen flow condition. In Fig. 6(c), corresponding to 10 sccm, the Set process shows a slope of 1.007 in the LRS, confirming Ohmic conduction. In the HRS, slopes of 1.213 and 1.827 are obtained, suggesting a transition from Ohmic conduction to SCLC. During the Reset process, the LRS slope of 1.023 indicates Ohmic conduction, whereas the HRS slopes of 1.080 and 1.481 remain primarily within the Ohmic-dominated regime with partial deviation toward trap-controlled transport.

Under the 16 sccm condition shown in Fig. 6(d), the Set process exhibits a slope of 1.001 in the LRS, indicating Ohmic conduction. In the HRS, slopes of 1.442 and 1.447 suggest predominantly Ohmic behavior with slight deviation due to trap effects. During the Reset process, the LRS shows a slope of 1.002, consistent with Ohmic conduction, whereas the HRS exhibits slopes of 1.127 and 2.359, indicating a transition from Ohmic conduction to SCLC at higher electric fields. Overall, Ohmic conduction dominates the LRS under all oxygen flow

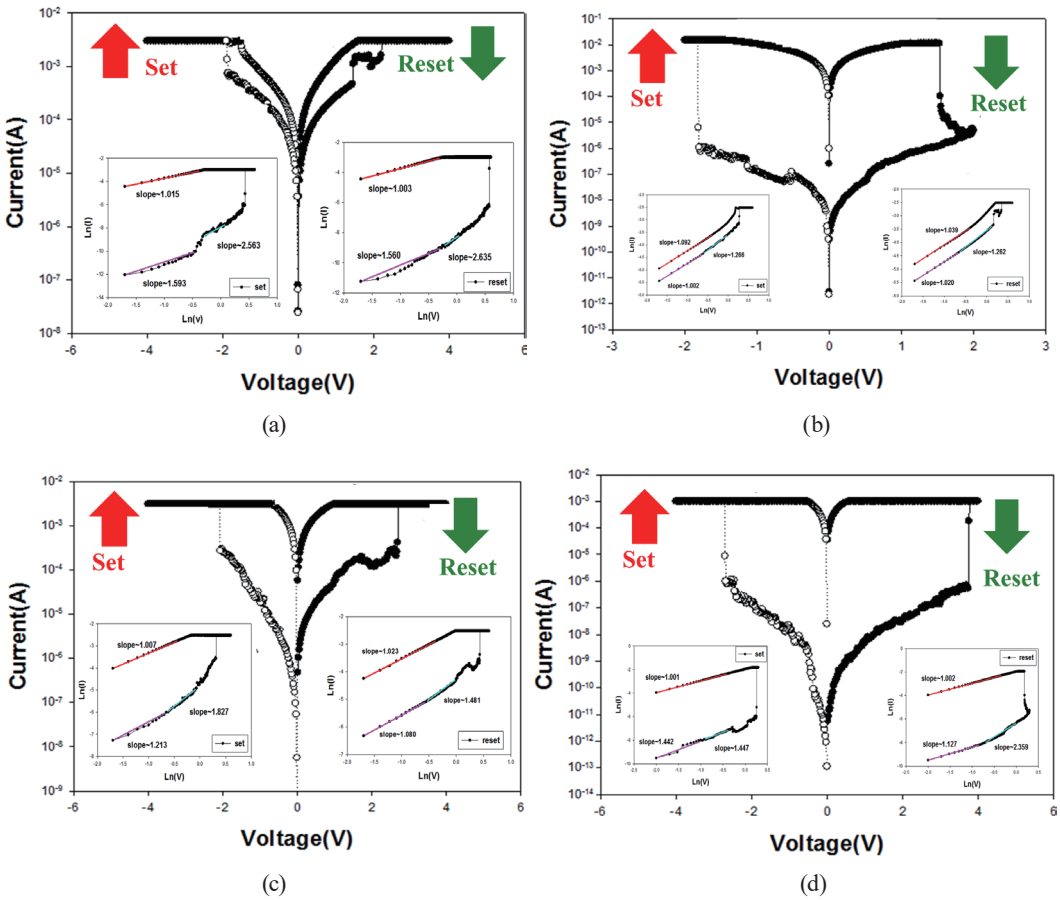

Fig. 6. (Color online) *I–V* curves and electrical conduction mechanism of SiO_2:Sm oxide film RRAM devices for oxygen flow rates of (a) 4,(b) 6, (c) 10, and (d) 16 sccm.

conditions, while the HRS exhibits mixed conduction behavior depending on the oxygen concentration, with SCLC becoming more pronounced at specific flow rates and bias regions.

The electrical properties of the devices are strongly affected by oxygen flow rate, which controls oxygen vacancy concentration and trap density. At a low flow rate (4 sccm), pronounced SCLC behavior indicates high defect density and trap-controlled transport. At a moderate flow rate (6 sccm), Ohmic conduction dominates, suggesting optimal defect balance and uniform carrier transport. Increasing the flow rate to 10 sccm introduces partial SCLC behavior due to nonuniform defect distribution. At a high flow rate (16 sccm), conduction is mainly Ohmic with slight trap effects. Overall, moderate oxygen flow ensures stable switching, while insufficient or excessive oxygen leads to trap-dominated conduction and reduced device reliability.

Figure 7 shows the *I–V* characteristics of the devices fabricated under different Sm sputtering powers: (a) 20, (b) 30, (c) 40, and (d) 50 W. In Fig. 7(a), corresponding to 20 W, a large memory window is clearly observed, and the HRS and LRS are clearly distinguishable. The SET transition occurs at approximately −1.8 V, where the device switches from the HRS to the LRS. The RESET process occurs at around +1.6 V, switching the device from the LRS back to the

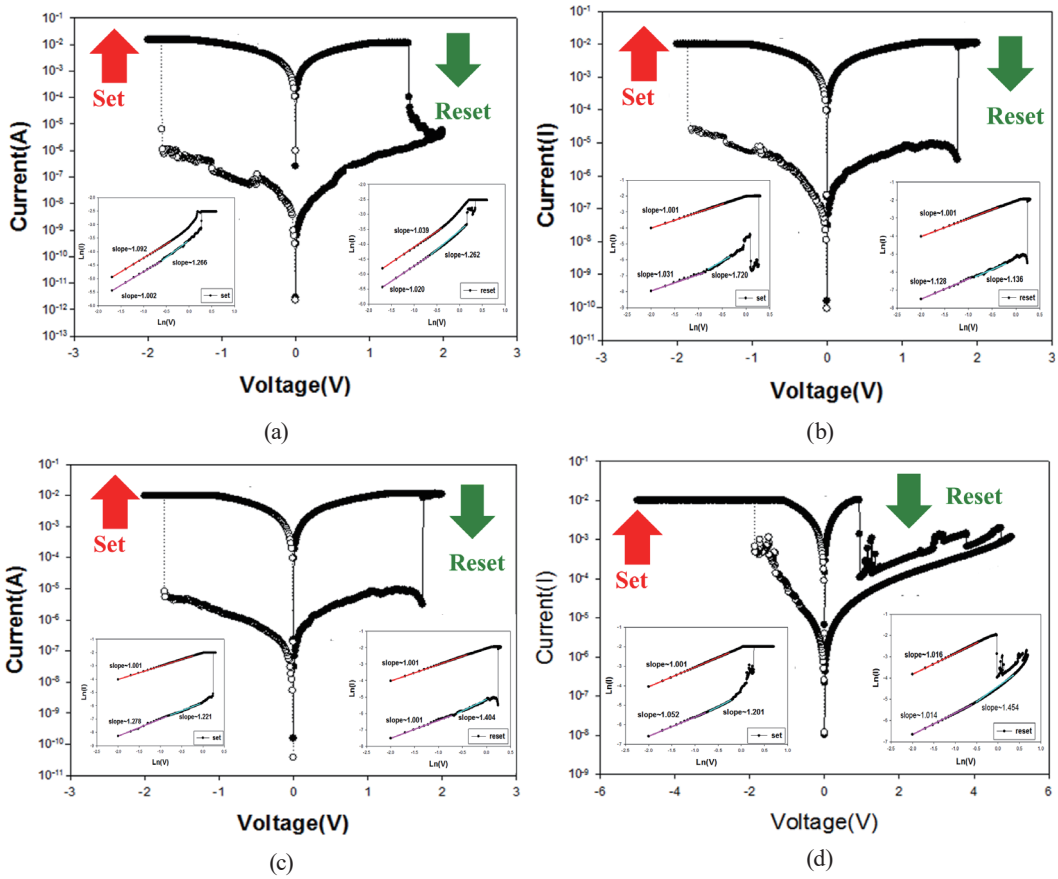

Fig. 7. (Color online) *I–V* curves and electrical conduction mechanism of SiO_2:Sm oxide film RRAM devices for rf powers of (a) 20, (b) 30, (c) 40, and (d) 50 W.

HRS. The bipolar switching behavior is well defined, with transitions from the negative SET bias to the positive RESET bias completing the *I–V* cycle.

Figure 7(b), corresponding to 30 W, also exhibits a relatively large memory window on both positive and negative bias sides, and the HRS and LRS remain distinguishable. However, the SET process shows instability, with a current interruption around −1.2 V before the device switches from the HRS to the LRS at approximately −1.9 V. During the RESET process, switching occurs near +1.8 V. Nevertheless, a notable discontinuity is observed in the right-side RESET branch, reducing the reliability of this parameter. For the 40 W condition shown in Fig. 7(c), the memory window initially appears significant on both bias polarities, with SET and RESET voltages occurring at approximately −1.8 and +1.8 V, respectively. However, as the number of switching cycles increases, the memory window gradually shrinks and the switching stability deteriorates. Therefore, this parameter was not considered suitable for further study.

In Fig. 7(d), corresponding to 50 W, the memory characteristics are inferior to the other three conditions, likely due to excessive sputtering power. The SET transition occurs at approximately −2.0 V, whereas the RESET process occurs near +0.5 V. However, the memory window is relatively small, and the number of stable switching cycles is limited, making this condition

unsuitable for further optimization. Among the four sputtering powers investigated, 20 W requires relatively low operating voltages while maintaining a large and stable memory window with good endurance performance. Although 30 and 40 W exhibit comparable initial memory windows, they lack the switching continuity and endurance observed at 20 W. 50 W shows both a reduced memory window and poor cycling stability. Therefore, 20 W was selected as the optimal sputtering power for subsequent experiments.

The electrical performance of the devices is strongly dependent on sputtering power. At 20 W, a large memory window and stable switching behavior are achieved, indicating uniform defect distribution and reliable filament formation. Increasing the power to 30–40 W introduces switching instability and discontinuity, suggesting nonuniform conductive paths due to increased defect density. At 50 W, the memory window significantly degrades, and cycling stability deteriorates, likely caused by excessive defect formation and structural disorder. Overall, the optimal sputtering power (20 W) ensures balanced defect density and stable conduction, while excessive power leads to trap-dominated transport and reduced device reliability.

Figure 8 presents the Ln(I)–Ln(V) plots for the films deposited under different sputtering times: (a) 10, (b) 20, (c) 30, and (d) 40 min. The thicknesses of the films were about 220 ± 5, 243 ± 5, 285 ± 5, and 322 ± 5 nm for the different sputtering times, respectively. The dominant conduction mechanisms were determined from the slope values obtained by linear fitting. In Fig. 8(a), corresponding to a sputtering time of 10 min, the Set process exhibits a slope of 1.092 in the LRS, indicating Ohmic conduction. In the HRS, slopes of 1.002 and 1.266 are observed, both close to unity and consistent with Ohmic-dominated transport. During the Reset process, the LRS slope is 1.039, whereas the HRS slopes are 1.020 and 1.262, confirming that Ohmic conduction dominates under this condition. Under the 20 min condition shown in Fig. 8(b), the Set process shows a slope of 1.002 in the LRS, indicating Ohmic conduction. In the HRS, slopes of 1.001 and 1.262 remain close to unity. During the Reset process, the LRS slope is 1.013, and the HRS slopes are 1.024 and 1.411, suggesting primarily Ohmic conduction with slight deviation due to trap-assisted transport.

In Fig. 8(c), corresponding to 30 min, the Set process exhibits a slope of 1.037 in the LRS, consistent with Ohmic conduction. The HRS slopes of 1.007 and 1.128 further confirm Ohmic-dominated behavior. During the Reset process, the LRS slope is 1.004, and the HRS slopes of 1.002 and 1.337 indicate that Ohmic conduction remains the primary transport mechanism. However, under the 40 min condition shown in Fig. 8(d), the conduction mechanism changes significantly. During the Set process, the LRS slope increases to 1.558, indicating the onset of SCLC. In the HRS, slopes of 1.603 and 2.231 further confirm SCLC-dominated behavior. During the Reset process, the LRS slope of 1.042 indicates Ohmic conduction, whereas the HRS slopes of 1.450 and 2.656 reveal a transition from Ohmic conduction to SCLC at higher electric fields. Overall, the films deposited for 10–30 min exhibit predominantly Ohmic conduction in both resistance states, while extended sputtering time (40 min) promotes SCLC behavior, suggesting increased trap density or thickness-induced space charge effects.

The electrical properties of the devices are strongly dependent on sputtering time, which affects film thickness and defect density. For deposition times of 10–30 min, the Ln(I)–Ln(V)

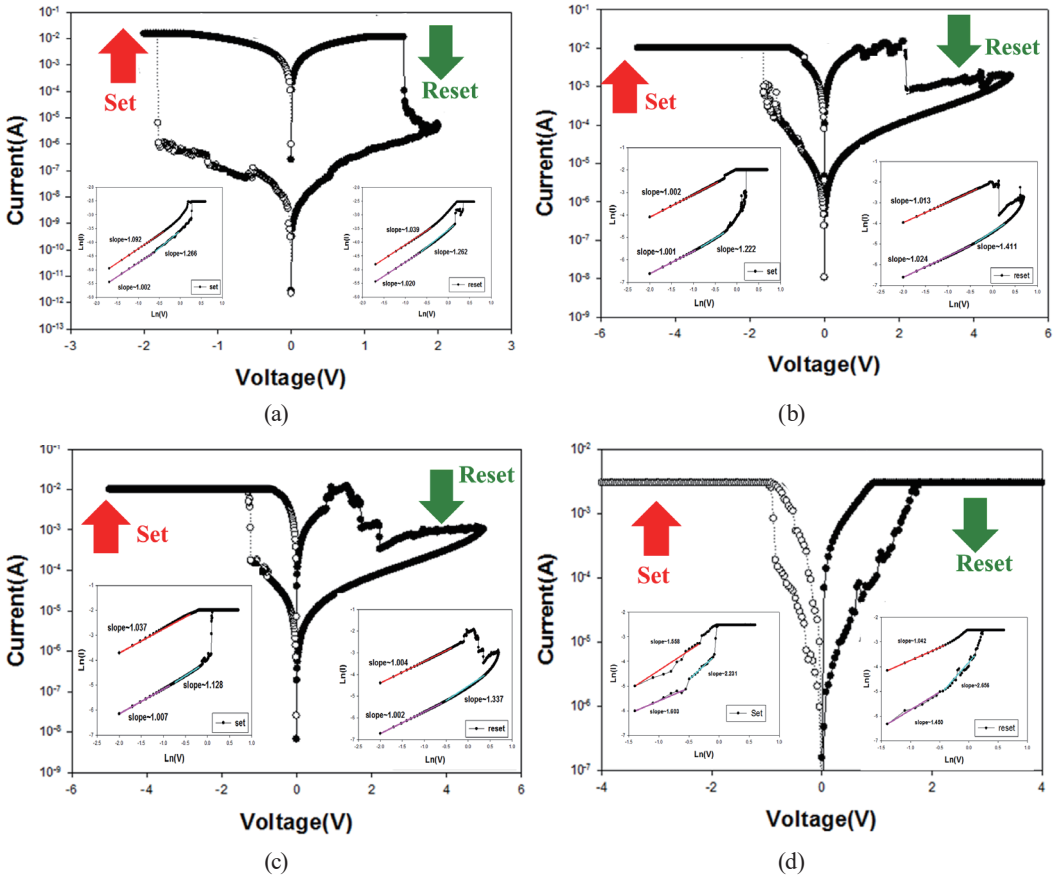

Fig. 8. (Color online) *I–V* curves and electrical conduction mechanism of SiO_2:Sm oxide film RRAM devices for deposition times of (a) 10, (b) 20, (c) 30, and (d) 40 min.

slopes are close to unity in both LRS and HRS, indicating dominant Ohmic conduction. This suggests uniform carrier transport with low trap density and stable conductive paths, resulting in reliable switching behavior. At 40 min, the conduction mechanism transitions to SCLC, as indicated by slopes exceeding 1.5. This implies increased trap density and space charge effects owing to thicker films and defect accumulation, such as oxygen vacancies. Overall, moderate sputtering times provide uniform conduction and stable performance, while excessive deposition time leads to trap-dominated transport and increased switching variability in RRAM devices.

Figure 9(a) illustrates the resistance values of the fabricated RRAM devices as a function of the number of switching cycles. The HRS and LRS are clearly distinguishable throughout the measurement range. The device exhibits stable bipolar switching behavior, maintaining a consistent resistance window over repeated cycling. The HRS remains in the range of approximately 10^4–10^5 Ω, while the LRS is maintained around 10^2–10^3 Ω. The resulting resistance ratio ($R_{_HRS}/R_{_LRS}$) is approximately 10^3, indicating a well-defined and reliable memory window. Furthermore, the distribution of resistance values shows minimal fluctuation across the measured switching cycles, demonstrating excellent endurance performance and stable filament formation/rupture processes within the dielectric layer.

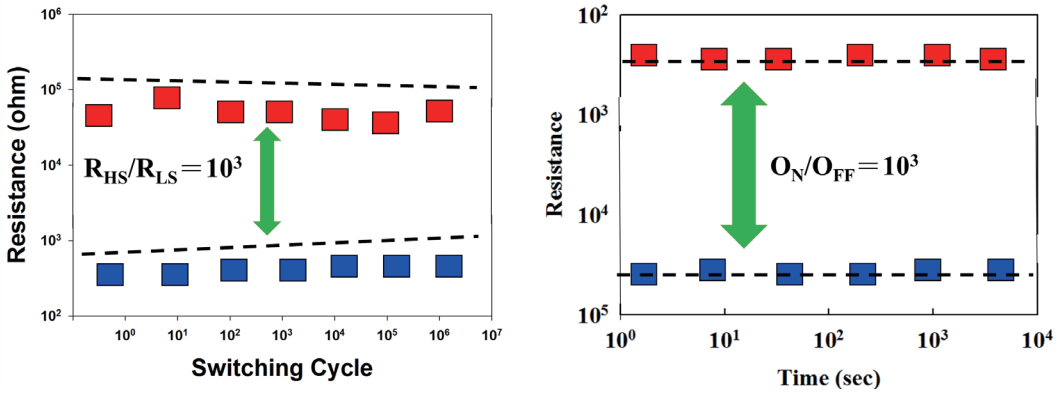

Fig. 9. (Color online) Resistance versus (a) switching cycle curves and (b) time of SiO_2:Sm oxide film RRAM devices for flow rate of 6 sccm power of 20 W, and deposition time of 10 min.

Figure 9(b) presents the retention characteristics of the RRAM device, showing resistance as a function of time. Both the HRS and the LRS remain well separated over the entire measurement period. The on/off ratio (R_{ON}/R_{OFF} or R_{HRS}/R_{LRS}) is maintained at approximately 10^3 without notable degradation. The resistance states exhibit negligible drift, confirming strong data retention capability. Extrapolation analysis suggests that the device can sustain stable memory behavior beyond 10^4 s. Overall, the results demonstrate that the optimized thin-film RRAM device exhibits excellent endurance stability and long-term retention reliability. The large and stable resistance ratio (10^3), combined with minimal resistance fluctuation during cycling and time-dependent measurements, confirms the robustness of the resistive switching mechanism and its suitability for nonvolatile memory applications.

4. Conclusions

In this study, the resistive switching characteristics of Sm-cosputtered SiO_2 thin films were systematically optimized by controlling oxygen flow rate, Sm sputtering power, and sputtering time. The results demonstrate that deposition parameters critically affect film morphology, defect distribution, and electrical performance. Among the investigated oxygen conditions, 6 sccm provided the most stable switching behavior, exhibiting a clear distinction between the HRS and the LRS, improved endurance, and predominantly Ohmic conduction with minimal SCLC contribution. Regarding sputtering power, 20 W yielded the most uniform surface morphology and the largest, most stable memory window with reliable bipolar switching and superior endurance performance. Higher sputtering powers (30–50 W) resulted in degraded microstructure, reduced switching stability, and limited cycle endurance due to excessive defect formation and grain nonuniformity.

Furthermore, sputtering time significantly affected the conduction mechanism. Films deposited for 10–30 min exhibited dominant Ohmic conduction in both resistance states,

indicating controlled carrier transport and stable trap distribution. However, at 40 min, the SCLC behavior became pronounced, suggesting increased trap density and thickness-induced space charge effects that degrade switching reliability. Overall, the optimized condition of 6 sccm oxygen flow, 20 W sputtering power, and moderate deposition time provides the best balance between structural uniformity and electrical performance, offering a reliable pathway for enhancing Sm-doped SiO_2-based RRAM devices.

Finally, in this study, we investigated the effects of oxygen flow rate and sputtering parameters on the microstructure and electrical properties of Sm–SiO_2 thin films. The bipolar resistive switching behavior and conduction mechanisms of RRAM devices were systematically analyzed. By the defect engineering of oxygen vacancies, the memory window, switching stability, and device reliability can be significantly improved. The proposed material and process demonstrate strong potential for integrated sensor and memory applications.

Acknowledgments

This work was performed at the National Science Council Core Facilities Laboratory for Nano-Science and Nano-Technology in the Kaohsiung-Pingtung area and was supported by the National Science Council of the Republic of China under Contract No. NSTC 113-2622-E-230-001.

References

1 L. Li, T. J. Dai, K. Liu, K. C. Chang, R. Zhang, X. Lin, H. J. Liu, Y. C. Lai, and T. P. Kuo: Nanoscale **13** (2021) 14035.
2 L. Li, K. C. Chang, R. Zhang, X. Lin, Y. C. Lai, and T. P. Kuo: Nanoscale **12** (2020) 15721.
3 L. Li, K. C. Chang, C. Ye, X. Lin, R. Zhang, Z. Xu, W. Xiong, Y. Zhou, and T. P. Kuo: Nanoscale **12** (2020) 3272.
4 K. C. Chang, T. J. Dai, L. Li, X. N. Lin, S. D. Zhang, Y. C. Lai, H. J. Liu, and Y. E. Syu: Nanoscale **12** (2020) 22070.
5 K. C. Chang, R. Zhang, T. C. Chang, T. M. Tsai, T. J. Chu, H. L. Chen, C. C. Shih, C. H. Pan, Y. T. Su, and P. J. Wu: Proc. IEEE Int. Electron Devices Meeting (IEDM) (2014) 33–34.
6 C. Ye, Z. Xu, K. C. Chang, L. Li, X. N. Lin, R. Zhang, Y. Zhou, W. Xiong, and T. P. Kuo: Nanoscale **11** (2019) 20792.
7 M. Lanza, R. Waser, D. Ielmini, J. J. Yang, L. Goux, J. Suñe, A. Kenyon, A. Mehonic, S. Spiga, and V. Rana: ACS Nano **15** (2021) 17214.
8 A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, and E. Eleftheriou: Nat. Nanotechnol. **15** (2020) 529.
9 A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, C. Funck, and S. Menzel: ACS Appl. Electron. Mater. **3** (2021) 3674.
10 T. Dalgaty, N. Castellani, C. Turck, K. E. Harabi, D. Querlioz, and E. Vianello: Nat. Electron. **4** (2021) 151.
11 M. Lanza, H. S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B. Regan, L. Larcher, M. Villena, J. Yang, and L. Goux: Adv. Electron. Mater. **5** (2019) 1800143.
12 K. H. Chen, C. M. Cheng, N. F. Wang, H. W. Hung, C. Y. Li, and S. Wu: Nanomaterials **13** (2023) 198.
13 T. M. Tsai, K. C. Chang, T. C. Chang, R. Zhang, T. Wang, C. H. Pan, K. H. Chen, H. M. Chen, M. C. Chen, and Y. T. Tseng: IEEE Electron Device Lett. **37** (2016) 408.
14 R. Zhang, T. F. Young, M. C. Chen, H. L. Chen, S. P. Liang, Y. E. Syu, S. M. Sze, K. C. Chang, T. C. Chang, and T. M. Tsai: IEEE Electron Device Lett. **35** (2014) 630.
15 C. Y. Lin, K. C. Chang, T. C. Chang, T. M. Tsai, C. H. Pan, R. Zhang, K. H. Liu, H. M. Chen, Y. T. Tseng, and Y. C. Hung: IEEE Electron Device Lett. **36** (2015) 564.
16 C. H. Jung, S. I. Woo, Y. S. Kim, and K. S. No: Thin Solid Films **519** (2001) 3291.

17 W. W. Zhuang, W. Pan, B. D. Ulrich, J. J. Lee, and L. Stecker, A. Burmaster, D. R. Evans, S. T. Hsu, M. Tajiri, A. Shimaoka: Proc. Int. Electron Devices Meeting (2002) 193–196.
18 N. Raghavan, K. L. Pey, W. Liu, X. Wu, X. Li, and M. Bosman: Microelectron. Eng. **88** (2011) 1124.
19 G. Rajendran, W. Banerjee, A. Chattopadhyay, and M. M. S. Aly: Adv. Electron. Mater. **7** (2021) 2100536.
20 Z. Miao, L. Chen, F. Zhou, and Q. Wang: J. Phys. D: Appl. Phys. **51** (2017) 2.
21 Z. Yan, Y. Guo, and G. Zhang: Adv. Mater. **23** (2011) 1351.
22 X. Wu, Z. Xu, F. Zhao, X. Xu, B. Liu, T. Sun, S. Liu, W. Zhao, and Z. Ma: J. Alloys Compd. **602** (2014) 175.
23 N. N. Ge, C. H. Gong, X. C. Yuan, H. Z. Zeng, and X. H. Wei: Royal Soc. Chem. **8** (2018) 29499.
24 X. Zhang, X. Chen, J. P. Cao, H. W. Wang, W. Y. Deng, L. H. Yang, K. Lin, Q. Li, Q. H. Li, and Y. L. Cao: Nanoscale **6** (2024) 3081.
25 S. F. Wang, Y. C. Wu, Y. G. Hsu, J. P. Chu, and C. H. Wu: J. Appl. Phys. **46** (2007) 2978.
26 H. Itoh, H. Asano, K. Fukuroi, M. Nagata, and H. Iwahara: J. Am. Ceram. Soc. **80** (1997) 1359.
27 C. Walczyk, D. Walczyk, T. Schroeder, T. Bertaud, M. Sowin, M. Lukosius, M. Fraschke, D. Wolansky, B. Tillack, and E. Miranda: IEEE Trans. Elect. Dev. **58** (2011) 3124.
28 H. Lei, T. Liu, and L. Xu: Mater. Chem. Phys. **237** (2019) 121819.
29 D. M. Mattox: Handbook of Physical Vapor Deposition (PVD) Processing (William Andrew, Norwich, 2010) 2nd ed.
30 M. Ozga, R. Mroczynski, A. Wolska, M. Klepka, M. Godlewski, and B. S. Witkowski: Solid-State Electron. **228** (2025) 109140.