Fabrication of Pressure Sensors Using Silicon Direct Bonding

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Anodic bonding is usually used in typical bulk micromachined pressure sensors. In this study, pressure sensors were fabricated by the 6-inch silicon direct bonding method. Silicon direct bonded wafers can yield approximately four times the number of chips than anodically bonded wafers. Equations are derived to compare the sizes of the chips obtained by the different methods. It is revealed that silicon direct bonding is particularly suitable in high-pressure applications and thick wafers. When contacted to form a pair, voids are sometimes observed upon inspection. Large voids did not change significantly, and it was also found in the experiment that small voids (<6 mm) disappeared after the high-temperature annealing process. Three major defects which are cracked membranes, broken membranes, and peeling at the wafer edge, were observed during the grinding of the sensing wafers.

1.   Introduction

Wafer bonding is a technology that is of great importance in the field of micromachining, especially in areas which require complex structures. Some of the earliest uses of wafer-to-wafer bonding were for the packaging of pressure sensors. Anodic bonding was introduced in 1969,[1] and it has become an important hermetic sealing process for microsensors and microactuators. Anodic bonding is used for joining an electron conducting material (silicon) and a material with ion conductivity (alkali-containing glass). The bonding mechanism is assisted by heating at 200–500°C and applying an external electric field typically in the range of 200–1000 V. When the external electric field is applied at an elevated temperature, the positive sodium ions in the glass migrate toward the negative

pole and create a depletion region adjacent to the interface of glass and silicon. The elevated temperature causes the positive sodium ions to become quite mobile facilitating the migration process. The voltage drop over this depletion layer creates a large electric field that pulls the wafers into intimate contact. This glass substrate provides stress isolation between the silicon sensing element and the housing when the wafer is diced up into individual chips. Anodic bonding affects the wafer bow significantly, because dissimilar materials have different thermal expansion coefficients.

Micromachined pressure sensors are being incorporated into many products when it is impractical to incorporate larger conventional pressure sensors using anodic bonding technology. Micromachined pressure sensors are being incorporated into such diverse types of equipment as medical instruments, laboratory instruments, industrial equipment and automotive circuitry. The features of small size, high performance, and low cost are needed for micromachined pressure sensors.

Silicon direct bonding is a process for bonding two silicon wafers at the atomic level without applying glue or an electric field. Silicon direct bonding produces structures with far fewer thermal mismatch problems when compared with anodic or eutectic bonding. Alkali contamination occurs in anodically bonded wafers, which limits the applications of anodic bonding.

Silicon direct bonding was first performed in the fabrication of pressure sensors by Peterson *et al.* in 1988.[2] The fabrication technology of integrated pressure sensors using silicon direct bonding was then published.[3] Silicon direct bonding was then adopted in sensors, actuators and microstructures.[4] Surface morphology in the case of silicon direct bonding was studied.[5] Schmidt's group studied pressure sensors fabricated using silicon direct bonding.[6-9] Gösele's group studied the interface of silicon direct bonding.[10-12] The silicon direct bonding technology was then reviewed.[13-15]

The front-end micromachining process steps are used to form the wafer with sealed cavities. IC fabrication can be performed by any existing foundry process. Cavities are present internally in the substrate, and will not cause alkali contamination. The detailed fabrication process of pressure sensors and the three major defects caused by grinding are presented in this article.

Silicon wafer bonding has major advantages over anodic bonding. The most important is that silicon directly bonded wafers can produce more chips than anodically bonded wafers. The process of silicon direct bonding is more complex than that of anodic bonding. However, there is an absence of mathematical expressions to compare the sizes of the two chips. The present study proposes mathematical expressions to compare these two methods.

2. Device Fabrication Process

In this study, pressure sensors were fabricated by forming cavities within a silicon wafer (constraint wafer) and then attaching a second silicon wafer (sensing wafer) to the first wafer and thinning the second wafer above the cavities, thereby producing diaphragms over sealed chambers. Finally, the device circuitry was realized by an IC process. The absolute pressure sensor measures pressure by sensing to what extent the pressure acting on the front side of the diaphragm deflects the diaphragm into the sealed chamber.

The process is shown in Fig. 1. The first step in the fabrication process is to form V-groove wafers. In this experiment, *n*-type (resistivity = 5–10 ohm-cm), 525-μm-thick, 6-inch Si (100) wafers were used. Constraint wafers (bottom wafer) of silicon dioxide are thermally grown on both sides as protective layers. The protective layer on the front side
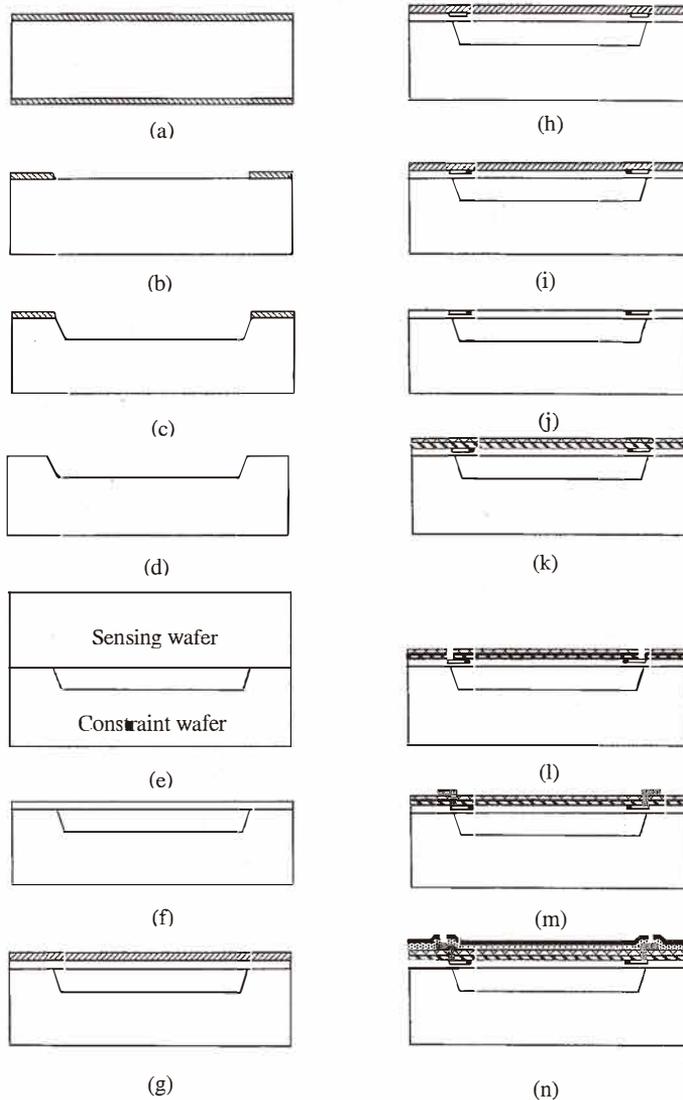

Fig. 1. Pressure sensor fabrication process: (a) grow thermal oxide; (b) define V-groove pattern; (c) TMAH etch; (d) remove oxide; (e) wafer contact and annealing; (f) wafer thinning; (g) grow pad oxide; (h) P+ ion implant; (i) P- ion implant; (j) remove oxide; (k) grow oxide/ nitride layer; (l) open contact; (m) metal patterning; (n) passivation layer and open bond pads.

of the wafer is patterned, and an etching window is opened using a 5:1 buffered oxide etching (BOE) solution (5 parts 40% NH_4F and 1 part 49% HF). The V-groove cavity is etched using an anisotropic etchant of 25% TMAH at 85°C for 90 min. The depth of 50 μm of the cavities is controlled by the etch time. The first step is shown in Fig. 1(a) to Fig. 1(c).

The second step involves bonding two silicon wafers together. It is necessary to perform RCA cleaning, because organic contamination and particle adhesion should be avoided in the annealing furnace. Two wafers are contact bonded together and then annealed at a high temperature of 1100°C for two hours. Figure 1(d) and Fig. 1(e) show the second step.

The third step involves grinding the sensing wafer. The sensing wafers are then thinned down to a thickness of 23 μm using precision polishing. The diaphragm thickness is a key factor which affects the sensitivity of pressure sensors. The third step is shown in Fig. 1(f).

The final step is the device circuit fabrication process. A pad oxide is grown. P+ ion implantation is performed. Connections to resistors are provided by the P+ diffusion area. Four pairs of piezo-resistors are formed by P- ion implantation on the four sides of the diaphragm. Then, the pad oxide is removed. A contact opening is formed through the oxide to the P+ region. Aluminum metalization and patterning are performed. A silicon dioxide layer protects the top surface of the silicon wafer. A silicon nitride layer protects the silicon dioxide and the metal layer. Finally, the bond pads are opened for attachment of the wire bonds. The final step is shown in Fig. 1(g) to Fig. 1(n).

3.   Results and Discussion

3.1 *Chip size analysis*

Figure 2(a) shows front-side-etched pressure sensors fabricated using silicon direct bonding. Figure 2(b) shows back-side-etched pressure sensors using anodic bonding. It is clear that silicon directly bonded chips are of smaller size. The smaller chip size is due to front-side etching. The small thickness is because of the grinding of the sensing wafers.

Pressure sensor sensitivity (S) can be expressed as eq. (1),[16]

$$S = \frac{\Delta V_o}{V_c P} = 0.1539\pi_{44}(1 - \upsilon)\left(\frac{L}{h}\right)^2 , \tag{1}$$

where ΔV_o is the signal voltage output, V_c is the power supply voltage, P is pressure, S is sensor sensitivity, L is diaphragm length, h is diaphragm thickness, υ (=0.27) is Poisson ratio of the sensor and π_{44} is the piezoresistive coefficient. From Fig. 2, eq. (2) can be obtained.

$$\tan(54.7°) = \frac{2t}{D} \tag{2}$$

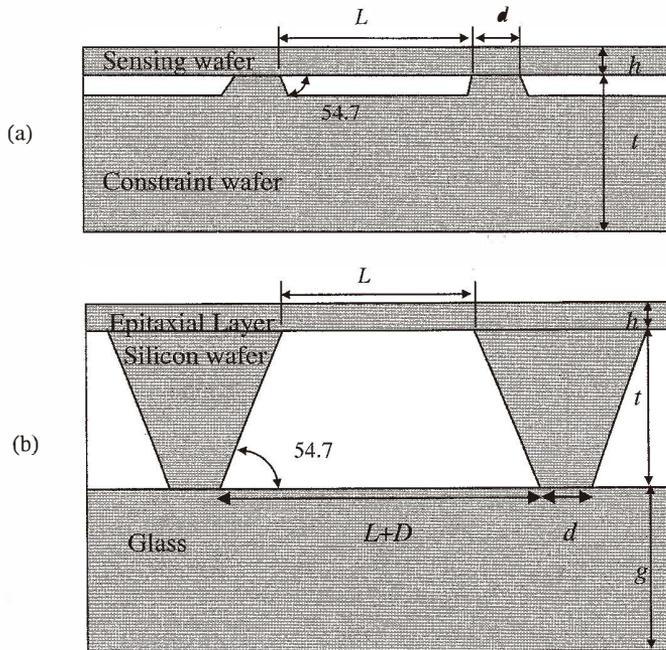Equation (3) can be derived from eq. (1) and eq. (2).

Fig. 2.   Schematic of front-side etching and back-side etching. *L* is effective sensing length. *D* is the increase in size by back-side etching over that of front-side etching. The glass thickness is *g*. (a) Silicon direct bonding by front-side etching; (b) Anodic bonding by back-side etching.

$$\frac{D}{L} = 0.475\sqrt{\frac{\pi_{44}}{S}\left(\frac{t}{h}\right)} \tag{3}$$

Then, it can be expressed in the following form.

$$\left(\frac{L}{L+D}\right)^2 = \frac{1}{\left(1+0.475\sqrt{\frac{\pi_{44}}{S}\left(\frac{t}{h}\right)}\right)^2} \tag{4}$$

Here, *D* is the difference in size between the back-side etched window and the front-side etched window, and it denotes the reduction in size realized by silicon direct bonding over anodic bonding. The value of $(L/(L+D))^2$ is the ratio of the front-side etched window to the back-side etched window, and t/h is the ratio of constraint wafer thickness to sensing wafer thickness. The piezoresistive coefficient π_{44} is determined by the implantation conditions and annealing conditions. The sensitivity is determined by the pressure range and the magnitude of output voltage.

Equation (4) is presented as dimensionless, because we can calculate $(L/(L+D))^2$ for different etch window sizes, sensing wafer thickness, and constraint wafer thickness. Equation (4) shows $(L/(L+D))^2$ as a function of t/h and π_{44}/S. To achieve low cost, a small size is desired. A low sensitivity S can obtain a small $(L/(L+D))^2$, and high-pressure sensors have low sensitivity. Thus, silicon direction bonding can reduce the chip size significantly for high-pressure applications.

Large-diameter wafers must be thicker in order to maintain their structural integrity and planarity during the wide range of processing steps encountered during fabrication. From eq. (4), a large constraint wafer thickness t can obtain a small $(L/(L+D))^2$, and this means that anodic bonding can produce less chips from a thick wafer.

Figure 3(a) shows the size of chips fabricated by silicon direct bonding and anodic bonding. The difference in chip size is caused by front-side etching and back-side etching.
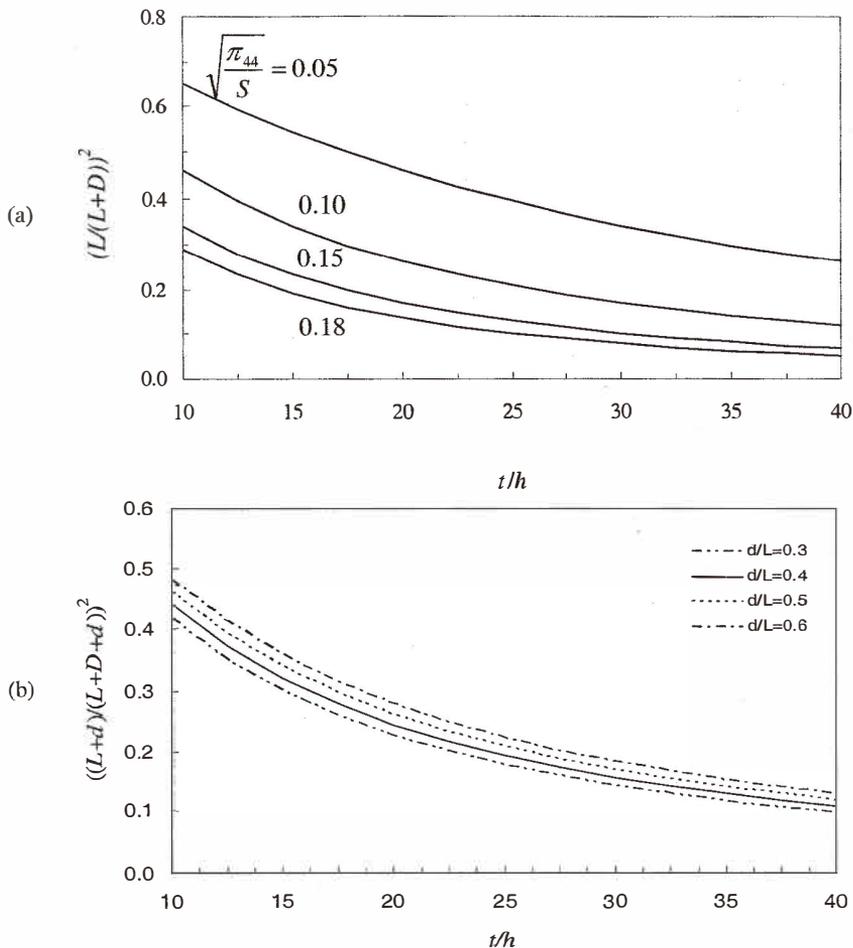

Fig. 3. Size of chips fabricated by silicon direct bonding and anodic bonding, (a) comparison of etch window sizes, (b) comparison of full chip size.

The constraint wafer thickness $t = 525$ μm, the sensing membrane thickness $h = 23$ μm, π_{44} = 100×10^{-12} cm^2/dyne, and $S = 43.5$ μV/V/kPa are calculated, and $t/h = 22.8$, $(\pi_{44} / S)^{0.5} = 0.15$, and $(L/(L+D))^2 = 0.15$ can be obtained. From Fig. 3(a), it is clear that front-side etching can save more of the chip area than back-side etching. However, the area saved per chip is overpredicted by Fig. 3(a), because the bonded rims are neglected.

If the bonded rims are considered, eq. (4) can be modified to eq. (5).

$$\left(\frac{L+d}{L+D+d} \right)^2 = \left(\frac{1 + d/L}{1 + 0.475 \sqrt{\dfrac{\pi_{44}}{S} \left(\dfrac{t}{h} \right)} + \dfrac{d}{L}} \right)^2 \tag{5}$$

From Fig. 3(b), we can obtain $((L+d)/(L+D+d))^2 = 0.23$ using $t = 525$ μm, $h = 23$ μm, $\pi_{44} = 100 \times 10^{-12}$ cm^2/dyne, $S = 43.5$ μV/V/kPa, $L = 600$ μm, and $d = 300$ μm. Thus, the chip size ratio of silicon direct bonding and anodic bonding is 0.23. Silicon directly bonded wafers can yield approximately four times more chips than anodically bonded wafers. Although the fabrication process of silicon direct bonding is more complex than that of anodic bonding, it is still cost-effective because it yields four times the number of chips.

To compare the fabrication costs of the two methods, the total complexity of the fabrication processes are considered. The process of silicon direct bonding is more complex than that of anodic bonding. The process of anodic bonding is easy and stable, and an electrochemical automatic etch-stop is the most widely adopted technique for fabricating membranes. The throughput of anodic bonding and bulk micromachining is low. The bonded and thinned silicon wafers can be of high yield, as a precise grinding system is adopted. By controlling particles, silicon direct bonding can obtain a high yield. In addition, the throughput of silicon direct bonding is high. Thus, chip size is the key parameter in cost.

To decrease the chip size, back-side etching can be replaced by isotropic deep reactive ion etching (RIE). Deep RIE, based upon the inductively coupled plasma (ICP) process, has been adopted in the fabrication of pressure sensors.[17–18] Pressure sensors fabricated using deep RIE process are designed for use in aircraft and spacecraft. To meet the high-temperature requirements, silicon carbide is selected as a piezoresistive material. Silicon-on-insulator (SOI) wafers and the fabrication process for silicon carbine piezoresistive pressure sensors are still expensive. Small size, high performance, and low cost are needed for the new generations of equipment in the medical, analytical, and industrial fields, but silicon carbine piezoresistive pressure sensors cannot meet the cost demand at present.

3.2 Surface roughness effect

Silicon direct bonding relies on forces that naturally attract surfaces together when wafers are very smooth and flat. Silicon wafers deform during the matching of two wafers at room temperature. The deformation of wafers was described by Maszara *et al.*[5] The contacting process is critical to prevent trapping of particles or air between the surfaces. In

order to avoid void generation at the interface during storage or annealing, the surfaces of silicon wafers should be optically smooth, flat, and clean, and bonding should be accomplished by van der Waals forces.

The surface roughness (rms value) has to be less than 0.5 nm to achieve spontaneous bonding of cleaned silicon wafers at room temperature without applying additional pressure.[12] Fortunately, chemical mechanical polishing can achieve a surface roughness of less than 0.3 nm. Commercial wafers can meet the requirement. Figure 4(a) shows the IR image of wafers subjected to silicon direct bonding with surface roughnesses of less than 0.5 nm; it shows that an unpatterned wafer pair can be bonded free of bubbles. Figure 4(b) shows an IR image of a high-density bonded wafer pair with bubbles. Without applying additional pressure, it is found that unpatterned wafers can be bonded free of bubbles and high-density cavities can generate bubbles. Thus, applying additional pressure can decrease the generation of bubbles.

3.3 *High-temperature annealing effect*

After surface preparation, two wafers are immediately brought into contact with each other so as to avoid any particulate contamination of the surfaces. On contact the wafers stick together due to the hydrogen bonding of hydroxyl groups and van der Waals forces. The contacted wafers are then transferred to a furnace tube for heat treatment at 1100°C for 2 h. When contacting and annealing a wafer pair, voids are sometimes observed upon inspection. These voids are classified into two categories: extrinsic and intrinsic.

The extrinsic voids are those created by particles, protrusions on the wafer surfaces, or trapped air. These voids are usually observed on contact and do not change significantly

(a)   (b)
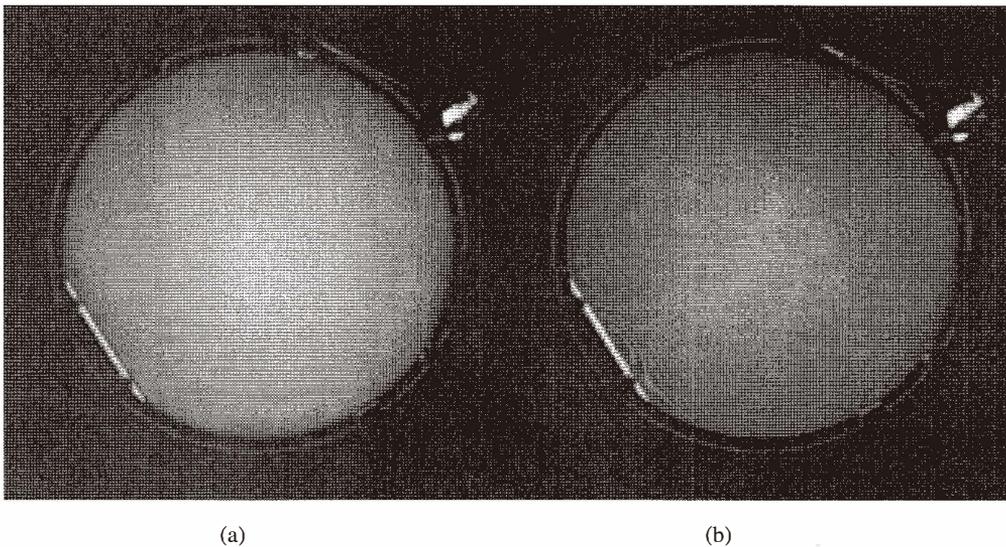
Fig. 4.   IR image of silicon directly bonded, (a) unpatterned wafers, (b) with high-density cavity structures.

during annealing. Figure 5(a) shows two large extrinsic voids which appeared at contact. The two squares are for process alignment. Laser marking of wafer numbers between the interface of the two bonded wafers caused the large void near the flat plane. Figure 5(b) shows the wafer after high-temperature annealing in nitrogen ambient. The large voids did not change significantly. It is worth noting that the small voids (< 6 mm) disappeared after the high-temperature annealing process in this experiment.

Intrinsic voids are generated during the annealing cycles. After contact, the wafer pair appears to be void-free. As the annealing temperature is increased, voids begin to appear above 400°C and subsequently disappear above 900°C. Mitani *et al.*[19] suggested annealing at 1100°C for a few hours to eliminate any bubbles. The disappearance of thermal bubbles at the bonding interface after 1100°C annealing has been found mainly due to the gas dissolution into the surrounding bulk silicon or oxide layer.

3.4 *Grinding effect*

The precision grinding system used a 2-step process including coarse grinding and subsequent fine grinding in order to partially remove the damaged layer and obtain a sensing wafer with precise thickness. Following polishing, we subjected every wafer to an automated, scrubless, chemical-cleaning process. The purpose of this process is to remove any adherent particles or metallic impurities from the polished surface. The sensing wafer thickness and cavity size determine the detectable pressure range. The thickness of the sensing wafer and the cavity size are key factors in determining the sensitivity of pressure sensors.

There are three major defects in the grinding process. Figure 6(a) shows cracks at the membrane edge. As shown in Fig. 6(b), membranes are broken during the wafer grinding process. Figure 6(c) shows peeling at the wafer edge. The bonded interfaces should be
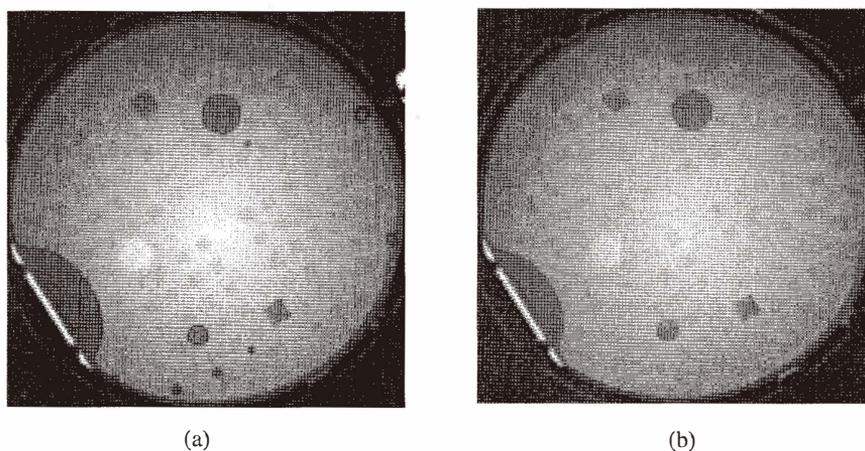

| (a) | (b) |

Fig. 5. Wafer with V-groove structure: (a) pre-bonded wafers; (b) after 1100°C, 2 h annealing.
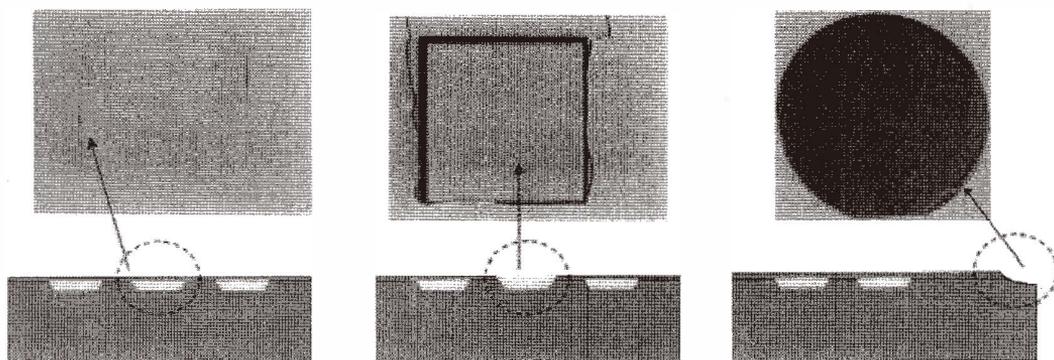
Fig. 6.   Defeats caused by thinning and polishing: (a) micro-cracks at membrane edge; (b) broken membranes; (c) wafer edge peeling.

void-free after high-temperature annealing, because voids cause three major defects during the thinning of sensing wafers. A decrease in defects with a low thinning rate was observed in this experiment.

The bow of plain wafers and the bow of bonded wafers should be controlled to < 20 μm and < 30 μm, respectively. This requirement is reasonable for 6-inch wafers. A bow of less than 5 μm for 4-inch wafers is too strict a requirement.[14] A bow of < 5 μm is very expensive, because such a wafer is not easy to fabricate. The low cost requirement cannot be met, if a bow of less than 5 μm is necessary. The bow < 50 μm is commercial grade, and the bow < 30 μm is still reasonable in special applications.

The other problem is the so-called dishing effect.[20] Pressure sensors require the bonding of wafers with cavities etched in one of the wafers, thus forming sealed cavities in the wafer after bonding. The nature of the gases that exist in the cavities can be very important, particularly in subsequent high-temperature bonding. It has been shown that when wafers are contacted in air, and subsequently annealed at high temperature, the oxygen in the cavity can react with the silicon surface and create a partial vacuum. When the oxygen is completely consumed, the resultant pressure inside the cavity is 0.8 atm, consistent with the consumption of the 20% oxygen in air. Under high temperatures, the residual gases trapped in the cavities can induce plastic deformation in thin silicon membranes as the gases expand.[21] Pressure sensors fabricated using silicon direct bonding have a small chip size. Thus, the membrane deflection is relatively small. As shown in Fig. 7, the cross section of the pressure sensor fabricated using silicon direct bonding shows a uniform membrane after appropriate grinding.

3.5 *Bonding strength*

Figure 8 shows the bonded wafers after 1100°C annealing, and it shows that the interface is atomically rough. The bonding strength after the contact was low. Surface energies of about 0.2 J/m² have been reported.[22] Above 300°C, the strength increased with increasing temperature. It was thought that room-temperature adhesion takes place as the
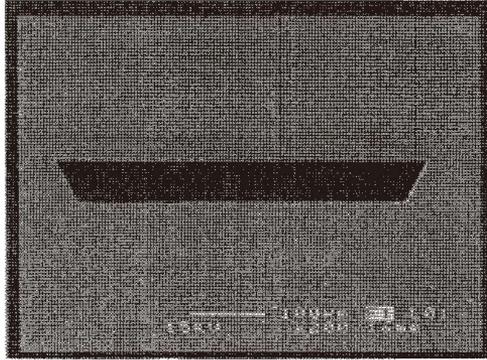
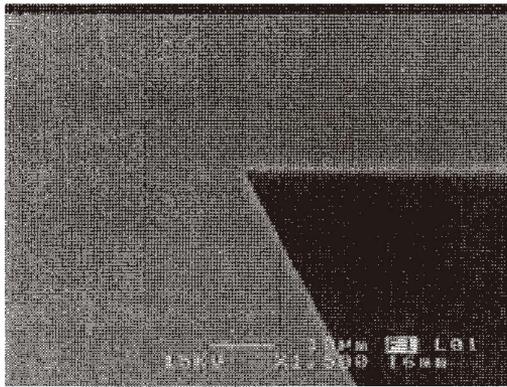Fig. 7.   Cross section of bonded wafer after annealing.

Fig. 8.   SEM image of the interfaces of a bonded wafer pair after annealing.

result of interaction between Si-OH groups, formed on the surface during the hydrophilic treatment. The increasing bonding force by heating is caused by the formation of Si-O-Si bonds.[23] The present bonded wafers were tested, and the surface energy was found to be sufficient for wafer sawing.

4.   Conclusions

Pressure sensors using silicon direct bonding have been fabricated. The sensor sensitivity is 43.5 μV/V/kPa, and the temperature coefficient of sensitivity is –0.23%FS/°C. Anodic bonding is usually used in bulk micromachined pressure sensors. Chip size after sawing is 1.1 mm × 1.1 mm in this study, and silicon direct bonded wafers can yield

approximately four times more chips than anodically bonded wafers. Equations are proposed to compare the size of silicon direct bonded chips with that of anodically bonded chips.

Small size, high performance, and low cost are needed for new generations of equipment in the medical, analytical, and industrial fields. Silicon direct bonding is particularly suitable in low-pressure-sensitive, thick wafers, because silicon bonded wafers are able to produce many more chips than anodically bonded wafers. Although the fabrication process of silicon direct bonding is more complex than that of anodic bonding, it is still cost effective because it yields four times the number of chips. Pressure sensors using the deep RIE process can decrease the chip size, but the cost is high. Silicon carbine piezoresistive pressure sensors are designed for high-temperature applications.

For silicon direct bonding, the surfaces of the silicon wafers have to be optically smooth, flat, and clean. Without applying additional pressure, it is found that unpatterned wafers can bond easily and are bubble-free and a high density of cavities may generate bubbles. Applying additional pressure can decrease the generation of bubbles. In this experiment, small voids (< 6 mm) disappeared during high-temperature annealing. The bow of < 5 μm for 4-inch wafers can be extended to the bow of < 20 μm for 6-inch wafers.

Cracked membranes, broken membranes, and peeling at wafer edges are three major defects. Low thinning rates decreased defects in this experiment. The bonded wafers were tested, and the bonding strength was found to be sufficient for wafer sawing.

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In January 2001, he joined Asia Pacific Microsystems, Hsinchu, where he had a position as a R&D manager and product manager at the Intelligent Sensor Division. He developed many pressure sensors and created new techniques. He was also the project leader of monolithic pressure sensors for tire pressure monitoring systems. Since September 2003, he has been working with Professor Michael M. Chen as a visiting scientist in the department of mechanical engineering, the University of Michigan, Ann Arbor, Michigan. He is studying the applications of inkjet and MEMS. He is a member of IEEE, SPIE, and ASME. His research interests include microsensors, microactuators, optical-MEMSs, and bio-MEMSs.