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Design and Fabrication of Air-Bridge CPW using Porous Silicon and MEMS Technology

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This paper proposes a three-dimensional structure for an RF passive device using a thick oxidized porous silicon layer (OPSL). The OPS air-bridge was fabricated using an anodic reaction, reactive ion etching (RIE), tetramethyl ammonium hydroxide (TMAH) etching, and a multistep oxidation process. The problem of the high dielectric loss of a waveguide on silicon can be solved using a thick OPS air-bridge. The three dimensional structures were fabricated using a 20 wt.% TMAH solution at 80°C for 3 h, and the thickness of the micromachined OPS air-bridge was 10 μm. A coplanar waveguide (CPW) structure was also fabricated on the OPSL air-bridge for RF application. The fabricated structure was 2 mm in length, and the width of the signal line and the gap between the ground and the signal lines were 100 μm and 20 μm, respectively. This process is well compatible with conventional complementary metal oxide semiconductor (CMOS) fabrication process without post-processing, and does not require an additional mask for silicon etching.

1. Introduction

With the recent wide-spread development of wireless and mobile communication systems for commercial use, the development of low-cost, low-weight, and high-performance RF-MEMS devices is in great demand. Micromachining is one of the important technologies that offer high functionality and performance at the system level for low cost. Various passive microwave components fabricated by micromachining have already been proposed. At microwave frequencies, monolithic microwave integrated circuits (MMIC's) employ GaAs technology with integrated active devices. While GaAs offers a low dielectric constant and compatibility with active device technology, large-area GaAs substrates are costly to produce with a low defect density. Meanwhile, although silicon has

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very mature technology for device fabrication and integration, it has not been used as a microwave substrate due to its extremely high dielectric loss.(1–3) To overcome this problem, a high-resistivity silicon substrate has been used for the microwave region,(4–5) yet this is not good for the integration of silicon active devices. Micromachined structures such as an oxide-bridge or membrane have been identified as a way to overcome the problem of the high dielectric loss of a low-resistivity silicon substrate. Yet, such a structure is relatively fragile, as the oxide bridge supporting the passive elements is too thin for use in a general process. (6–8)

However, an oxidized porous silicon (OPS) layer offers many advantages as a microwave material for overcoming the high dielectric loss of a low-resistivity silicon substrate in microwave passive devices.(9) Plus, an OPS layer has low fabrication cost and time for a thick SiO_2 layer compared with other oxidation processes.

Accordingly, in this study, we investigated the three-dimensional structure of an OPS layer for RF-MEMS application. The OPS layer was fabricated using porous silicon micromachining, reactive ion etching (RIE), tetramethyl ammonium hydroxide (TMAH) etching, and a multistep oxidation process.(10,11) First, the porous silicon layer (PSL) was obtained using an anodic reaction process. Then, the PSL was oxidized by multistep thermal oxidation to form a thick oxide layer. Finally, a three-dimensional structure was formed by a surface micromachining technique using a TMAH solution. A CPW structure was also fabricated on the OPSL air-bridge to lower the insertion loss in the microwave frequency range.

2. Experimental

2.1 *Silicon anisotropic etching*

Anisotropic chemical wet etching is commonly used in MEMS technology to fabricate three-dimensional structures on a single-crystal silicon wafer. The use of a TMAH solution (Aldrich Chem. Co.) for silicon etching is gaining popularity in MEMS, plus it is complementary metal oxide semiconductor (CMOS) compatible, as it has no mobile K^+ contaminants, which are often encountered in a KOH-like etchant.

This paper presents the anisotropic etching properties of TMAH solutions for fabricating three-dimensional structures for RF passive elements. The starting material was a (100) p-type silicon wafer. A NON (Si_3N_4(150 nm) /SiO_2(300 nm) /Si_3N_4(150 nm)) structure was produced by LPCVD, APCVD, and PECVD, respectively. The three-dimensional structure of the NON insulator was fabricated by silicon anisotropic etching. The starting etching mixture in the experiment was a 25 wt.% TMAH solution diluted with DI water.

2.2 *Formation of oxidized porous silicon*

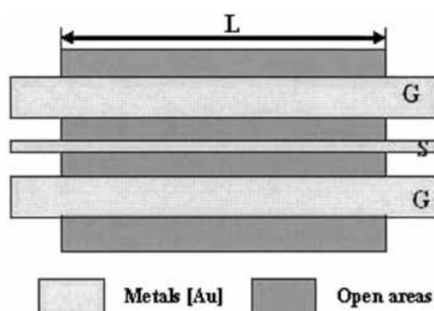
The oxidized porous silicon layer (OPSL) was fabricated by an anodic reaction and a multistep oxidation process.(9–10) First, the PSL was obtained by an anodic reaction process, then the OPSL was fabricated by a multistep oxidation process. The properties of the PSL, including the porosity, etch depth, and pore size, all depend on the current density, hydrofluoric acid (HF) concentration, silicon type, and silicon resistivity. A porosity of

56% is suitable for oxidation. The OPSL surface analysis was performed by X-ray photoelectron spectroscopy (XPS).

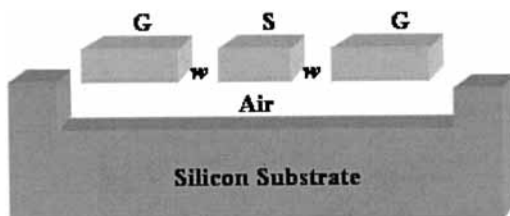
2.3 *Design and Fabrication*

The coplanar waveguide (CPW) lines were designed for a nominal characteristic impedance of 50 Ω. Figure 1 shows the schematic diagrams of an OPS air-bridge CPW on a silicon substrate. Figure 1(a) shows a simplified layout of the ground-signal-ground configuration. A cross-sectional diagram of the CPW is shown in Fig. 1(b). A gold metallized CPW 2.5 μm thick on an OPS substrate 20 μm thick has been shown to have a measured attenuation per length of 0.1 dB/mm at 4 GHz.[4] In this study, the CPW lines had a signal linewidth s = 100 μm and a line spacing w = 20 μm, and 2 μm of Au electrodeposition.

The OPS air-bridge structures were fabricated using an anodic reaction, RIE, TMAH etching, Au electroplating, and a multistep oxidation process.[11] Figure 2 shows the



(a)



(b)

Fig. 1. Schematic diagrams of OPS air-bridge CPW. (a) Simplified layout, (b) cross-sectional diagram.

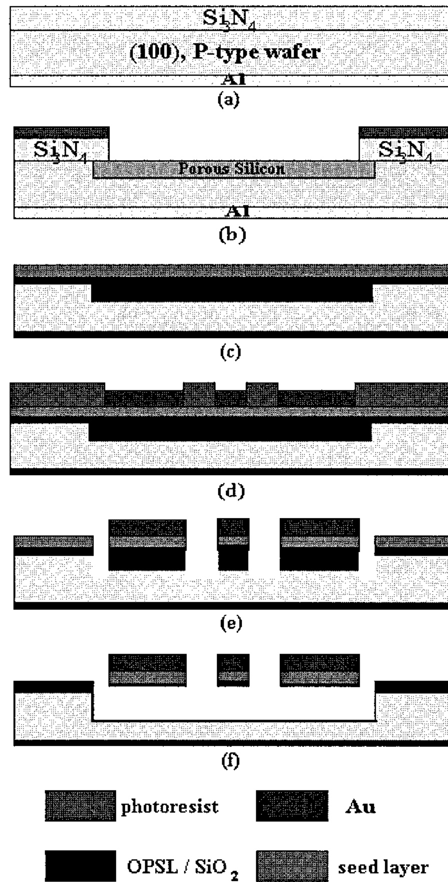


Fig. 2. Fabrication process of OPS air-bridge CPW.

fabrication process of the OPS air-bridge CPW. The substrate was a (100) p-type silicon wafer. First, silicon nitride (Si_3N_4) was deposited on the silicon substrate by LPCVD at 800°C for 30 min to obtain a thickness of 150 nm. Windows for electrical contact were defined on the back-surface, followed by RIE of the Si_3N_4 layer. To provide an ohmic contact for anodization, the silicon nitride resulting from the anodic reaction was patterned and RIE performed. Then, aluminum (Al) with a thickness of 150 nm was deposited using thermal evaporation to provide a uniform current density during the anodic reaction process shown in Fig. 2(a). Thereafter, the OPSL was obtained by an anodic reaction and a multistep oxidation process. The anodic reaction was performed in a 43 wt.% aqueous HF solution for 10 min at room temperature by applying a constant current density of 20 mA/cm^2. The silicon nitride was then etched away after the anodic reaction process shown in Fig. 2(b). Next, the PSL was pre-oxidized at 400°C under dry oxygen at atmospheric pressure for 30 min, which created a thin layer of silicon dioxide over all the pore walls,

thereby preventing the destruction of the PSL during the further oxidation process. The pre-oxidized PSL was oxidized for 1 h in dry oxygen at 1000°C and for 30 min in wet oxygen at 1000°C for surface solidity. Then, Ni-Cr (50 nm) /Au (50 nm), as a seed layer for the Au electroplating process, was deposited on the front side shown in Fig. 2(c). The 3-D structure was defined using a thick photoresist (SU-8) to obtain a total resist thickness higher than 10 µm. Then, 2 µm of Au was grown by electrodeposition in the resist-free windows. The bath temperature and current density were maintained constant at 40°C and 10 mA/cm^2, respectively, during the electroplating process. To obtain the 2 µm thickness, the process was performed for 25 min as shown in Fig. 2(d). The seed layer was then removed by wet etching, after the photoresist had been stripped off. The TMAH etching window was defined by a photolithography process. Thereafter, the silicon dioxide and OPS were etched away by RIE as shown in Fig. 2(e). Lastly, the silicon underneath the OPSL was removed by surface micromachining using a TMAH solution. The suspended OPS CPW with a 3-D structure was fabricated using a 20 wt.% TMAH solution at 80°C as shown in Fig. 2(f).

3. Results and Discussion

3.1 *Characteristics of silicon anisotropic etching*

According to the previous study(12) on silicon anisotropic etching using a TMAH solution, the silicon etch rate increased linearly with decreasing the TMAH solution concentration from 25 wt.% to 5 wt.% and increasing TMAH solution temperature from 80°C to 90°C. In addition, the etched silicon surface roughness decreased as the TMAH concentration increased.

Figure 3 shows SEM images of the etching pattern obtained with the TMAH solution. The 3-D structures were successfully fabricated. The etching process was performed using a 20 wt.% TMAH solution at 80°C, and the etch rate of the (100) silicon wafer was 32 mm/h.

3.2 *Characteristics of OPSL*

The properties of the PSL, including the porosity, etch depth, and pore size, all depend on the current density, hydrofluoric acid concentration, silicon type, and silicon resistivity. A porosity of 56% is suitable for oxidation. Figure 4 shows the porosity of the porous silicon with respect to the HF concentration, where the porosity decreased with increasing in the HF concentration. Figure 5 shows the porosity with respect to the current density, where the porosity increased with increasing in the current density.

Thus, to achieve a PSL with a 56% porosity, a 43 wt.% HF solution was used with a constant current density of 20 mA/cm^2. The thickness of the PSL was fabricated according to the process time. The growth rate of the PSL was 1.4 µm/min, and its porosity was 56%.™ Then, the OPSL was formed using a multistep thermal oxidation process. Figure 6 shows an SEM image of a 10-µm-thick OPSL. The surface and internal composition of the OPSL were analyzed by X-ray photoelectron spectroscopy (XPS). Figure 7 shows the oxide characteristics of the OPSL with respect to surface (Fig. 7(a)) and depth (Fig. 7(b)). The Si-2p peak and O-1s peak of the OPSL surface were measured at the binding energies

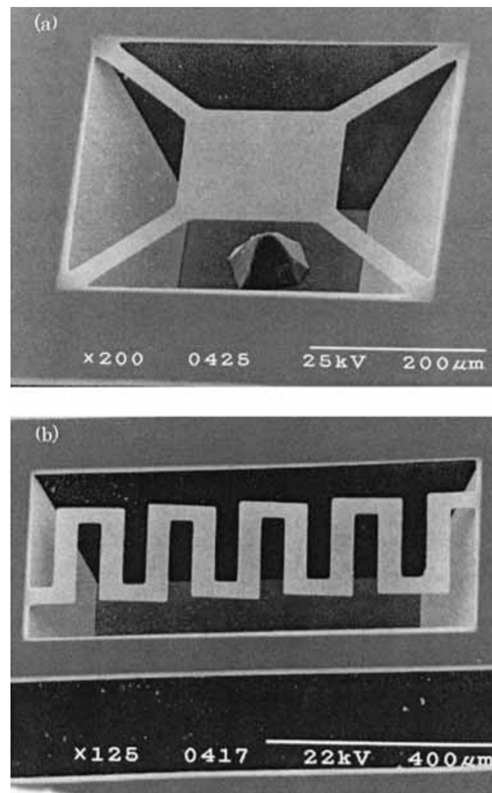


Fig. 3. SEM images of etching pattern obtained with TMAH solution (20 wt.%, 80°C). (a) Membrane pattern, (b) resistor pattern.

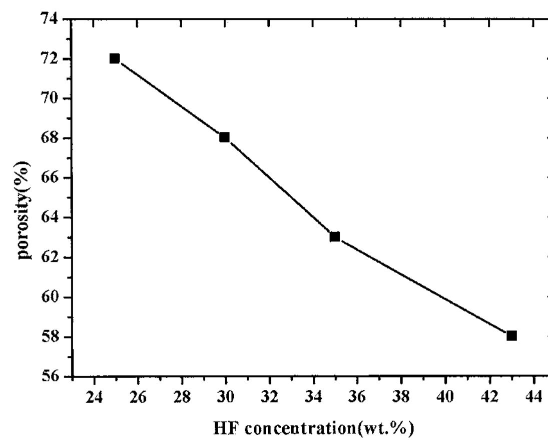


Fig. 4. Porosity versus HF concentration.

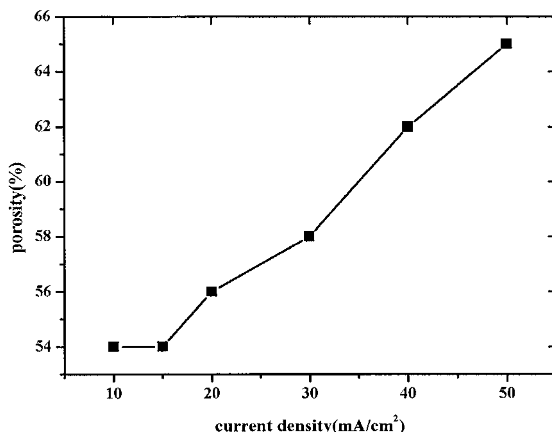


Fig. 5. Porosity *versus* current density.

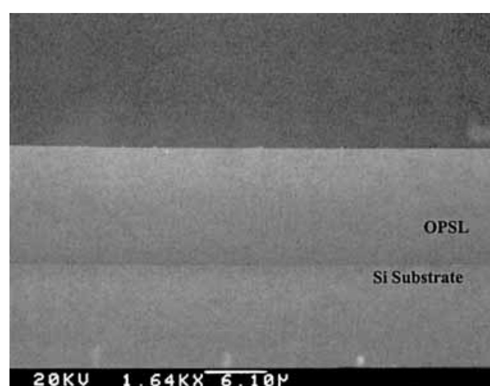
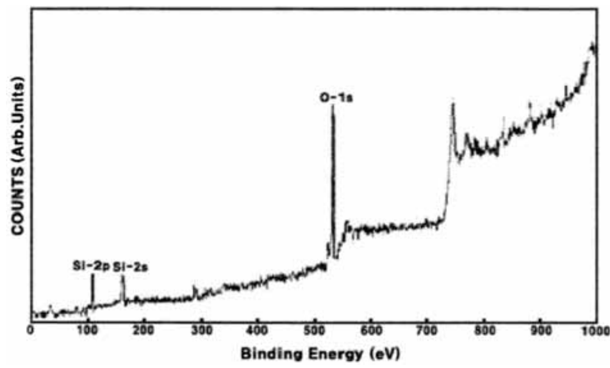


Fig. 6. SEM image of OPSL with thickness of 10 μm.

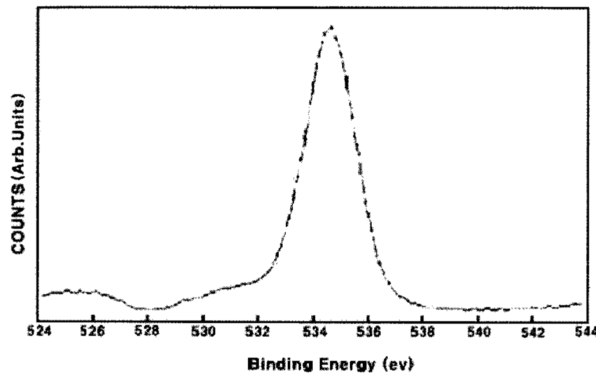
of 104.9 eV and 534.1 eV, respectively. The O-1s peak of the OPSL at 10 μm depth was at 534.4 eV. In the case of thermal oxide films, the Si-2p peak and the O-1s peak were at 105.0 eV and 534.2 eV, respectively. As a result, the binding energy of the OPSL compared with that of the thermal oxide film was moved by –0.1 eV and showed almost identical characteristics.

3.3 *OPS air-bridge CPW*

In this paper, the air-bridge structures were fabricated using an anodic reaction, RIE, a multistep oxidation process, and TMAH etching. First, to fabricate a PSL of about 10 μm tchickness, an anodic reaction was performed in a 43 wt.% HF solution for 10 min at room temperature by applying a constant current density of 20 mA/cm^2. Then, the OPSL was formed by a multistep oxidation process under the above conditions. Lastly, the 3-D structures were fabricated using a 20 wt.% TMAH solution at 80°C for 3 h.



(a)



(b)

Fig. 7. XPS analysis of OPSL. (a) Surface, (b) 10 mm depth.

The micromachined OPS air-bridge is shown in Fig. 8, where the thickness was 10 mm and the 300 µm width of the air-bridge was entirely micromachined. The <100>-directional etch rate was 32 µm/h.

Figure 9 shows a SEM image of the air-bridge CPW structure for RF application. The CPW was fabricated on the OPSL air-bridge using 10 µm-thick SiO_2, and the length of the fabricated CPW structure was 2 mm. The width of the signal line and gap between the ground and the signal were 100 µm and 20 µm, respectively. The CPW lines consisted of a double layer of evaporated Ni-Cr/Au followed by 2 µm of Au electrodeposition.

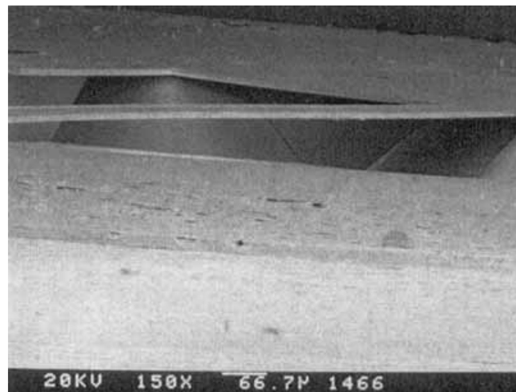


Fig. 8. SEM image of OPS air-bridge structure.

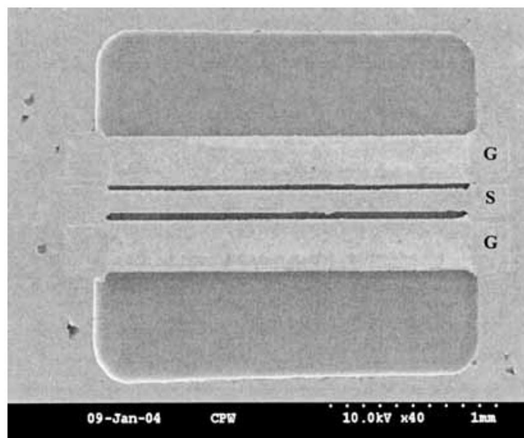


Fig. 9. SEM image of OPS air-bridge CPW structure.

4. Conclusions

OPS air-bridge structures were fabricated by an anodic reaction, RIE, a multistep oxidation process, and a TMAH etching process. The thickness of the OPS air-bridge structure was 10 μm, the silicon etch rate was 32 μm/h, and the 3-D structures were fabricated using a 20 wt.% TMAH solution. Thus, a TMAH solution was found to be compatible with the CMOS fabrication process due to the post-processing, plus it did not require any additional photomask or back-surface etching. Also, the structure was stable because of the thick oxide layer. Three-dimensional CPW structures were fabricated by the above fabrication process and found to have a low insertion loss and low dielectic loss in the microwave frequency range.

Accordingly, the advantages of the proposed fabrication process are that it has a low processing cost and enables the fablication of monolithic structures compatible with analog digital CMOS circuits. The proposed process is also expected to improve the insertion loss characteristics, duspersion characeristics, and phase velocity in MMIC applications.

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