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Fabrication of Direct-Printed OTFT Array Using Flexible h-PDMS Stamp

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Printed organic thin-film transistors (OTFTs) for use as a switching device in an organic light-emitting diode (OLED) were fabricated by microcontact and direct printing at room temperature. The printed OTFT was used in the fabrication of a printed gate with source and drain electrodes (W/L = 500 μm/5 μm, 500 μm/10 μm, and 500 μm/20 μm) printed using a hard poly (dimethylsiloxane) (h-PDMS) stamp and low-viscosity Ag ink, a spin coated parylene-C gate dielectric, and a soluble poly (3-hexylthiophene-2,5-dily) (P3HT) organic semiconductor on flexible, transparent poly(ethylenenaphthalate) (PEN) plastic substrates. The printed OTFT was characterized and the following parameters were obtained: a mobility of 0.06 (±0.02) cm^2/Vs, an on/off current ratio of 10^3, and a subthreshold slope of 2.53 V/decade. Also, it was possible to fabricate a printed OTFT with channel lengths down to 5 μm, and reduce the fabrication process by 20 steps compared with photolithography.

1. Introduction

The development of organic thin-film transistors (OTFTs) for use as a switching and driving device in flexible displays, low-cost printed electronics, and printed electro-mechanical systems (PEMS) is a very important field of study because of the increasing demand for such devices.(1) Consequently, many of the early demonstrations of OTFTs and circuits made use of a variety of conventional device fabrication techniques for material deposition and patterning, including vapor-phase deposition, photolithography,

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and wet and dry etching.[2] However, these methods have disadvantages: they often require photoresists, solvents, and developers that are incompatible with the materials that must be patterned, they are unable to take advantage of the simple processes and high temperatures that can be used with many organic materials, they cannot be used for the single-step patterning of large areas, and they do not work well when applied to rough, uneven, or curved substrates.

More recently, because of these and other limitations, a number of techniques and processes including ink-jet printing, screen printing, and microcontact printing have been introduced for the fabrication of OTFT circuits and displays that aim specifically at reducing the fabrication cost.[3–5] In particular, microcontact printing is the collective name for soft lithography, which has been developed as an alternative to photolithography and as a replication technology for micro- and nanofabrication.[6–8] This technique uses a patterned poly (dimethylsiloxane) (PDMS) elastomer as the mold, stamp, or mask to generate or transfer the pattern and is a low-cost process.[5,9–11]

In this paper, we report in more detail a related study in which a printed OTFT was used for the fabrication of printed electrodes with a soluble organic semiconductor on poly (ethylenenaphthalate) (PEN, Teijin Dupont Films) plastic substrates. The indium tin oxide (ITO) gate electrodes of the OTFT were patterned by microcontact printing and wet etching, and source and drain electrodes were fabricated by a high-resolution printing technique based on injecting a pattern from a hard PDMS (h-PDMS) stamp[12] to a PEN substrate by physical contact using low-viscosity Ag ink. A printed OTFT with a parylene-C[13] dielectric layer was formed using a special coating system, and poly (3-hexylthiophene-2,5-dily) (P3HT)[14] as an organic semiconductor layer was used in the ink-jet printing process. Microcontact and direct printing offer immediate advantages over photolithography and other conventional micro- and nanofabrication techniques for applications in which the patterning of nonplanar substrates, or unusual materials, or large-area patterning are of major concern.

2. Fabrication of h-PDMS Stamp and Printed OTFT

To fabricate a high-resolution and large-area printed OTFT, the following steps were performed: the design and manufacture of a master, the fabrication of a soft PDMS (s-PDMS) stamp and an h-PDMS stamp, and a microcontact and direct printing process. We used a PEN substrate with a thickness of 200 μm and a surface roughness of 0.6 nm. The PEN was preshrunk at a temperature of 200°C for 30 min in a vacuum oven to improve its dimensional stability. Parylene-C was used as an organic dielectric layer. Its dielectric strength is 5600 (DC volts/mil), its sheet resistance is 10^{14} (Ω, 23°C, 50%), and its dielectric constant is 3.15 (60 Hz). The solution-processable organic semiconductor used for the printed OTFT was P3HT, which shows the highest reported field-effect mobility.[15,16]

In this work, we fabricated master patterns by electron-beam lithography onto a quartz substrate with dimensions 125 × 125 × 2.3 mm. The pattern area of 30 × 30 mm was divided into 4 areas, each with a unit device, a 4-pixel, and a 6-pixel array structure. The composite stamps of h-PDMS and s-PDMS fabricated using the master were made up of a thin layer (~500 μm) of h-PDMS bonded to a thick slab (3±0.5 mm) of s-PDMS. The h-PDMS solution was prepared by mixing 3.4 g of VDT-731 ((vinylmethylsiloxane) (dimethylsiloxane) copolymer), 18 μl of SIP6831.1 (platinum-divinyltetramethyl-disiloxane complex in xylene), and 5 μl of 87927 modulator. Afterwards, the mixture was degassed for 1 min using a micromixer, 1 g of HMS-301 ((vinylmethylsiloxane) (dimethylsiloxane) copolymer) was added, and the h-PDMS solution was gently stirred. We then spin-coated (1000 rpm for 20 s) a thin h-PDMS layer onto the master surface and cured it at 60°C for 1 h. After the polymerization, a mixture of Sylgard 184A and Sylgard 184B, in the form of liquid prepolymer, was poured onto the h-PDMS layer and cured at 80°C for 1 h. Then, the composite stamp was carefully peeled off from the master surface.

Figure 1 shows the schematic fabrication process of the printed OTFT by microcontact and direct printing using the h-PDMS stamp and low-viscosity Ag ink. First, we deposited 1000 Å of ITO as an etching layer on a PEN plastic substrate using an e-beam deposition device, and then carried out microcontact printing using the h-PDMS stamp and self-assembled monolayer (SAM) of a 0.2 mM solution of hexadecanethiols (HDT). We then selectively etched the ITO using a solution of LCE-12K (Cyantek) and fabricated the gate electrodes.

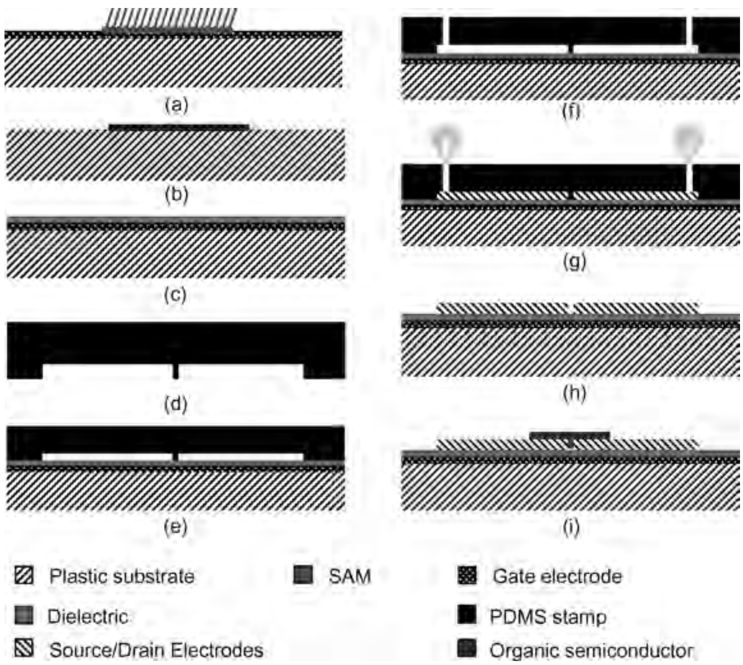


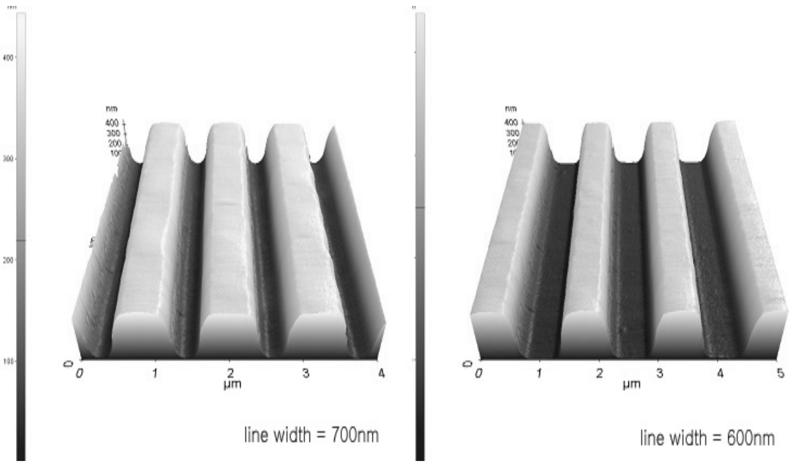
Fig. 1. Fabrication of printed OTFT by microcontact and direct printing (a) SAM solution inked onto ITO-deposited PEN substrate, (b) fabricated gate electrode, (c) deposited and patterned parylene-C dielectric layer, (d) fabricated h-PDMS stamp, (e) h-PDMS stamp laminated onto formed gate dielectric layer, (e) fabricated injection holes, (f) injected conductive Ag ink, (g) fabricated source and drain electrodes, and (h) P3HT organic semiconductor jetted onto prefabricated contact electrodes.

On the fabricated gate electrodes, parylene-C organic dielectric layers between 4000 and 9000 Å thick were formed using a specialized deposition coater at room temperature. The patterned organic dielectric layer was selectively etched using O_2 plasma for 10 min. We fabricated source and drain electrodes using the h-PDMS stamp of dimensions of 125 × 125 × 3 (±0.5) mm with 5, 10, and 20 μm channel lengths (L) and differing channel widths (W) and pattern shapes, and then the electrodes were physically placed in contact with h-PDMS stamp, and an ink injection hole was created in the h-PDMS stamp. The source and drain electrodes were formed by direct printing, wherein low-viscosity and low-resistance conductive Ag ink was injected. Finally, we formed an organic semiconductor using e-beam deposition (HELISYS) and using an ink-jet system (UNISYS) whereby the vacuum deposition of a 100-nm-thick pentacene layer at a rate of 0.05 nm/s and a 45-nm-thick pentacene layer at a rate of 0.03 nm/s were carried out, and 100 μl of P3HT was ink-jet printed 10 times. During the fabrication of the printed OTFT, to preserve the flatness, we used dry film photoresist (DFR) as an adhesion layer and a glass substrate as a rigid layer adhering to the PEN layer (not shown here). Then, we placed the glass substrate on a hot plate maintained at 60°C, cut the DFR film to the required size, and adhered the DFR film flat onto the glass substrate using a roll laminator. We then adhered the PEN plastic substrate to the glass substrate on the hot plate without the use of a passivation layer.

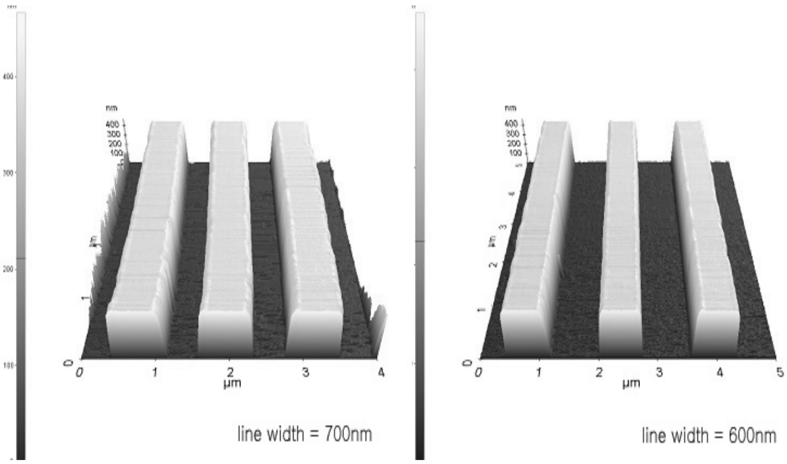
3. Experiment and Results

By the above procedure, which included microcontact and direct printing using an h-PDMS stamp mask, printed OTFT devices with channel lengths of 5, 10, and 20 μm were fabricated on a 5 inch substrate without pattern defects. Figure 2 shows the results of comparing the accuracy of the replication of the s-PDMS stamp with that of the h-PDMS stamp by analyzing them by atomic force microscopy (AFM, NanoMan, VEECO) in the case when they have pattern sizes of 600 and 700 nm. Figure 2(a) shows the result for the s-PDMS stamp, and it was ascertained that not all the pattern corresponded to the master in shape and that the pattern consisted of trapezoids, i.e., the top face was different in size from the bottom face, and that the space between a adjacent patterns was not exactly distinguishable. Figure 2(b) shows that the h-PDMS stamp has a replicated pattern exactly corresponding to the master pattern and has a high accuracy of filling and releasing. Also, as a surface characteristic, by measuring the wettability, it was demonstrated that the h-PDMS stamp was hydrophobic with a contact angle of 110° and a surface energy of 22 dyne/cm. The adhesion force was 12 nN, which was very low.

Figures 3(a) and 3(b) respectively show the actual h-PDMS stamp and the printed OTFT devices with various channel lengths between 5 and 20 μm and a channel width of 500 μm, with various spaces between the lines. Figure 3(a) shows the injection test carried out during direct printing using conductive Ag ink with a low viscosity of 4 cps (at 22°C) and a low resistance of 0.084 Ω (sq/mil (25 μm)) (see the inset). Figure 3(b) shows the result of depositing pentacene on the OTFT devices at the prefabricated source and drain electrodes on the ITO patterned 5 inch PEN substrate. Figure 3(c) shows an optical microscope image of a printed OTFT array using pentacene as the semiconductor,



(a)



(b)

Fig. 2. AFM images showing accuracy comparison of the fabricated line patterns between (a) s-PDMS and (b) h-PDMS stamps for pattern sizes of 600 and 700 nm.

parylene-C as the gate dielectric layer, ITO as the gate electrode, and Ag source and drain electrodes. For the pattern formation of the source and drain electrodes, a 1 wt.% solution of P3HT in high-purity chloroform was ink-jet printed onto the PEN substrate and then cured at 60°C for 5 min on a hot plate in air, as shown in Fig. 3(d). The printed OTFTs shown in Fig. 3 were fabricated without any defects in the patterns; however, it was ascertained that for this type of Ag ink and method of injection, the pattern formation was poor and a number of defects appeared such as reduced size, sagging, shrinking, deformation, and a filling defect, so that the pattern was hardly fabricated, as shown in Fig. 4. It was established that the printed OTFT was incompletely formed due to the

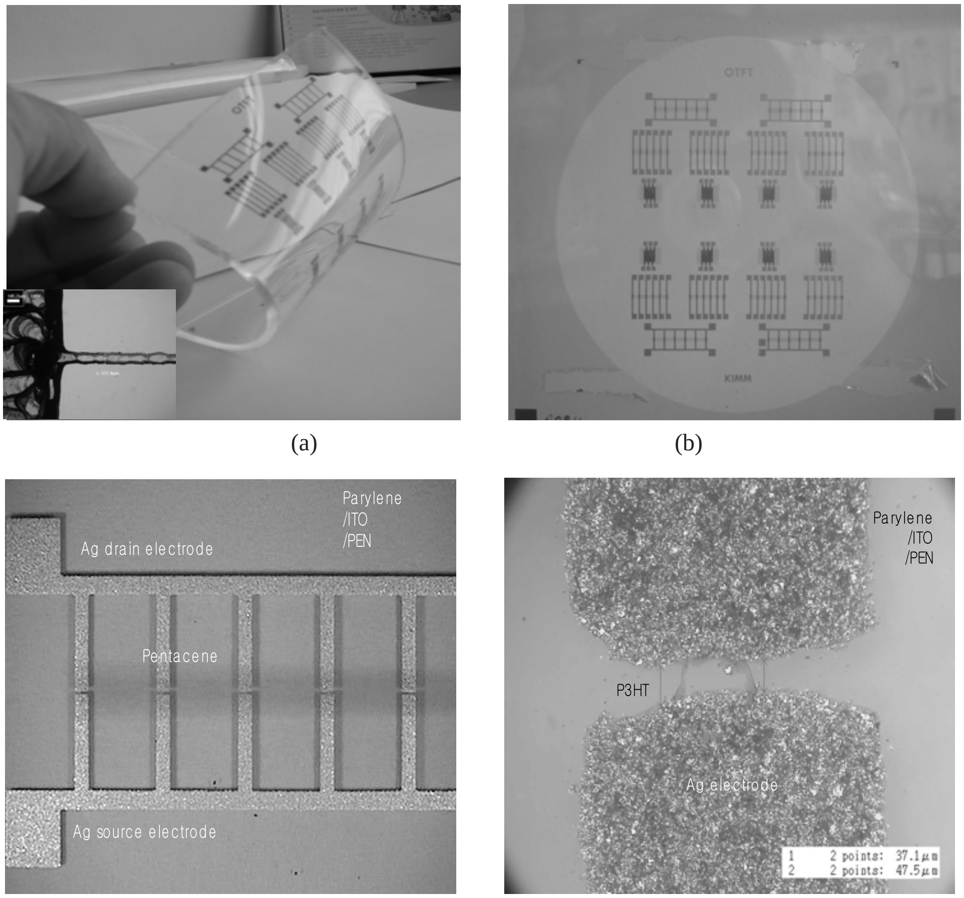
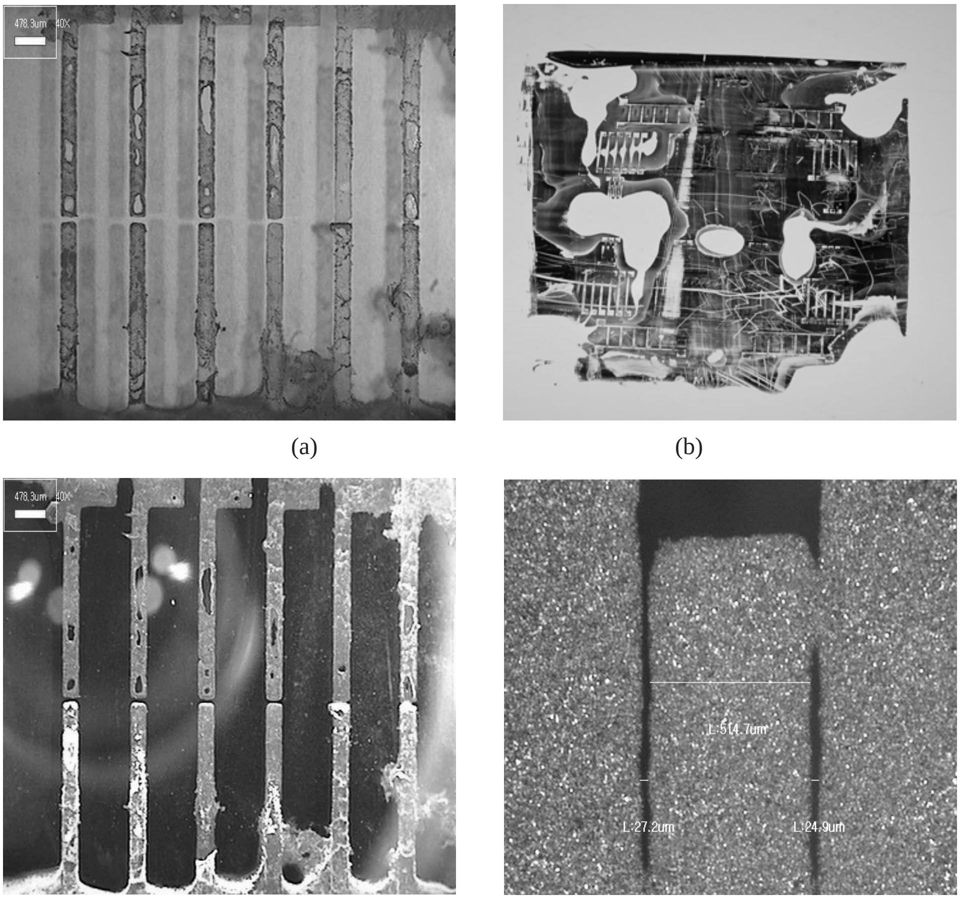


Fig. 3. Images of fabrication of printed OTFTs: (a) h-PDMS stamp, (b) printed OTFT devices of 125 × 125 mm size, (c) pentacene deposited onto OTFT, preformed parylene-C dielectric layer, ITO gate, and Ag source and drain electrodes, and (d) ink-jet printing of solution of P3HT organic semiconductor onto Ag source and drain electrodes.

effect of the contact between the h-PDMS stamp and the PEN substrate. It is necessary to optimize the surface treatment process, the method of injection, and the fabrication process including the curing temperature and the curing time in a new method.

Printed OTFT devices were fabricated by an all-room-temperature process and characterized in air. Figures 5 and 6 show the measurement results for the transfer and output characteristics. Figure 5 shows a typical plot of drain current I_{DS} versus drain voltage V_{DS} output characteristics at various gate voltages V_{GS}, which corresponds to a device using P3HT as the semiconductor, a 7000 Å coating of parylene-C as the gate dielectric layer, a 1000 Å ITO coating as the gate electrode, and Ag source and drain electrodes. Figure 6 shows a graph of the transfer characteristics including an I_{DS} versus



(a) (b)

(c) (d)

Fig. 4. Images of failures and defects in printed OTFT fabrication: (a) infidelity, (b) leakage of ink, (c) pinholes, and (d) short channel.

V_{GS} plot and an $|I_{DS}|^{1/2}$ versus V_{GS} plot. The figure corresponds to a printed OTFT with a channel length of L = 24 μm (designed length: L = 10 μm), a width of W = 480 μm (designed width: W = 500 μm), a P3HT semiconductor, a parylene-C gate dielectric layer, an ITO gate electrode, and Ag source and drain electrodes. The field-effect mobility of this device was 0.08 cm^2/Vs, while the threshold voltage V_T was about –2.94 V. The I_{on}/I_{off} ratio was above 10^3 when V_{GS} was scanned from –20 to +5 V. Figure 6(b), which corresponds to the same device as that in Fig. 6(a), shows a plot of the transfer characteristics, and the calculated mobility value is 0.073 cm^2/Vs at V_{DS} = –18 V. The value of V_{DS} is chosen so that it lies in the saturation regime of the I_{DS} versus I_{DS} curve. For this device, the channel length was 24 μm and the width was 480 μm.

As a result of evaluating the printed OTFT fabricated by the proposed process using

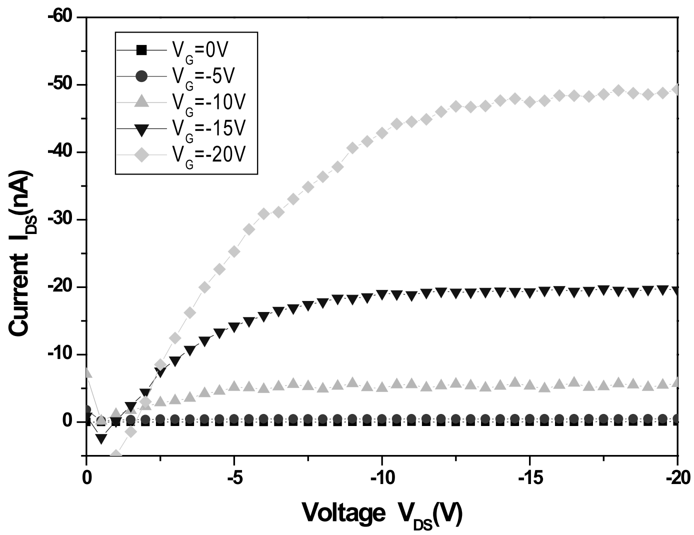
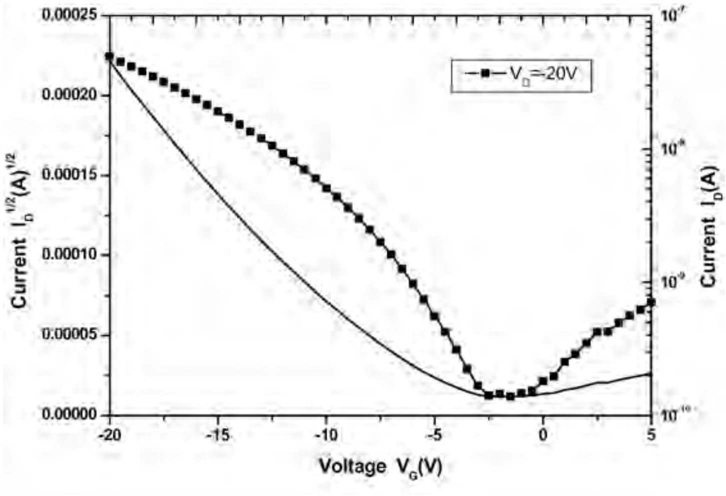


Fig. 5. Drain current I_{DS} versus drain voltage V_{DS} for a range of gate-voltage values V_{GS}: device characteristics for a printed P3HT OTFT having an ITO gate electrode, a 7000 Å coating of parylene-C as the gate insulating layer, and Ag source and drain electrodes with L=24 µm and W=480 µm. V_{DS} was varied from 0 to –20 V and V_{GS} was varied from 0 to –20 V in steps of –5 V (collaboration with J. B. Koo, ETRI).

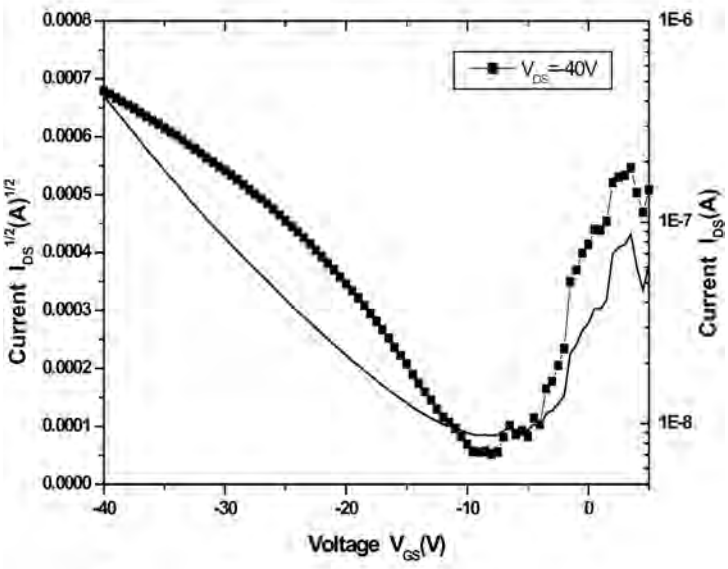
low-viscosity Ag ink and an h-PDMS stamp, the following parameters were obtained: a mobility of 0.06 (±0.02) cm^2/Vs, an I_{on}/I_{off} current ratio of 10^3, an I_{off} current of 1.26×10^{-10} A, a subthreshold slope of 2.53 V/decade, and a threshold voltage of –2.94 V.

4. Conclusion

Microcontact and direct printing using an h-PDMS stamp, low-viscosity conductive Ag ink, and a SAM made it possible to fabricate a printed OTFT with a channel length as small as 5 µm on a PEN plastic substrate. The number of steps in the fabrication process was reduced by 20 compared with photolithography, and there were no need to carry out UV exposure, development, or removal processes. Also, the h-PDMS stamp replicated the master pattern exactly and demonstrated high accuracy in filling and releasing. Since the fabrication of the printed OTFT devices was carried out at room temperature, it was possible to minimize dimensional distortion and to provide better alignment in the patterning process, thus preventing performance degradation. Also, during the device fabrication, there was no substrate shrinkage, bending, or pattern deformation. As a result of measuring the electrical characteristics of a printed OTFT fabricated by the proposed simple process, the field-effect characteristic was verified. This technology



(a)



(b)

Fig. 6. Transfer characteristics of drain current IDS versus gate voltage V_{GS} and $|I_{DS}|^{1/2}$ versus VGS for a printed P3HT OTFT (W/L = 480 μm/24 μm): (a) V_{DS} = –20 V and (b) V_{DS} = –40 V (collaboration with J. B. Koo, ETRI)

of using patterned electrodes and soluble organic semiconductors combined with large-area stamping and printing techniques is believed to have the potential to reduce manufacturing costs by eliminating the need for photolithography.

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