*Sensors and Materials*, Vol. 20, No. 7 (2008) 381–387
MYU Tokyo

S & M 0735

# Low-Noise Logarithmic Active Pixel Sensor Using a Gate/N-Well-Tied PMOSFET-Type Photodetector

Hyo-Young Hyun, Jae-Sung Kong[1] and Jang-Kyoo Shin[1,*]

Department of Sensor and Display Engineering, Kyungpook National University,
1370 Sankyuk-dong, Buk-gu, Daegu 702-701, Korea
[1]School of Electrical Engineering and Computer Science, Kyungpook National University,
1370 Sankyuk-dong, Buk-gu, Daegu 702-701, Korea

(Received July 31, 2008; accepted November 18, 2008)

***Key words:*** logarithmic active pixel sensor, gate/n-well-tied PMOSFET-type photodetector, simplified correlated-double sampling (SCDS)

A logarithmic active pixel sensor (APS) was designed as an image sensor. In the image sensor, a simplified correlated-double-sampling (SCDS) technique was applied to effectively reduce fixed pattern noise (FPN). In addition, a gate/n-well-tied p-channel metal-oxide-semiconductor (MOS)-type photodetector (PMOSPD) was used to obtain a large output swing. The measurement of the image sensor for image acquisition was carried out using a data acquisition (DAQ) card and LabVIEW system. From the experimental results, it was confirmed that the operation of the image sensor with noise reduction circuit is effective for reducing FPN.

## 1. Introduction

Wide dynamic range, moderate output swing, rapid response time, and high signal-to-noise ratio (SNR) are considered essential for good performance in an image-capturing device. A charge-coupled device (CCD) and a complementary metal-oxide-semiconductor (CMOS) image sensor (CIS) are commonly used for image capture. The CCD has better image quality and noise characteristics than the CIS; however, the CCD requires high supply voltage and a special fabrication process. On the other hand, the CIS requires a low supply voltage and a standard CMOS process, and is compatible with other circuits for image processing. Because of those advantages, the CIS is under focus these days.

Previously, charge-accumulation-type active pixel sensor (APS) had been widely used for image capturing in the CIS field.[(1)] This APS has several advantages including low power consumption, high SNR, large output swing, small size, and so on. However, its operation speed varies because it requires an exposure time for the accumulation of

*Corresponding author: e-mail: jkshin@ee.knu.ac.kr

charge. Furthermore, the dynamic range is not sufficiently wide. The dynamic range is the range between the maximum and minimum possible values. Therefore, those disadvantages limit the range of applications for charge-accumulation-type APS.

To overcome those disadvantages, a logarithmic APS might be considered.[2–4] The logarithmic APS has an advantage compared with the charge-accumulation-type APS. It has a wide dynamic range because of its image compression capability. Despite this advantage, logarithmic APS has several problems, such as poor SNR, large area consumption, and so on.

A conventional correlated-double-sampling (CDS) circuit, which is used for the reduction of fixed pattern noise (FPN) in CIS, has two capacitors for memorizing signals. However, its two capacitors require large area consumption. To enhance the resolution of an image sensor, the CDS circuit should occupy a minimum area.

In this paper, a simple and effective method is proposed to overcome those disadvantages of logarithmic APS and CDS circuit. The CIS chip has been designed and fabricated using a logarithmic APS, which employed a p-channel metal-oxide-semiconductor (MOS)-type photodetector (PMOSPD) and SCDS technique. The chip was implemented using 0.35 μm 2-poly 4-metal standard CMOS technology.

## 2. Circuits

### 2.1 *MOS-type photodetector*

A photodiode or a photobipolar junction transistor (BJT) was used for logarithmic APS. Although logarithmic APSs have a wide dynamic range of over 100 dB, they have several problems, such as poor SNR, large area consumption of unit-pixel and narrow range of output swing.

To overcome those problems, the PMOSPD was applied to the logarithmic APS.[5] A cross-sectional view and schematic of the PMOSPD are shown in Fig. 1. Its pixel size is $5.1\times 3.55$ μm$^2$ for the PMOSPD.

The operational principle of the PMOSPD is as follows.[5] Photogenerated electron-

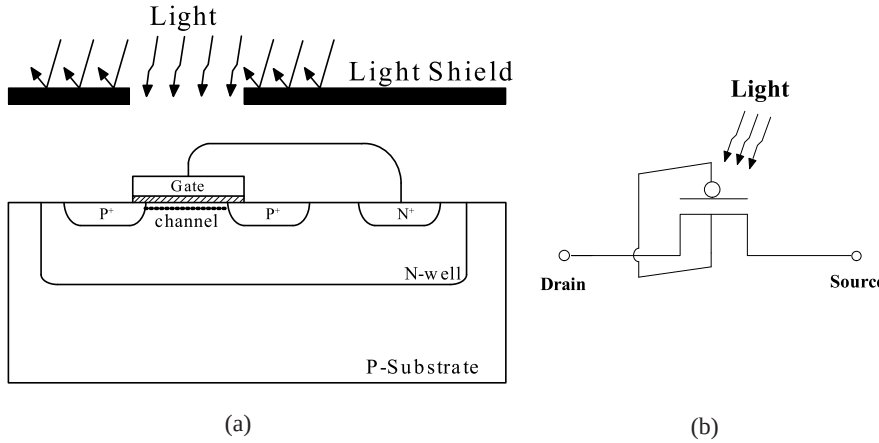



Fig. 1. Gate/N-well-tied PMOS-type photodetector: (a) cross-sectional view; (b) schematic.

hole pairs (EHPs) are separated by a vertical electric field, which is caused by differential Fermi level between the gate and n-well. The generated holes are driven to the channel and then they are swept to the drain by bias voltage. On the other hand, the generated electrons move to the n-well and then they are accumulated. These accumulated electrons are fed back to the gate through the gate/n-well connection, which is acting as a negative gate bias. The feedback leads to the further turn-on of the MOSFET. Therefore, the PMOSPD, which has a high sensitivity, can be used to obtain an amplified photocurrent.

According to the incident light intensity, the channel potential of the PMOSPD varies. Variation of channel potential induces the photocurrent variation of the PMOSPD.[4] The PMOSPD has several advantages, such as compatibility with the standard CMOS process, small size and a high sensitivity. Figure 2 shows its I-V characteristic curves in several illumination conditions from dark to 10,000 lx.

## 2.2 *Noise reduction*

A noise reduction circuit is one of the essential circuits for better image quality. CDS technique is commonly used for the reduction of noise in the field of CIS. A conventional CDS has two capacitors for memorizing both an image signal and a reference signal. However, two capacitors induce large area consumption. Therefore, it is not suitable for a high-resolution imager because those capacitors are a main factor in chip area consumption problems. To improve the area consumption problem, Kavadias proposed an SCDS technique, which is very effective for reducing the noise with minimum area consumption.[6]

Since the SCDS circuit consists of only one capacitor and five switches, area consumption could be minimized, compared with the conventional CDS technique. Therefore, a SCDS circuit is useful for high resolution, because the resolution is directly related to area consumption.

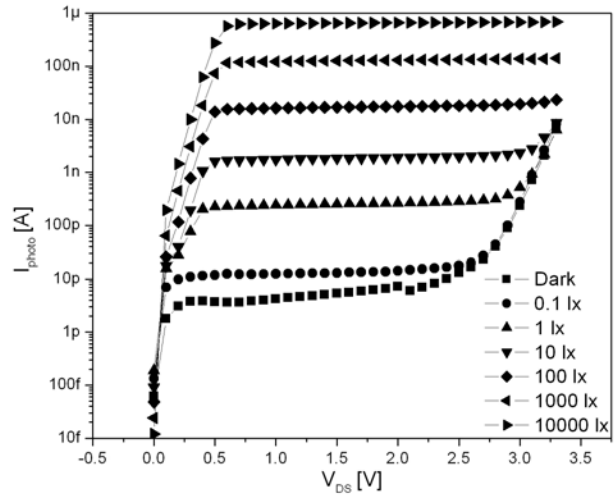



Fig. 2. I-V characteristic curves of the gate/n-well-tied PMOS-type photodetector.

Figure 3 shows the electronic circuit schematic of the proposed logarithmic APS. The logarithmic APS consists of three MOSFETs (PMOSPD, which is the PMOS-type photodetector, MN2, and MN3). It continuously sends output voltage according to incident light. Compared with a charge-accumulation-type APS, the logarithmic APS requires an additional circuit for noise reference. MOSFET MP1 offers a constant current for the noise reference signal. To reduce the current variation, which is caused by process variation, the MP1 was divided into five MOSFETs, and they were spread over neighboring pixels.

The reference current signal and the light-induced current signal are selected using an external control signal VMODSL. MOSFET MN1 and MP2 are operated as switches. Figure 4 shows the external control signals, which are generated by a LabVIEW system, for operation of the proposed chip. When SW1 is turned on and SW2 is turned off at the same time, a light-induced signal is sampled. When SW1 is turned off and SW2 is turned on at the same time, a reference signal is sampled. After the noise is subtracted from the light-induced signal, the output signal is read out.

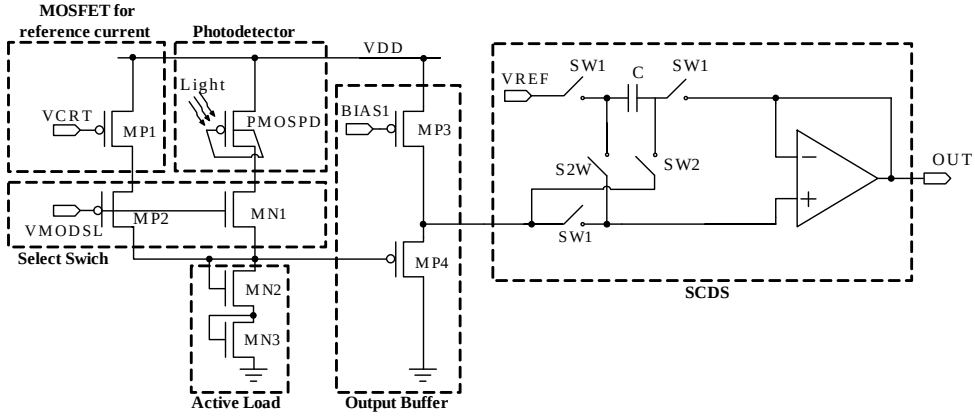



Fig. 3. Circuit schematics of the logarithmic APS and SCDS.

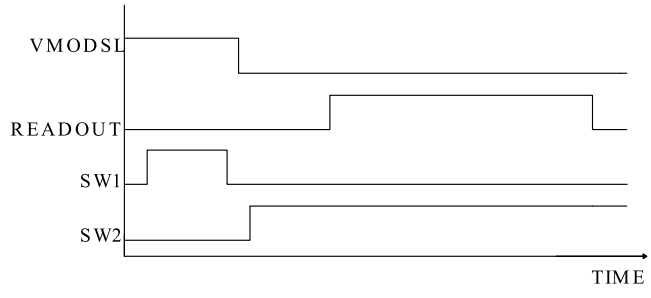


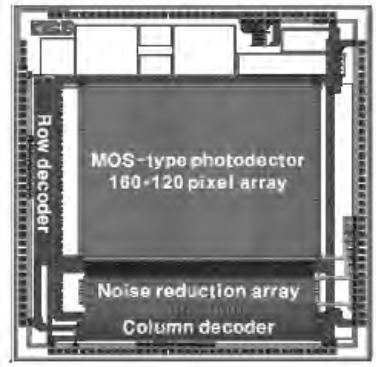

Fig. 4. Timing diagram.

## 3. Experimental Results

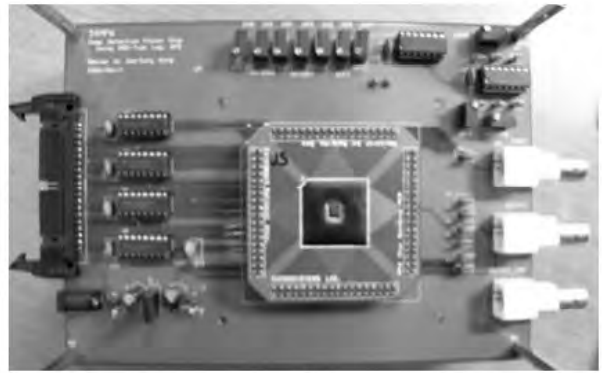
The layout and photograph of the fabricated chip on a printed circuit board (PCB) are shown in Fig. 5. This chip was fabricated using 0.35 μm double-poly four-metal CMOS technology. The fabricated chip consists of a noise reduction circuit, row and column decoder, and the PMOSPD. Each pixel is selected by external selection signals using row and column decoders. The output data acquisition and generation of the external selection signal are carried out using a LabVIEW system.

The PCB consists of several variable resistors, BNC connectors, 40-pin connector, and digital signal buffers. The variable resistors are for generating biases and the BNC connectors are for transferring analog output signals to a data acquisition (DAQ) card of the LabVIEW system. The 40-pin connector is for the external signals and the digital signal buffers are for interconnection between the DAQ card and the chip.

Figure 6 shows the output results of 140 pixels under several illumination conditions from dark to 10,000 lx. When the PMOSPD is operated without a noise reduction circuit, the average FPN of each illumination condition is approximately 110 mV peak-

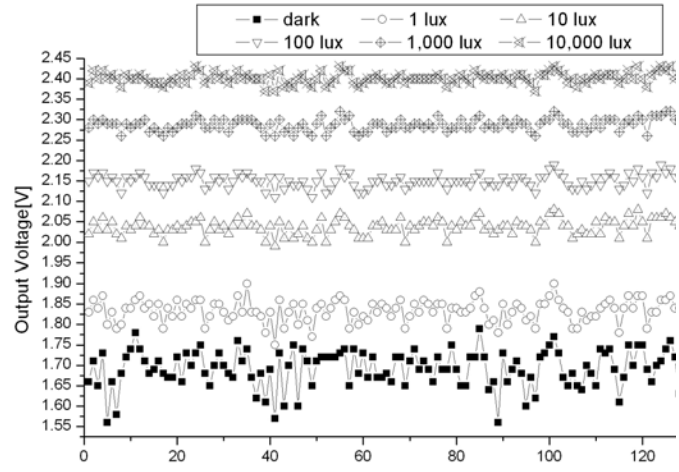



(a)

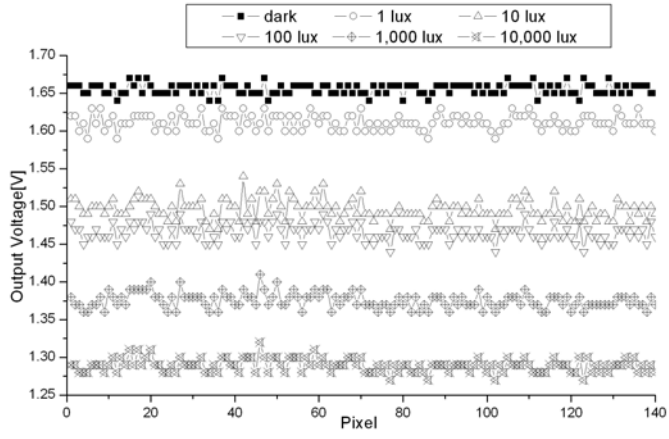


(b)

Fig. 5. (a) Layout of the fabricated chip; (b) fabricated chip on a printed circuit board (PCB).




(a)




(b)

Fig. 6. Measured output voltages: (a) before noise reduction; (b) after noise reduction.

Table 1
Characteristics of the fabricated image sensor.

| | |
|---|---|
| Technology | 0.35 μm 2-poly 4-metal standard CMOS technology |
| Pixel pitch | 5.1 μm × 3.55 μm for MOS-type sensor,<br>23 μm × 72 μm with noise reduction circuit |
| Power consumption | About 30 μW for a unit-pixel with noise reduction circuit |
| Output swing | 306 mV under the condition of dark~10000 lx |
| FPN | 20 mV peak-to-peak |

to-peak. However, when the PMOSPD is operated with the noise reduction circuit, the average FPN of each illumination condition is approximately 50 mV peak-to-peak. Therefore, we can confirm that the SCDS circuit can reduce the average FPN by 55%.

## 4. Conclusion

A logarithmic APS was designed with a noise reduction circuit for CIS. To overcome several problems of logarithmic APS, a highly sensitive PMOSPD for large output swing and a SCDS for noise reduction with small area consumption have been applied. The proposed circuit was implemented using 0.35 μm 2-poly 4-metal standard CMOS technology. Through experiments, the operation of the proposed circuit has been investigated. From the results, it is confirmed that the proposed circuit shows better performance in terms of FPN, speed, power consumption, and dynamic range with small area consumption.

## Acknowledgements

This work was supported by the Brain Science Research Center at KAIST and Brain Korea 21 (BK21) Program.

## References

1 A. Moini: Vision Chips or Seeing Silicon, CHiPTec (1997).
2 S. Kavadias, V. Dierickx, D. Schelffer, A. Alaerts, D. Uwaerts and J. Mogaerts: IEEE J. Solid-State Circuits **35** (2000) 1146.
3 L.-W. Lai, C.-H. Lai and Y.-C. King: IEEE Sensors Journal **4** (2004) 112.
4 M. Loose, K. Meier and J. Schemmel: IEEE J. Solid-State Circuits **36** (2001) 586.
5 W. Zhang and M. Chan: IEEE Trans. Electron Devices **48** (2001) 1097.
6 S. Kavadias: Electron. Lett. **35** (1999) 2112.