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Fabrication of Buried Nanochannels by Transferring Metal Nanowire Patterns

Daniel S. Choi* and Eui-Hyeok Yang[1]

Department of Materials Science and Engineering,
University of Idaho, Moscow, ID 83844
[1]Department of Mechanical Engineering, Stevens Institute of Technology, Hoboken, NJ 07030

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A method of fabricating channels with widths of 30–50 nm in silicon substrates with channels buried under overlying layers of dielectric materials has been demonstrated. Buried nanochannels with an opening size of 20×80 nm^2 have been successfully fabricated on a silicon wafer by transferring metal nanowire patterns. With further refinement, the method might be useful for fabricating nanochannels for the manipulation and analysis of large biomolecules at single-molecule resolution.

1. Introduction

A number of nanoscale channel fabrication methods have been reported for bionanotechnology applications.[1–10] The traditional electron beam lithography technique has been exploited to generate exposed nanometer-sized trenches for the analysis of biomolecules at single-molecule resolution.[1] An additional process step in sealing exposed trenches is required to complete such nanochannels. Currently, sealing techniques such as wafer bonding and soft-elastomer sealing require a flat, defect-free surface.[2] Moreover, the elastomer sealing process can lead to clogging due to soft material intrusion into the channels.[3] Various fabrication techniques using conventional machining, surface micromachining, step sidewalls, and laser machining methods have been reported for fabricating nanochannels[4–9] and microchannels.[10,11] In addition, a method of fabricating nanochannels without nanolithography has been reported by one of the authors' group in a previous paper.[12] Although the method described in ref. (12) provides a means of constructing nanochannels without using a sophisticated and high-cost process such as e-beam lithography, it was found that the yield of precision nanochannels obtained using such a technique was highly dependent on chemical mechanical polishing (CMP), which requires extensive hands-on control.

*Corresponding author: e-mail: dchoi@uidaho.edu

2. Experiments and Results

In this report, we describe a technique for fabricating nanometer-scale channels buried under dielectric materials. The features of this technique are the pattern transfer of metal nanowires and the selective etching of a patterned sacrificial layer to create an inner space for nanofluidic channels. An overview of the method is given in Fig. 1. The

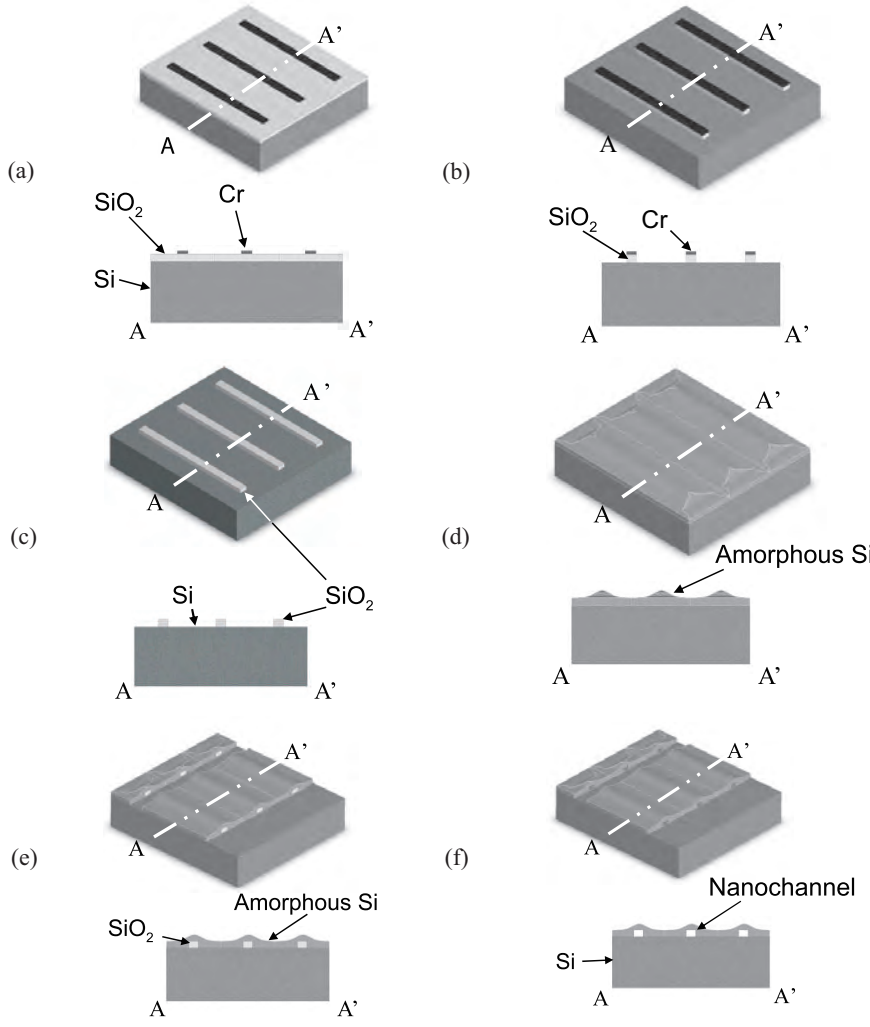


Fig. 1. Fabrication process of buried nanochannels. (a, b) An array of nanometer-scale metal (Cr) nanowire patterns was fabricated on a SiO_2/Si wafer by focused ion beam (FIB) lithography and a subsequent metallization/lift-off process and (c) SiO_2 nanowires were obtained after removing metal mask patterns. (d) An amorphous Si layer was deposited by plasma enhanced chemical vapor deposition (PECVD) on the SiO_2 nanowire patterns. (e) FIB milling was used to generate trenches at both the front and rear regions of nanowires. (f) As a result of a different etch rate of SiO_2 and amorphous Si in BOE, buried nanochannels were fabricated.

first step in this method is to establish a channel pattern by forming an array of metal nanowires on a SiO_2/Si substrate. An array of metal (Cr) nanowire patterns was first fabricated on a SiO_2/Si wafer by focused ion beam (FIB) lithography and a subsequent metallization/lift-off process (Fig. 1(a)). The metal nanowire patterns were transferred onto a SiO_2 layer by reactive ion etching (RIE), yielding sacrificial SiO_2 nanowires on a Si substrate (Fig. 1(b)). Figure 2 shows the fabricated SiO_2 nanowires prepared by FIB lithography and the subsequent RIE process. The nanometer-scale SiO_2 nanowires were obtained by removing the metal nanowire patterns (Fig. 1(c)). After removal of the metal patterns covering the SiO_2 nanowires, plasma-enhanced chemical vapor deposition (PECVD) was used to form an amorphous Si layer over the Si substrate as well as over the SiO_2 wires on the surface of the Si substrate (Fig. 1(d)). Figure 3 shows a cross-sectional view of SiO_2 nanowire patterns buried under a PECVD dielectric layer. After this step, FIB milling was used to generate trenches at both ends of each SiO_2 wire (Fig. 1(e)). The trenches serve as openings for the entry of chemicals (*e.g.*, buffered oxide etchant (BOE) for etching SiO_2). The sacrificial SiO_2 nanowires are etched out between the dielectric material (i.e., amorphous Si) and the Si substrate, leaving buried channels (Fig. 1(f)). Figure 4(a) shows the trenches formed by FIB milling to generate openings

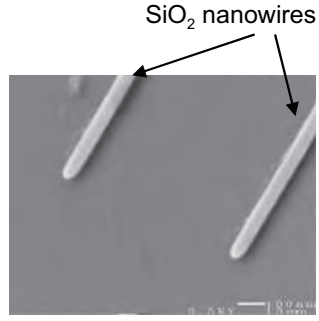


Fig. 2. Scanning electron microscopy (SEM) image showing nanometer-scale SiO_2 nanowires prepared by FIB lithography and subsequent RIE processes. The metal mask patterns still remain on the top of the SiO_2 nanowires.

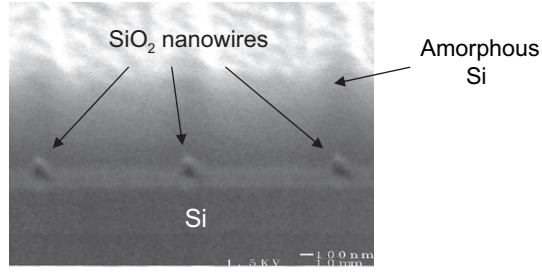
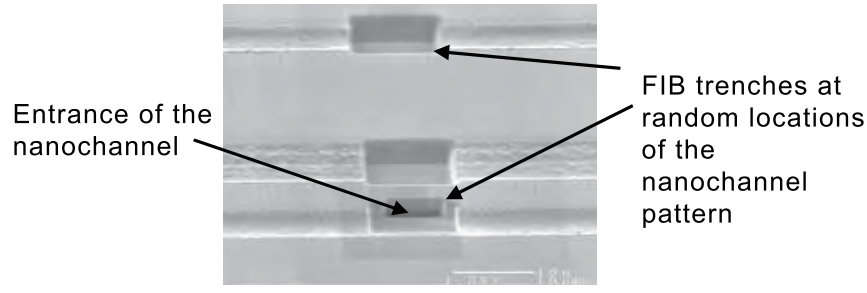
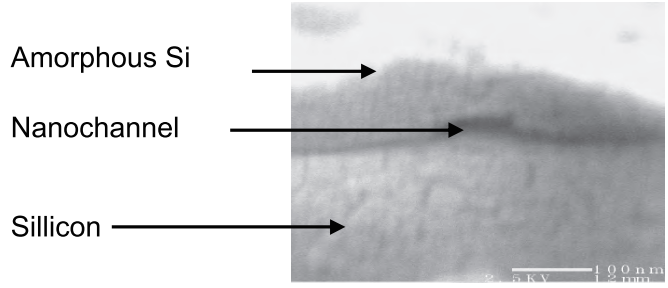


Fig. 3. Cross-sectional SEM image of sacrificial SiO_2 nanowires buried under the amorphous silicon layer.



(a)



(b)

Fig. 4. Fabricated Nanochannel. (a) SEM image showing a trench created by FIB milling to generate openings for sacrificial etching and analysis. (b) Cross-sectional SEM image of 20-nm-high, 80nm-wide channel. The successful fabrication of nanochannels by etching sacrificial oxide has been confirmed by observing SEM images of trench areas created by using FIB milling at random locations of nanochannel patterns.

for sacrificial etching and subsequent analysis, which investigated the features of the nanochannels using field emission scanning electron microscopy (FESEM). An enlarged view of a buried nanochannel is shown in Fig. 4(b). At this stage, FIB characterization was introduced to check the etching area. When a gallium (Ga) ion beam is scanned in a line on a surface, a trench is produced. The trench initially has an inverse Gaussian shape, as expected from the beam profile. As the dose is increased, the trench becomes sharp, narrow, V-shaped, and deep. The area of interest for observation (i.e., at the end of each channel) was ion milled. The sample was then tilted and observed by FESEM for high-resolution imaging. By checking both ends of the nanochannels (i.e., FIB milling formed two trenches at randomly chosen locations), we confirmed that nanochannels were successfully fabricated by etching oxide all the way through. Nanochannels, 3 μm long, 20 nm high, and 80 nm wide, were fabricated using this technique (See Fig. 4(b)). Five lengths (3, 6, 8, 10, and 20 μm) of pillar patterns were fabricated to determine the maximum length of nanochannels that can be fabricated without experiencing "diffusion-blocking"[13] during the etching of sacrificial pillar patterns. Mass transfer analysis was

performed to elucidate the oxide etch process of diffusion blocking necessary for the fabrication of nanochannels. We assumed that only Fick's Law governed the transport of the active chemicals (i.e., BOE) to the oxide surface. It was found that an extremely long etch time (>> 10 h) is required for generating nanochannels with lengths beyond 3 μm (from the openings), which corresponds to the experimental results. As a future work, buried nanochannels with smaller widths (less than 15 nm) will be fabricated for single molecule detection. Nanometer-scale ferromagnetic electrodes will be patterned on both ends of the nanochannel. Magnetic nanoparticles or nanowires attached by a single molecule will be transmitted through the buried nanochannel by applying a magnetic field between two ferromagnetic electrodes patterned on both ends of the nanochannel.

3. Conclusions

In summary, a new process technique for fabricating in-plane nanochannels buried under layers of dielectric materials has been demonstrated. Buried nanochannels with an opening size of 20×80 nm^2 have been successfully fabricated on silicon wafers by transferring metal nanowire patterns.

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